19-3550; Rev 0; 1/05

Delay Lines for High-Speed Clock Distribution Systems

General Description

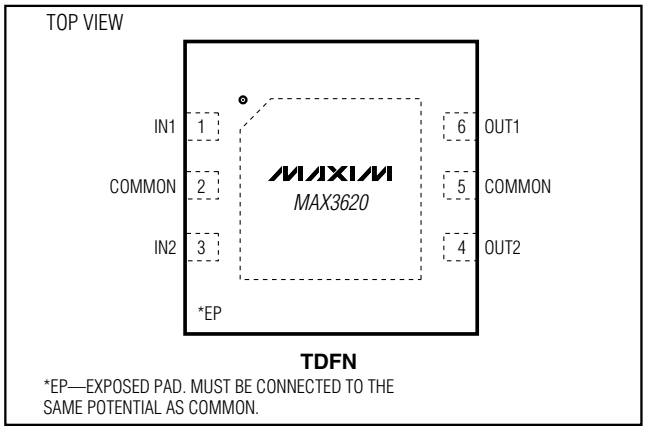
The MAX3620 series is a family of high-performance passive delay lines for use in QDR/QDRII synchronous memory systems. These delay lines support high-speed transceiver logic (HSTL) source terminated transmission with an unterminated load at the receiver, and deliver accurate delays of 0.75ns, 1.00ns, 1.25ns, and 1.50ns for the generation of the quarter clock phase. The MAX3620 is offered in a small 3mm x 3mm package which contains two delay lines of equal length that can be driven either differentially or single-endedly.

Applications

QDR/QDRII Memory Systems

Multiphase Clock Generation

Pin Configuration



Features

- ♦ **Supports HSTL Source Terminated Lines**
- ♦ **All-Passive Design**
- ♦ **Compatible with 100Ω Differential and 50Ω Single-Ended Transmission Lines**
- ♦ **Small 3mm x 3mm Package**

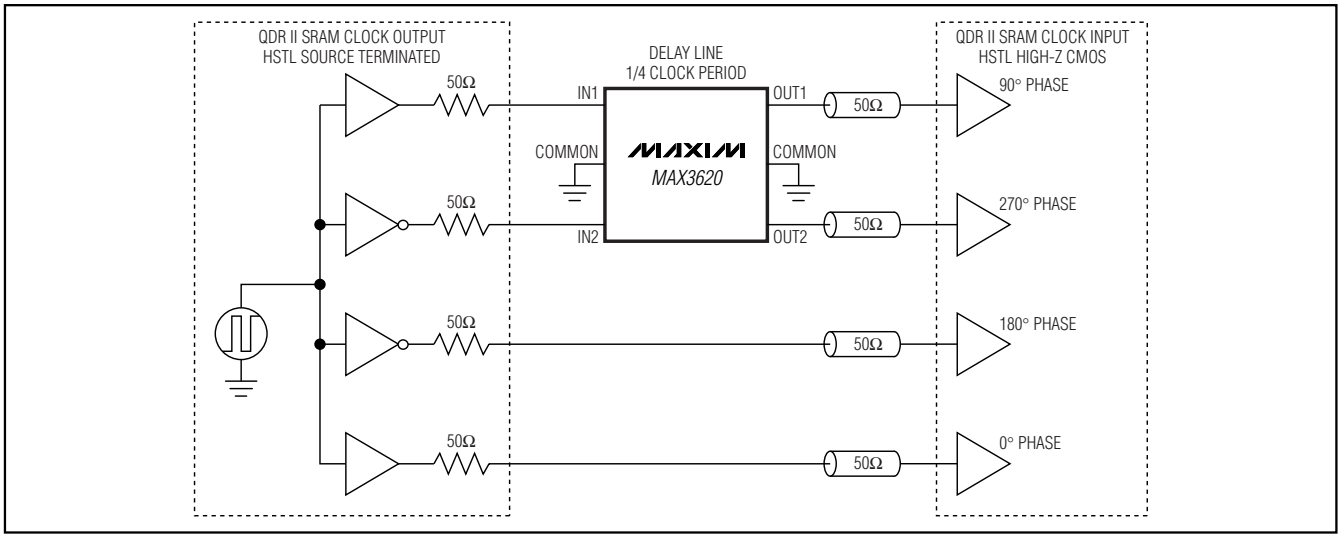
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3620AETT	-40°C to +85°C	6 TDFN
MAX3620BETT	-40°C to +85°C	6 TDFN
MAX3620CETT	-40°C to +85°C	6 TDFN
MAX3620DETT	-40°C to +85°C	6 TDFN

Selector Guide

PART	PKG CODE	TOP MARK
MAX3620AETT	T633-2	AJX
MAX3620BETT	T633-2	AIY
MAX3620CETT	T633-2	AIZ
MAX3620DETT	T633-2	AJA

Typical Application Circuit



Delay Lines for High-Speed Clock Distribution Systems

ABSOLUTE MAXIMUM RATINGS

Maximum DC Voltage between COMMON and IOs (IN1, IN2, OUT1, OUT2).....±2.0V

Operating Temperature Range .....-45°C to +85°C
Storage Temperature Range .....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical ambient temperature is +25°C. See Table 1 for more information.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Characteristic Impedance	Z_0	See Table 1 clock frequency			50		Ω
Delay Values		$Z_{LOAD} = Z_{SOURCE}$ (Note 1)	MAX3620A	0.65	0.75	0.85	ns
			MAX3620B	0.90	1.00	1.10	
			MAX3620C	1.15	1.25	1.35	
			MAX3620D	1.40	1.50	1.60	
Delay Matching		IN2-to-OUT2 relative to IN1-to-OUT1, $Z_{LOAD} = Z_{SOURCE}$		-20		+20	ps
Insertion Loss		$Z_{LOAD} = Z_{SOURCE}$ (Notes 1, 2, 4)	MAX3620A		2.5		dB
			MAX3620B		2.1		
			MAX3620C		2.3		
			MAX3620D		2.2		
		$Z_{LOAD} >> Z_{SOURCE}$, source termination only (Notes 5, 6)	MAX3620A		4.6		
			MAX3620B		3.8		
			MAX3620C		3.1		
			MAX3620D		3.4		
Cutoff Frequency, 3dB Loss Relative to 10MHz		$Z_{LOAD} = Z_{SOURCE}$ (Note 3)	MAX3620A		450		MHz
			MAX3620B		370		
			MAX3620C		320		
			MAX3620D		300		
Input Return Loss		$Z_{LOAD} = Z_{SOURCE}$, 50MHz to 1GHz (Note 3)			12		dB
Output Return Loss		$Z_{LOAD} = Z_{SOURCE}$, 50MHz to 1GHz (Note 3)			15		dB
Input Leakage at ±1.5V		IN1 or IN2 to grounded COMMON		-10		+10	µA
Output Leakage at ±1.5V		OUT1 or OUT2 to grounded COMMON		-10		+10	µA
Output Transition Time (20% to 80%)		$Z_{LOAD} = Z_{SOURCE}$ (Notes 1, 2)	MAX3620A		540		ps
			MAX3620B		620		
			MAX3620C		700		
			MAX3620D		760		
		$Z_{LOAD} >> Z_{SOURCE}$, source termination only (Note 5)	MAX3620A		590		
			MAX3620B		720		
			MAX3620C		810		
			MAX3620D		890		

ELECTRICAL CHARACTERISTICS (continued)

(Typical ambient temperature is +25°C. See Table 1 for more information.)

Note 1: Load and source resistance = 50Ω ±1%, capacitance ≤ 1pF. Input transition time (20% to 80%) = 300ps.
Note 2: The clock frequency is the maximum operational clock frequency listed in Table 1.
Note 3: Load and source resistance = 50Ω ±1%, capacitance ≤ 1pF.
Note 4: Insertion loss is relative to a lossless 50Ω transmission line. Ideally, an insertion loss of 0dB will result in 0.5 times the open-circuit transmitter output.
Note 5: Source termination only (no-load termination), 5pF and 20kΩ at load, 300ps input transition time (20% to 80%). Load capacitance dominates performance.
Note 6: Insertion loss is relative to an ideal open 20kΩ load. Ideally, an insertion loss of 0dB will result in 0.998 times the open-circuit transmitter output.

Table 1. Recommended Operating Conditions

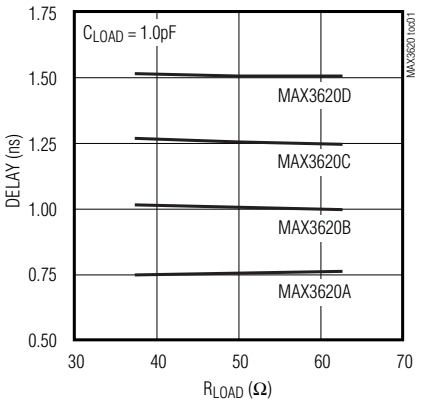
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Ambient Temperature		-40	+25	+85	°C
Recommended Load Capacitance	Z_{LOAD} >> 50Ω, source termination only		5		pF
Recommended Load Resistance	Z_{LOAD} >> 50Ω, source termination only		20		kΩ
Clock Frequency	MAX3620A	250		333	MHz
	MAX3620B	190		250	
	MAX3620C	150		200	
	MAX3620D	125		167	
Input Amplitude				1.5	V_{P-P}
Input Voltage Range		-1.5		+1.5	V

Delay Lines for High-Speed Clock Distribution Systems

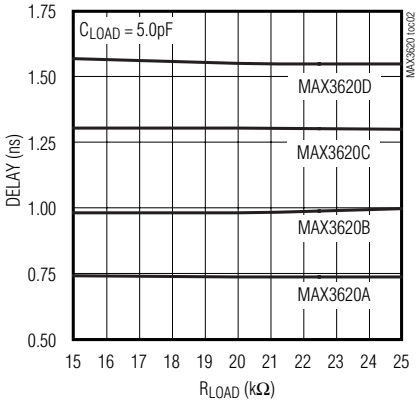
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

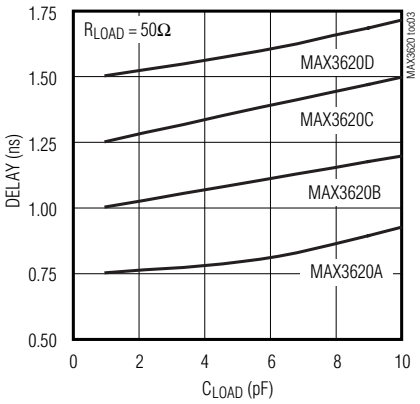
DELAY vs. R_{LOAD} (LOW LOAD RESISTANCE)



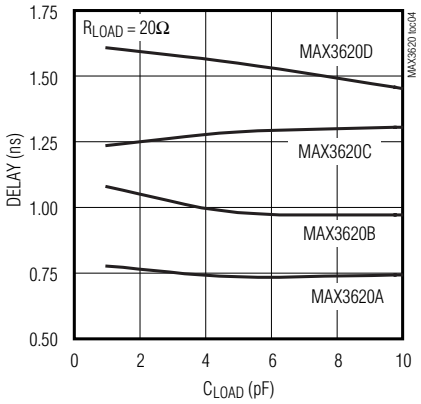
DELAY vs. R_{LOAD} (HIGH LOAD RESISTANCE)



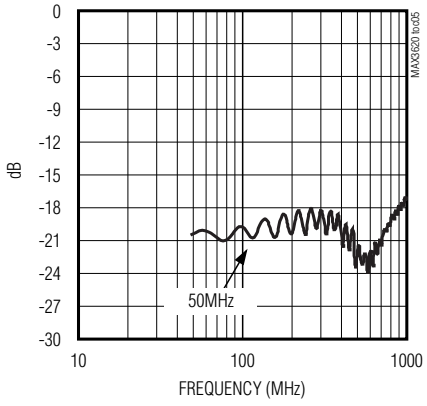
DELAY vs. C_{LOAD} (LOW LOAD RESISTANCE)



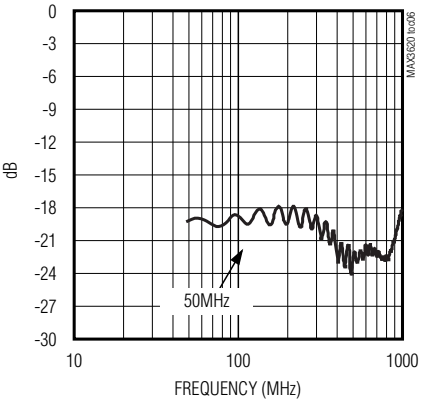
DELAY vs. C_{LOAD} (HIGH LOAD RESISTANCE)



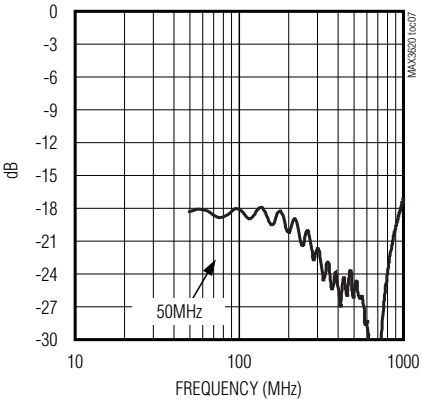
MAX3620A S11



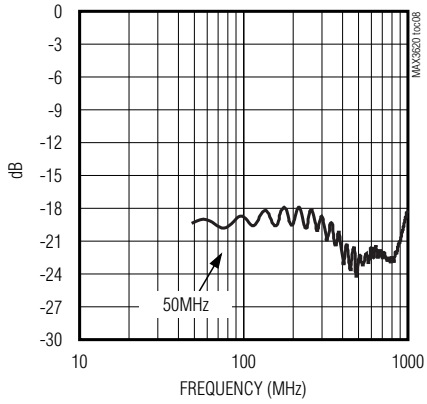
MAX3620B S11



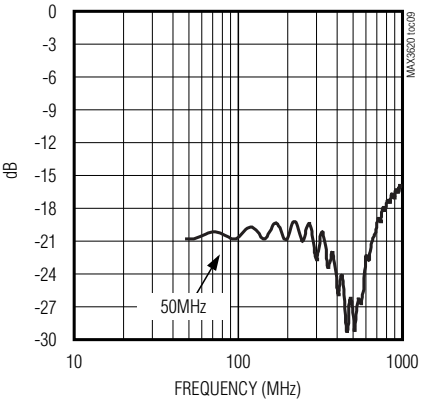
MAX3620C S11



MAX3620D S11

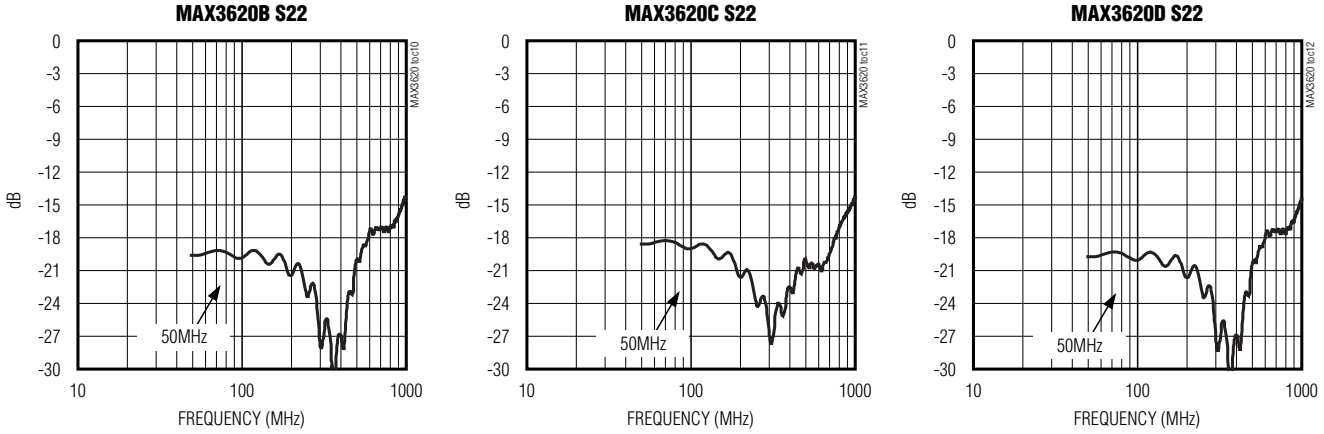


MAX3620A S22



Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	IN1	Single-Ended Input 1
2	COMMON	Common
3	IN2	Single-Ended Input 2
4	OUT2	Single-Ended Output 2
5	COMMON	Common
6	OUT1	Single-Ended Output 1
—	Exposed Pad	Connect to same potential as COMMON

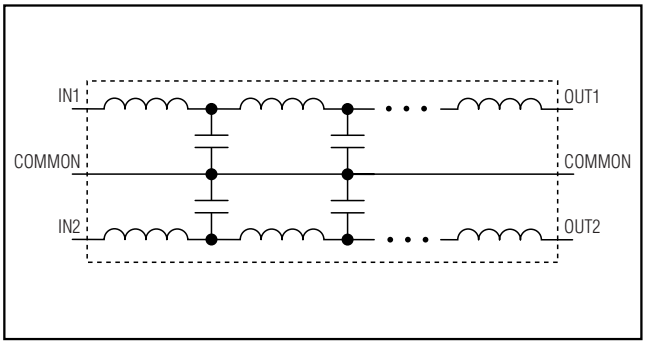


Figure 1. Functional Diagram

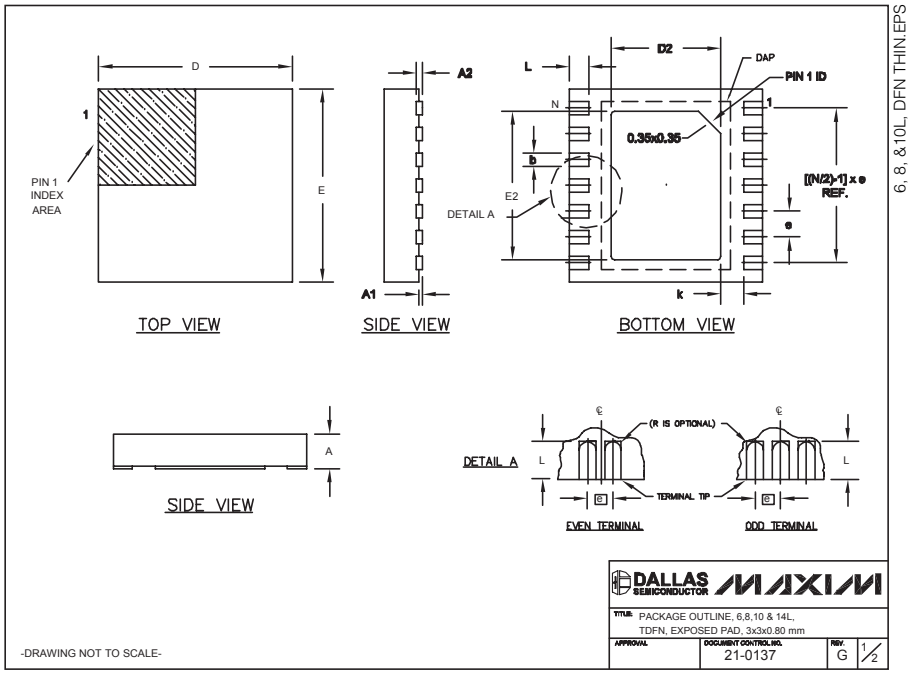
Detailed Description

The MAX3620 delay lines are transmission lines constructed with a series of L-C sections. Figure 1 is a functional diagram of the MAX3620. The distributed architecture of the MAX3620 allows for symmetrical impedance looking into each terminal. When the MAX3620 is used in single-ended operation, leave unused input/output open.

Delay Lines for High-Speed Clock Distribution Systems

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. G
2/2