FastEdge™ Series
CY2DP3110

1 of 2:10 Differential Clock/Data Fanout Buffer

Features

- **Ten ECL/PECL differential outputs**
- **One ECL/PECL differential or single-ended inputs (CLKA)**
- **One HSTL differential or single-ended inputs (CLKB)**
- **Hot-swappable/-insertable**
- **29 ps typical output-to-output skew**
- **95 ps typical part-to-part skew**
- **400 ps typical propagation delay**
- **0.1 ps typical RMS phase jitter**
- **1.5 GHz Operation (2.7 GHz maximum toggle frequency)**
- **PECL and HSTL mode supply range: V_{CC} = 2.5V± 5% to 3.3V±5% with V_{EE} = 0V**
- **ECL mode supply range: V_{EE} = –2.5V± 5% to –3.3V±5% with V_{CC} = 0V**
- **Industrial temperature range: –40°C to 85°C**
- **32-pin TQFP package**
- **Temperature compensation like 100K ECL**
- **Pin-compatible with MC100ES6111**

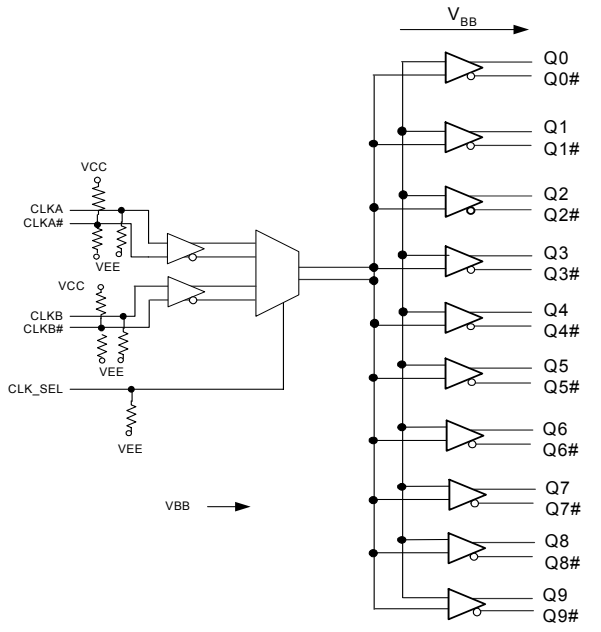
Functional Description

The CY2DP3110 is a low-skew, low propagation delay 2-to-10 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz.

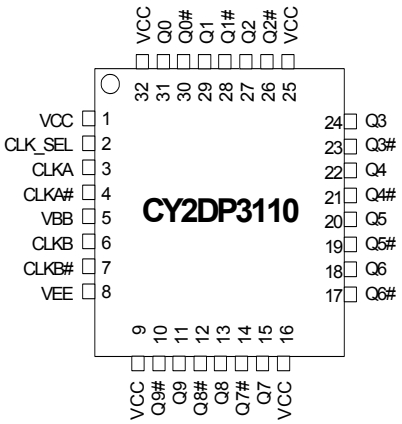
The device features two differential input paths that are multiplexed internally. This mux is controlled by the CLK_SEL pin. The CY2DP3110 may function not only as a differential clock buffer but also as a signal-level translator and fanout on HSTL single-ended signal to 10 ECL/PECL differential loads. An external bias pin, VBB, is provided for this purpose. In such an application, the VBB pin should be connected to either one of the CLKA# or CLKB# inputs and bypassed to ground via a 0.01-μF capacitor. Traditionally, in ECL, it is used to provide the reference level to a receiving single-ended input that might have a different self-bias point.

Since the CY2DP3110 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2DP3110 delivers consistent performance over various platforms

Block Diagram



Pin Configuration



Pin Definitions[1, 2, 3]

Pin	Name	I/O	Type	Description
2	CLK_SEL	I,PD	ECL/PECL	**Input Clock Select.**
3	CLKA	I,PD[1]	ECL/PECL	**Differential Input Clocks**.
4	CLKA#	I,PD/PU	ECL/PECL	**Differential Input Clocks**.
5	VBB	O	Bias	**Reference Voltage Output.**
6	CLKB,	I,PD	HSTL	**Alternate Differential Input Clocks**.
7	CLKB#	I,PD/PU	HSTL	**Alternate Differential Input Clocks**.
8	VEE	–PWR	Power	**Negative Power Supply.**
1,9,16, 25,32	VCC	+PWR	Power	**Positive Power Supply.**
31,29,27,24,22,20,18, 15,13,11	Q(0:9)	O	ECL/PECL	**ECL/PECL Differential Output Clocks**.
30,28,26,23,21,19,17, 14,12,10	Q#(0:9)	O	ECL/PECL	**ECL/PECL Differential Output Clocks**.

Table 1.

Control	Operation
CLK_SEL	
0	CLKA, CLKA# input pair is active (Default condition with no connection to pin) CLKA can be driven with ECL- or PECL-compatible signals with respective power configurations
1	CLKB, CLKB# input pair is active. CLKB can be driven with HSTL compatible signals with respective power configurations

Governing Agencies

The following agencies provide specifications that apply to the CY2DP3110. The agency name and relevant specification is listed below in *Table 2*.

Table 2.

Agency Name	Specification
JEDEC	JESD 020B (MSL) JESD 8-6 (HSTL) JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–B (skew,jitter)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:
1. In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power.
2. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between V_{CC} and V_{EE}.
3. V_{BB} is available for use for single-ended bias mode for |3.3V| supplies (not |2.5V|).

Absolute Maximum Ratings

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Positive Supply Voltage	Non-Functional	–0.3	4.6	V
V_{EE}	Negative Supply Voltage	Non-Functional	-4.6	0.3	V
T_S	Temperature, Storage	Non-Functional	–65	+150	°C
T_J	Temperature, Junction	Non-Functional		150	°C
ESD_h	ESD Protection	Human Body Model	2000		V
M_{SL}	Moisture Sensitivity Level		3		N.A.
Gate Count	Total Number of Used Gates	Assembled Die	50		gates

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
I_{BB}	Output Reference Current	Relative to V_{BB}		|200|	uA
LU_I	Latch Up Immunity	Functional, typical	100		mA
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	35[4]		°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	76[4]		°C/W
I_{EE}	Maximum Quiescent Supply Current	V_{EE} pin		130[5]	mA
C_{IN}	Input pin capacitance			3	pF
L_{IN}	Pin Inductance			1	nH
V_{IN}	Input Voltage	Relative to V_{CC}[6]	–0.3	V_{CC} + 0.3	V
V_{TT}	Output Termination Voltage	Relative to V_{CC}[6]	V_{CC} – 2		V
V_{OUT}	Output Voltage	Relative to V_{CC}[6]	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current[7]	$V_{IN} = V_{IL}$, or $V_{IN} = V_{IH}$		I150I	uA

PECL/HSTL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Operating Voltage	2.5V ± 5%, V_{EE} = 0.0V 3.3V ± 5%, V_{EE} = 0.0V	2.375 3.135	2.625 3.465	V V
V_{CMR}	PECL Input Differential Cross Point Voltage[8]	Differential operation	1.2	V_{CC}	V
V_X	HSTL Input Differential Crosspoint Voltage[9]	Standard Load Differential Operation	0.68	0.9	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[10]	V_{CC} – 1.25	V_{CC} – 0.7	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5% V_{CC} = 2.5V ± 5%	I_{OL} = –5 mA[10]	 V_{CC} – 1.995 V_{CC} –1.995	 V_{CC} – 1.5 V_{CC} – 1.3	 V V
V_{IH}	Input Voltage, High	Single-ended operation	V_{CC} – 1.165	V_{CC} – 0.880[11]	V
V_{IL}	Input Voltage, Low	Single-ended operation	V_{CC} – 1.945[11]	V_{CC} – 1.625	V
V_{BB}[3]	Output Reference Voltage	Relative to V_{CC}[6]	V_{CC} – 1.620	V_{CC} – 1.220	V

Notes:
4. Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1
5. Power Calculation: $V_{CC} * I_{EE} + 0.5 (I_{OH} + I_{OL}) (V_{OH} – V_{OL})$ (number of differential outputs used); I_{EE} does not include current going off chip.
6. where V_{CC} is 3.3V±5% or 2.5V±5%.
7. Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
8. Refer to *Figure 1*.
9. V_X(AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X(AC) range and the input swing lies within the V_{DIF}(AC) specification. Violation of V_X(AC) or V_{DIF}(AC) impacts the device propagation delay, device and part-to-part skew. Refer to *Figure 2*.
10. Equivalent to a termination of 50Ω to VTT. $I_{OHMIN}=(V_{OHMIN} – V_{TT})/50$; $I_{OHMAX}=(V_{OHMAX} – V_{TT})/50$; $I_{OLMIN}=(V_{OLMIN} – V_{TT})/50$; $I_{OLMAX}=(V_{OLMAX} – V_{TT})/50$.
11. V_{IL} will operate down to V_{EE}; V_{IH} will operate up to V_{CC}.

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{EE}	Negative Power Supply	–2.5V ± 5%, V_{CC} = 0.0V –3.3V ± 5%, V_{CC} = 0.0V	–2.625 –3.465	–2.375 –3.135	V
V_{CMR}	ECL Input Differential Cross Point Voltage[8]	Differential operation	V_{EE} + 1.2	0V	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[10]	–1.25	–0.7	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5% V_{EE} = –2.5V ± 5%	I_{OL} = –5 mA[10]	 –1.995 –1.995	 –1.5 –1.3	V
V_{IH}	Input Voltage, High	Single-ended operation	–1.165	–0.880[11]	V
V_{IL}	Input Voltage, Low	Single-ended operation	–1.945[11]	–1.625	V
V_{BB}[3]	Output Reference Voltage		–1.620	–1.220	V

AC Electrical Specifications

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{PP}	PECL/ECL Differential Input Voltage[8]	Differential operation	0.1		1.3	V
V_{CMRO}	Output Common Voltage Range (typ.)		V_{CC} – 1.425			V
F_{CLK}	Input Frequency	50% duty cycle Standard load	–		1.5	GHz
T_{PD}	Propagation Delay CLKA or CLKB to Output pair[13]	PECL, ECL < 660 MHz HSTL < 1 GHz	280 280	400 400	650 750	ps ps
V_{DIF}	HSTL Differential Input Voltage[12]	Duty Cycle Standard Load Differential Operation	0.4	–	1.9	V
V_O	Output Voltage (peak-to-peak; see *Figure 2*)	< 1 GHz	0.375	–	–	V
$tsk_{(O)}$	Output-to-output Skew	<660 MHz[13], See *Figure 3*	–	29	50	ps
$tsk_{(PP)}$	Part-to-Part Output Skew[13]		–	95	150	ps
$t_{jit(per)}$	Output Period Jitter (peak)[14]	156.25 MHz[13]	–	7.2	15	ps
$t_{jit(pn)}$	Output RMS Phase Jitter[13, 14] (See *Figure 6*)	156.25 MHz, 3.3V, broadband	–	0.165	–	ps
		156.25 MHz, 3.3V, filtered	–	0.151	–	ps
		312.5 MHz, 3.3V, broadband	–	0.141	–	ps
		312.5 MHz, 3.3V, filtered	–	0.107	–	ps
$tsk_{(P)}$	Output Pulse Skew[15]	660 MHz[13], See *Figure 3*	–	–	50	ps
T_R,T_F	Output Rise/Fall Time (see *Figure 2*)	50% duty cycle Differential 20% to 80%	0.08	–	0.3	ps

Notes:
12. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tkpd and device-to-device skew.
13. 50% duty cycle; standard load; differential operation.
14. Typical jitter measurements are taken at room temperature and nominal voltage. For further information regarding jitter, please refer to the Application note "Understanding Data sheet Jitter Specifications for Cypress Timing Products."
15. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

Timing Definitions

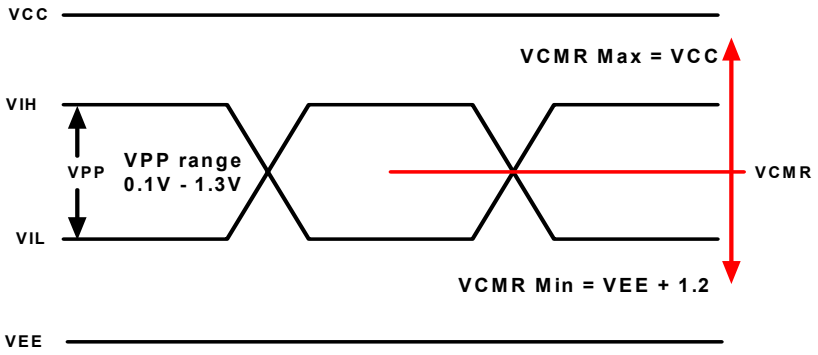


Figure 1. PECL/ECL Input Waveform Definitions

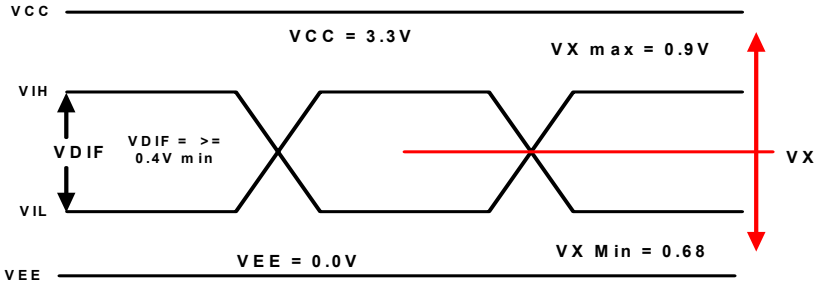


Figure 2. HSTL Differential Input Waveform Definitions

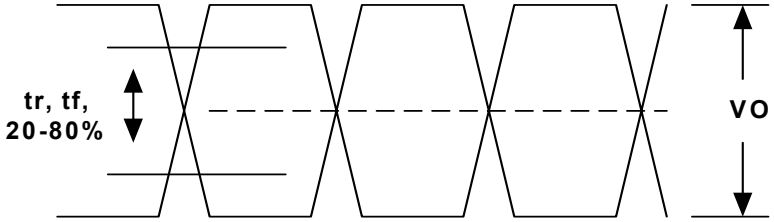


Figure 3. ECL/LVPECL Output

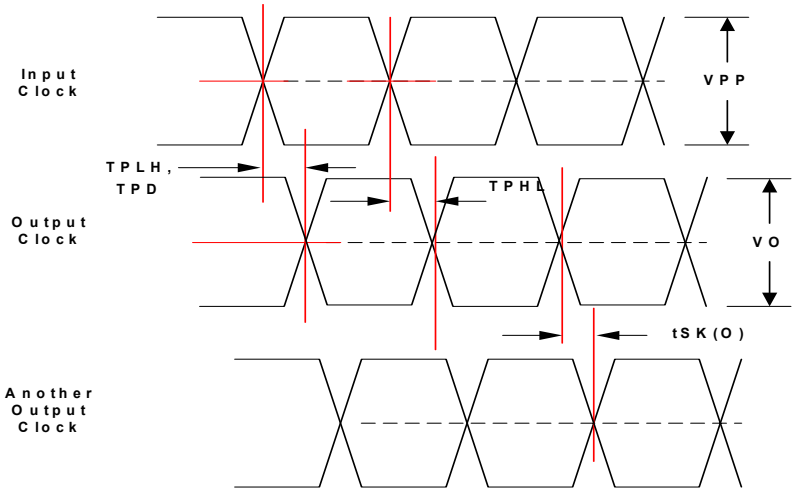


Figure 4. Propagation Delay (T_{PD}), output pulse skew ($|t_{PLH}-t_{PHL}|$), and output-to-output skew ($t_{SK(O)}$) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL

Test Configuration

Standard test load using a differential pulse generator and differential measurement instrument.

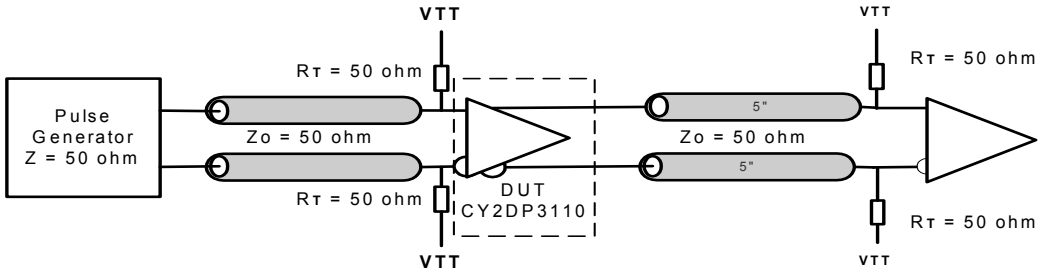


Figure 5. CY2DP3110 AC Test Reference

Supplemental Parametric Information

RMS Phase Jitter: **0.151 ps typical @ 156.25 MHz, 10 GbE Filter (1.875 MHz – 20 MHz)**
0.165 ps typical @ 156.25 MHz, Broadband (Raw Data from 10 Hz – 20 MHz)

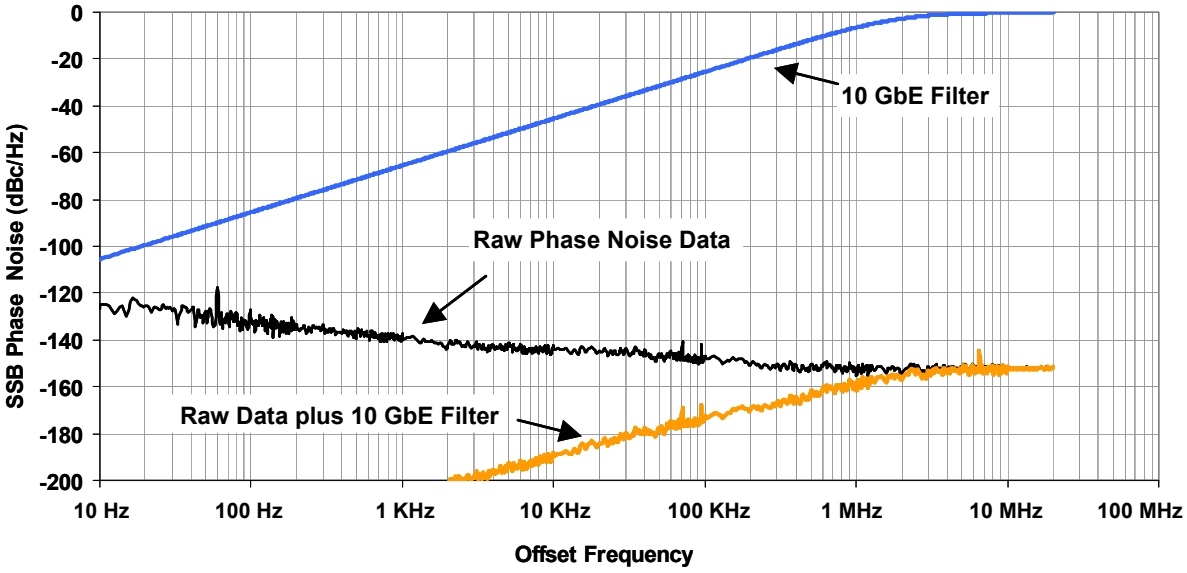


Figure 6. Typical Phase-noise Characteristics at 156.25 MHz, 3.3V, Room Temperature

Applications Information

Termination Examples

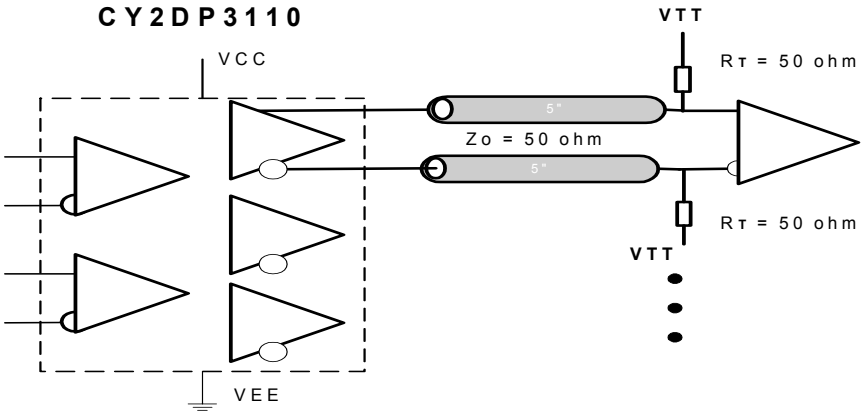


Figure 7. Standard LVPECL – PECL Output Termination

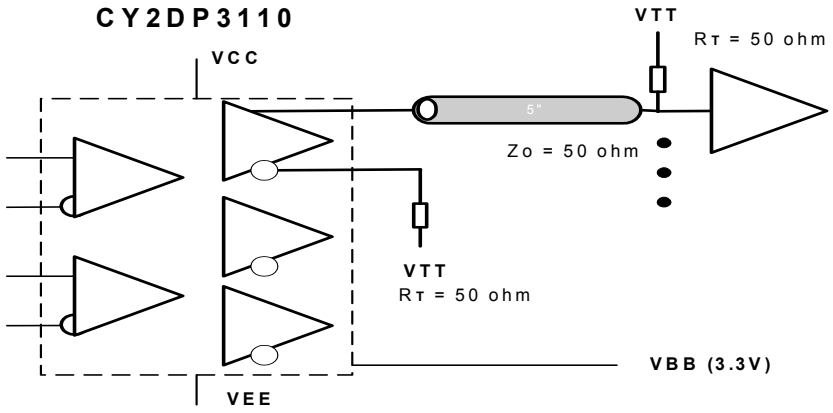


Figure 8. Driving a PECL/ECL Single-ended Input

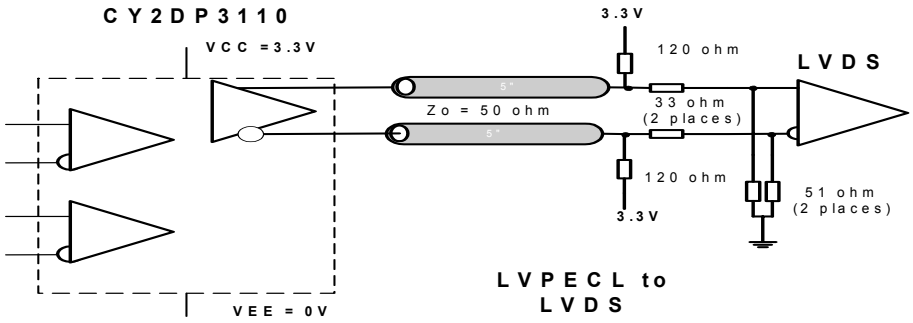
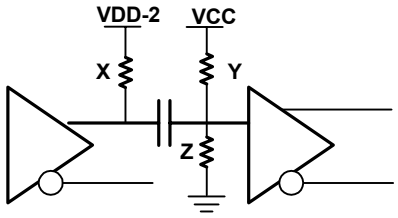


Figure 9. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface



One output is shown for clarity

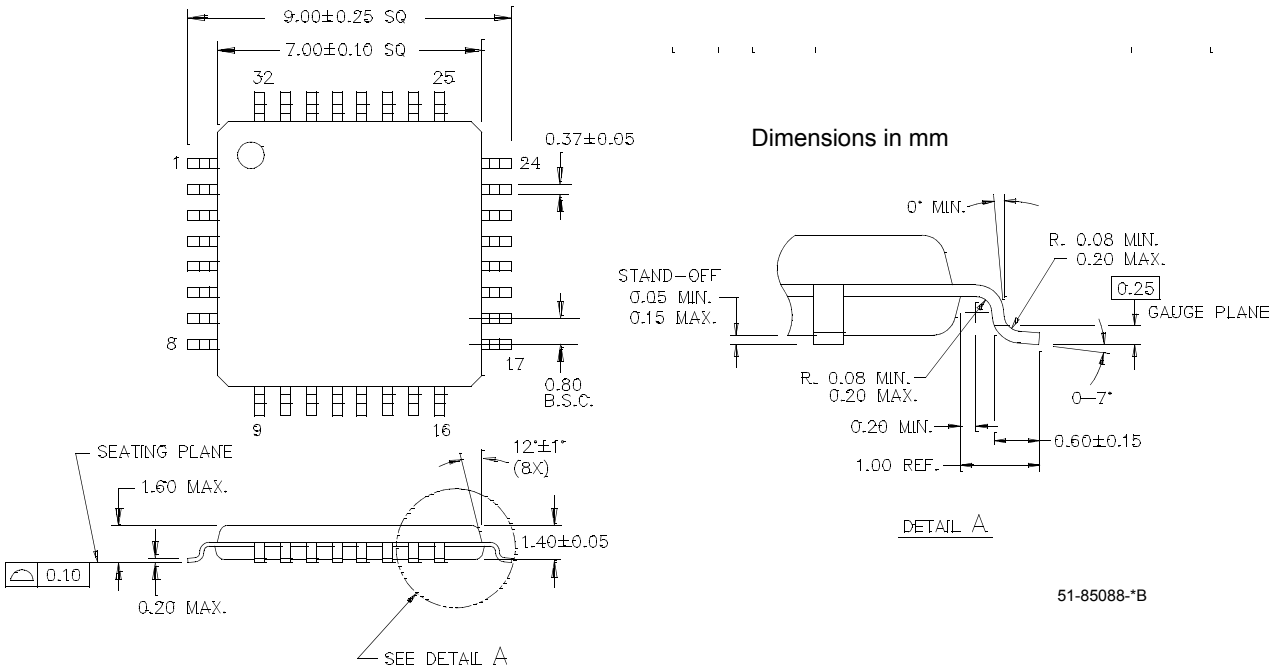
Figure 10. Termination for LVPECL to HTSL interface for VCC=2.5V would use X=50 Ohms, Y=2300 Ohms, and Z=1000 Ohms. See application note titled, “PECL Translation, SAW Oscillators, and Specs” for other signalling standards and supplies.

Ordering Information

Part Number	Package Type	Product Flow
CY2DP3110AI	32-pin TQFP	Industrial, –40° to 85°C
CY2DP3110AIT	32-pin TQFP – Tape and Reel	Industrial, –40° to 85°C
Lead-free		
CY2DP3110AXI	32-pin TQFP	Industrial, –40° to 85°C
CY2DP3110AXIT	32-pin TQFP – Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14



Document History Page

Document Title: CY2DP3110 FastEdge™ Series 1 of 2:10 Differential Clock/Data Fanout Buffer Document Number: 38-07469				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	121284	11/12/02	RGL	New Data Sheet
*A	126251	04/15/03	RGL	Added VBB in the block diagram Corrected specs that does not match EROS/IROS Changed V_{OHMIN} in PECL Output table to V_{CC}-1.2V Shifted table on ECL levels to match PECL Added power-up requirements to absolute maximum conditions Changed title (ComLink to FastEdge)
*B	127696	06/12/03	RGL	Changed operation value from 3.0 GHz to 1.5 GHz in features Modified Note 21: reduced swing value from up to 3 GHz to 2.2 GHz
*C	128731	08/04/03	RGL	Specified TTB value from TBD to 250 ps Specified Vo (pp) values from TBDs to 0.34 ps(min) at < 1.5 GHz, 0.30 ps (typ) at 2.2 GHz Changed Jitter value from 10 ps to 1 ps (intrinsic)
*D	130299	11/19/03	RGL	Corrected the “VCCO” to “VCC” in the Pin Configuration diagram.
*E	227708	See ECN	RGL/GGK	Changed the max. Dissipation, Junction to ambient from 100 to 70°C/W Added Junction Temperature(T_J) parameter of 150°C max Replaced I_{CC} calculation with power calculation in the footnote
*F	229393	See ECN	RGL/GGK	Provided data for TBD’s to match the device
*G	247626	See ECN	RGL/GGK	Changed V_{OH} and V_{OL} to match the Char Data
*H	381816	See ECN	RGL/GGK	Added Phase-noise information; Added typical information Added Lead-free devices
*I	392887	See ECN	RGL/GGK	Changed typical values for Output RMS Phase Jitter