SY89874AU

2.5 GHz, Any-In to LVPECL, Programmable Clock Divider/Fanout Buffer with Internal Termination

Features

- Integrated Programmable Clock Divider and 1:2 Fanout Buffer
- Guaranteed AC Performance over Temperature and Voltage:
  - >2.5 GHz f_{MAX}
  - <250 ps t_r/t_f
  - <5 ps Within-Device Skew
- Low-Jitter Design:
  - <10 ps_{PP} Total Jitter
  - <1 ps_{RMS} Cycle-to-Cycle Jitter
- Unique Input Termination and VT Pin for DC-Coupled and AC-Coupled Inputs; LVCMOS, LVTTL, CML, PECL, LVDS, and HSTL
- TTL/CMOS Inputs for Select and Reset
- 100k EP-Compatible LVPECL Outputs
- Parallel Programming Capability
- Programmable Divider Ratios of 1, 2, 4, 8, and 16
- Low Voltage Operation 2.5V or 3.3V
- Output Disable Function
- –40°C to +85°C Temperature Range
- Available in 16-Pin (3 mm x 3 mm) QFN Package

Applications

- SONET/SDH Line Cards
- Transponders
- High-End Multiprocessor Sensors

General Description

This low-skew, low-jitter device can accept a high-speed (622 MHz or higher) LVTTL, LVCMOS, CML, LVPECL, LVDS, or HSTL clock input signal and divide down the frequency using a programmable divider ratio to create a frequency-locked, lower speed version of the input clock. Available divider ratios are 2, 4, 8, and 16, or straight pass-through. In a typical 622 MHz clock system this would provide availability of 311 MHz, 155 MHz, 77 MHz, or 38 MHz auxiliary clock components.

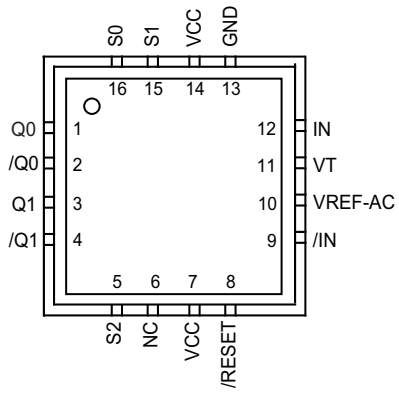
The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

The /RESET input asynchronously resets the divider. In the pass-through function (divide by 1) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN).

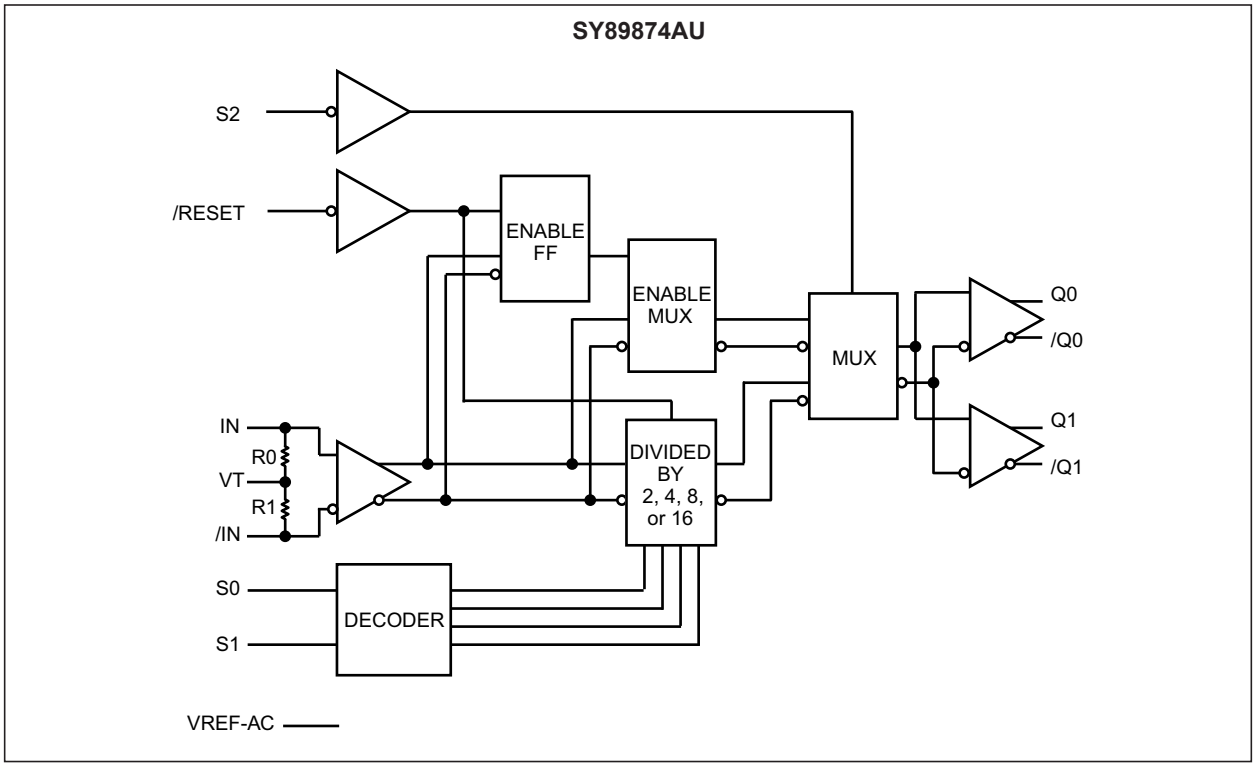
Use the SY89874U version, which has a wider input range, to DC-couple low offset differential signals.

Package Type

SY89874AU
3 mm x 3 mm QFN
(Top View)



Functional Block Diagram



Truth Table

TABLE 0-1: TRUTH TABLE

/RESET	S2	S1	S0	Outputs
1	0	X	X	Reference clock (pass through)
1	1	0	0	Reference clock ÷ 2
1	1	0	1	Reference clock ÷ 4
1	1	1	0	Reference clock ÷ 8
1	1	1	1	Reference clock ÷ 16
0	1	X	X	Q = Low, /Q = High, Clock disable

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}+0.3V
ECL Output Current (I_{OUT})
Continuous ..... 50 mA
Surge ..... 100 mA
Input Current IN, /IN (I_{IN}) ..... ±50 mA
VT Current (I_{VT}) ..... ±100 mA
VREF-AC Sink/Source Current ($I_{VREF-AC}$) (Note 1) ..... ±2 mA

Operating Ratings ‡

Supply Voltage (V_{CC}) ..... 3.3V ±10% or 2.5V ±5%

† Notice: Permanent device damage can occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C unless otherwise noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply	V_{CC}	2.375	—	3.63	V	—
Power Supply Current	I_{CC}	—	50	75	mA	No load, maximum V_{CC}
Differential Input Resistance (IN-to-/IN)	R_{IN}	90	100	110	Ω	—
Input High Voltage (IN, /IN)	V_{IH}	0.8	—	V_{CC} + 0.3	V	Note 2
Input Low Voltage (IN, /IN)	V_{IL}	–0.3	—	V_{IH} – 0.1	V	Note 2
Input Voltage Swing	V_{IN}	0.1	—	V_{CC}	V	Note 2, Note 3
Differential Input Voltage Swing	V_{DIFF_IN}	0.2	—	—	V	Note 2, Note 4
Input Current (IN, /IN)	$\|I_{IN}\|$	—	—	45	mA	Note 2
Reference Voltage	V_{REF-AC}	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V	Note 5

Note 1: The circuit is designed to meet the DC specifications in this table after thermal equilibrium has been established. For a wider input range, use the SY89874U device.

2: Due to the internal termination (see the Input Buffer Structure), the input current depends on the applied voltages at the IN, /IN, and VT inputs. Do not apply a combination of voltages that cause the input current to exceed the maximum limit.

3: See the Timing Diagram or Definition of Single-Ended and Differential Swing sections for V_{IN} definition. V_{IN} (maximum) is specified when VT is floating.

4: See the Definition of Single-Ended and Differential Swing section for V_{DIFF} definition.

5: Operation using V_{REF-AC} is limited to AC-coupled PECL or CML applications only. Connect directly to the VT pin.

LVPECL (100KEP) DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50Ω to V_{CC} – 2V unless otherwise stated. Note 1.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	V_{CC} – 1.145	V_{CC} – 1.020	V_{CC} – 0.895	V	—
Output Low Voltage	V_{OL}	V_{CC} – 1.945	V_{CC} – 1.820	V_{CC} – 1.695	V	—
Output Voltage Swing	V_{OUT}	550	800	1050	mV	—
Differential Output Voltage Swing	V_{DIFF_OUT}	1.10	1.60	2.10	V	—

Note 1: The circuit is designed to meet the DC specifications shown in this table after thermal equilibrium has been established. For a wider differential input range, use the SY89874U device.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C unless otherwise stated. Note 1.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input High Current	I_{IH}	–125	—	20	µA	—
Input Low Current	I_{IL}	–300	—	—	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in this table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C unless otherwise stated. Note 1, Note 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Maximum Output Toggle Frequency	f_{MAX}	2.5	—	—	GHz	Output Swing ≥ 400 mV
Maximum Input Frequency		3.2	—	—		Divide by 2, 4, 8, 16
Differential Propagation Delay, IN-to-Q	t_{PD}	510	620	760	ps	Input Swing < 400 mV
		450	570	700		Input Swing ≥ 400 mV
Within-Device Skew (Differential) Q0 - Q1	t_{SKEW}	—	7	15	ps	Note 3
Part-to-Part Skew (Differential)		—	—	250		Note 3
Reset Recovery Time	t_{RR}	600	—	—	ps	Note 4
Cycle-to-Cycle Jitter	t_{JITTER}	—	—	1	ps_{RMS}	Note 5
Total Jitter		—	—	10	ps_{PP}	Note 6
Rise/Fall Time (20% to 80%)	t_r/t_f	70	150	250	ps	—

Note 1: Specification for packaged product only.

2: Measured with 400 mV input signal, 50% duty cycle, all outputs loaded with 50Ω to V_{CC} − 2V, unless otherwise stated.

3: Skew is measured between outputs under identical transitions.

4: See the “Timing Diagram” section.

5: Cycle-to-cycle Jitter Definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = t_n - t_{n+1}$, where t is the time between rising edges of the output signal.

6: Total Jitter Definition: With an ideal clock input, of frequency ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Ambient Operating Temperature	T_A	–40	—	+85	°C	—
Storage Temperature	T_A	–65	—	+150	°C	—
Maximum Junction Temperature	T_J	—	—	+125	°C	—
Package Thermal Resistance						
Thermal Resistance, QFN 16-Ld	θ_{JA}	—	60	—	°C/W	Still-Air
	θ_{JA}	—	54	—	°C/W	500 lfpm
	Ψ_{JB}	—	32	—	°C/W	Junction-to-board, Note 2

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: Junction-to-board resistance assumes that the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 3.3V, V_{IN} = 400 mV, T_A = +25°C, unless otherwise stated.

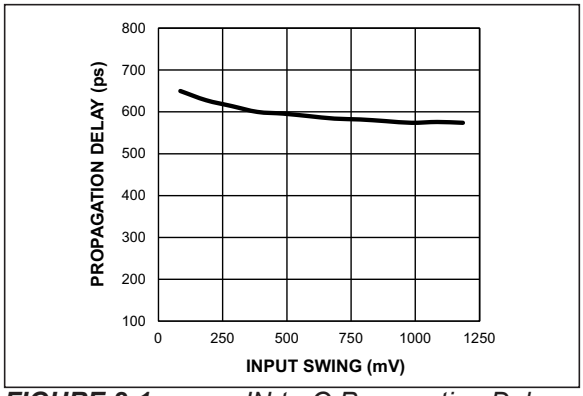


FIGURE 2-1: *IN-to-Q Propagation Delay vs. Input Swing.*

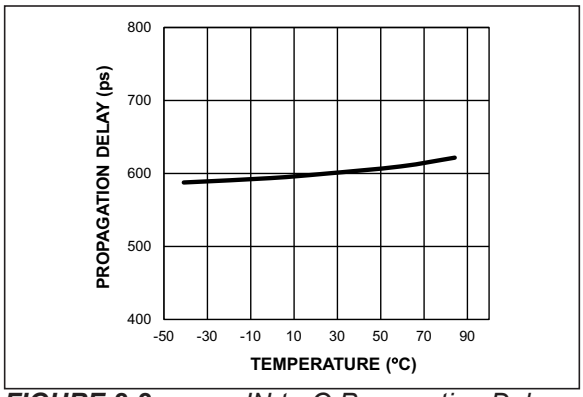


FIGURE 2-2: *IN-to-Q Propagation Delay vs. Temperature.*

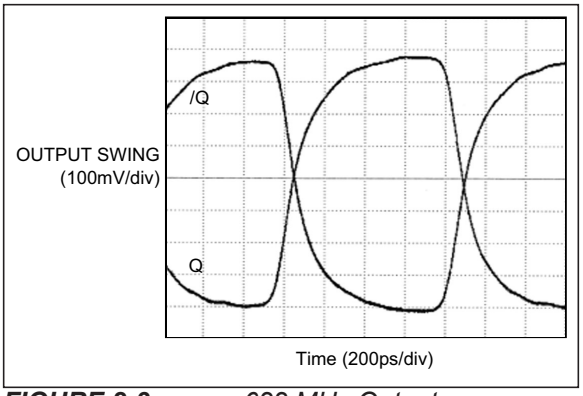


FIGURE 2-3: *622 MHz Output.*

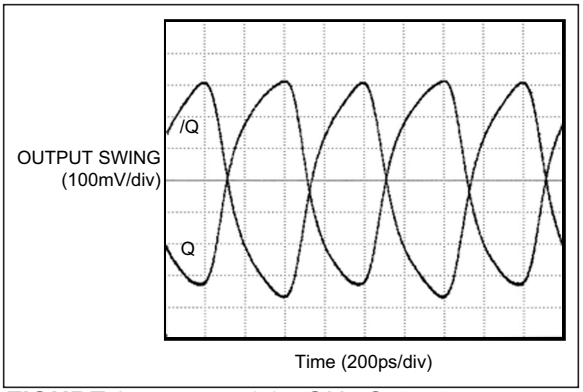


FIGURE 2-4: *1.25 GHz Output.*

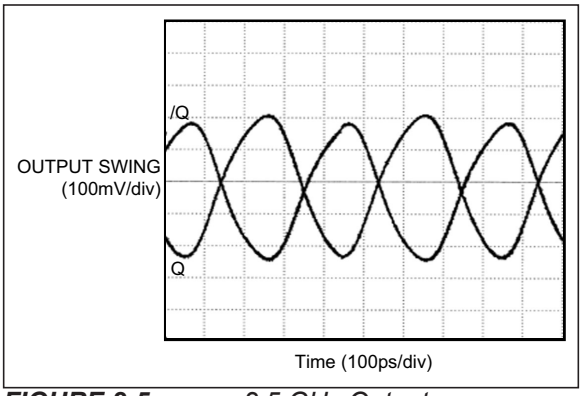
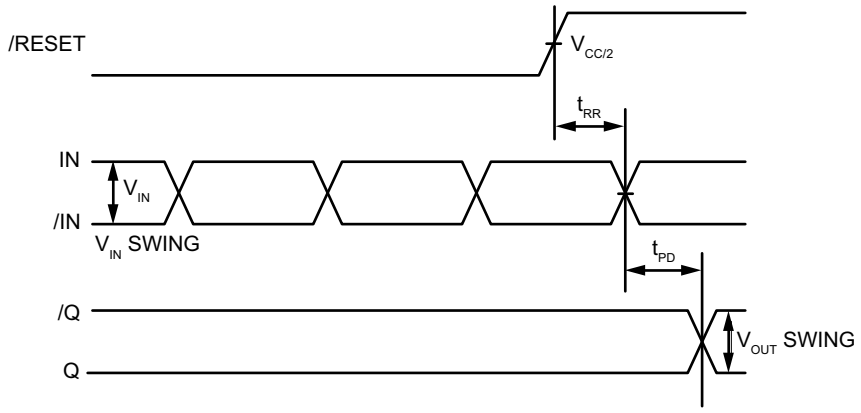
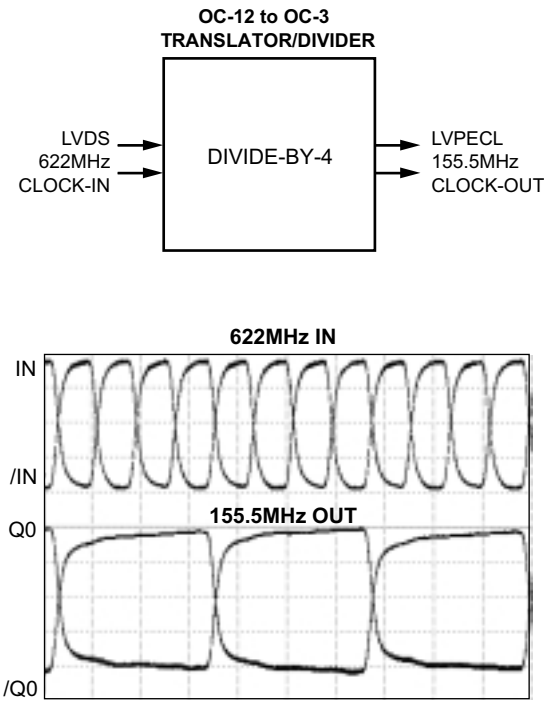


FIGURE 2-5: *2.5 GHz Output.*

Timing Diagram



Typical Performance



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2, 3, 4	Q0, /Q0 Q1, /Q1	Differential Buffered LVPECL Outputs. Divided by 1, 2, 4, 8, or 16. See the Truth Table. Unused PECL outputs may be left floating with no impact on jitter performance.
16, 15, 5	S0, S1, S2	Select Pins. See the Truth Table. LVTTL/CMOS logic levels. Internal 25 kΩ pull-up resistor. Logic high if left unconnected (divided by 16 mode). Input threshold is $V_{CC}/2$.
6	NC	No connect.
7, 14	VCC	Positive Power Supply. Bypass with 0.1 µF/0.01 µF low-ESR capacitor.
8	/RESET /DISABLE	LVTTL/CMOS Logic Levels. Internal 25 kΩ pull-up resistor. Logic high if left unconnected. Apply low to reset the divider (divided by 2, 4, 8, or 16 mode). Also acts as a synchronous disable/enable function. The reset and disable function occurs on the next high-to-low clock input transition. Input threshold is $V_{CC}/2$.
12, 9	IN, /IN	Input. Internal 50Ω termination resistors to VT input. Flexible input accepts any input. See the “Input Interface Applications” section.
10	VREF-AC	Reference Voltage. Equal to V_{CC} – 1.4V (approximately). Used for AC-coupled applications only. Decouple the VREF-AC pin with a 0.01 µF capacitor. See the “Input Interface Applications” section.
11	VT	Termination Center Tap. For CML or LVDS inputs, leave this floating. Otherwise, see the figures in the “Input Interface Applications” section.
13	GND	Ground.

4.0 DIAGRAMS

4.1 Definition of Single-Ended and Differential Swing

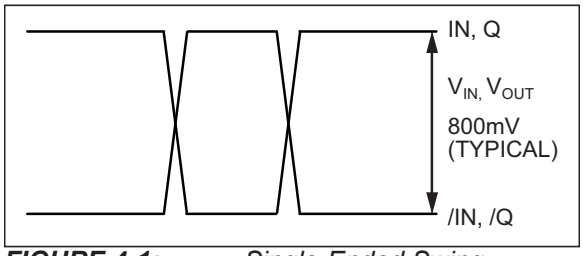


FIGURE 4-1: *Single-Ended Swing.*

Single-ended swing is the amplitude of the signal when driven differentially.

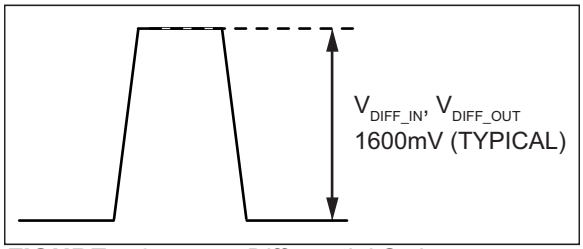


FIGURE 4-2: *Differential Swing.*

Differential swing is defined as IN – /IN (or Q – /Q).

4.2 Input Buffer Structure

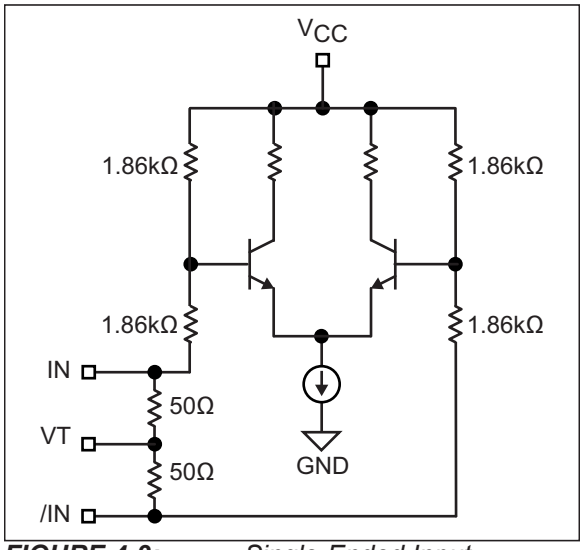


FIGURE 4-3: *Single-Ended Input Structure.*

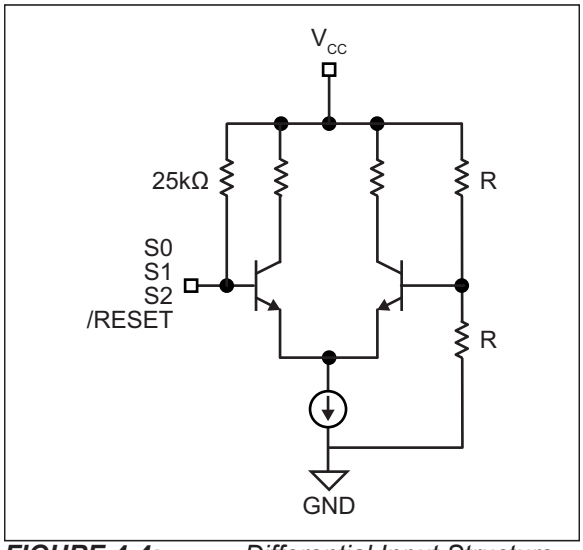


FIGURE 4-4: *Differential Input Structure.*

5.0 DIFFERENTIAL INPUT INTERFACE APPLICATIONS

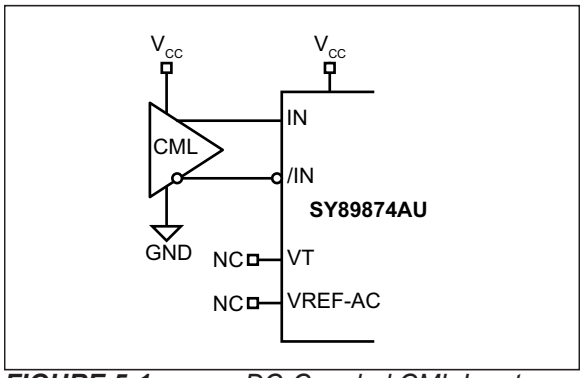


FIGURE 5-1: *DC-Coupled CML Input Interface.*

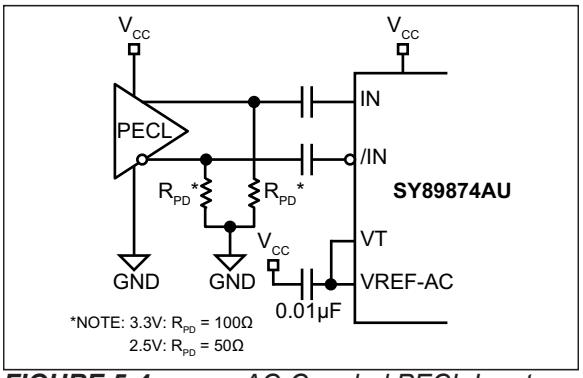


FIGURE 5-4: *AC-Coupled PECL Input Interface.*

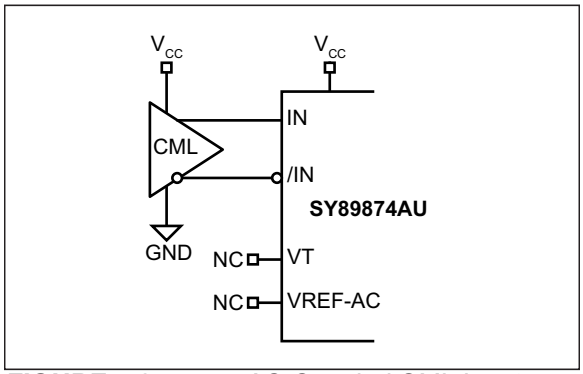


FIGURE 5-2: *AC-Coupled CML Input Interface.*

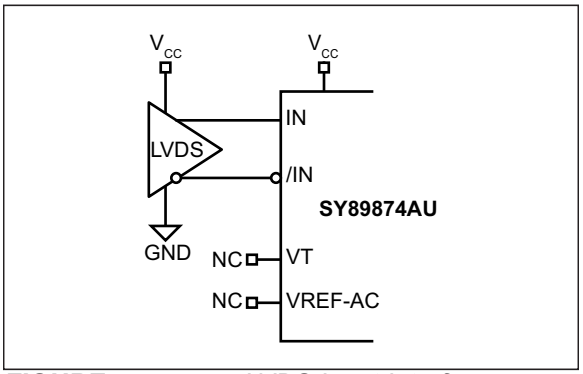


FIGURE 5-5: *LVDS Input Interface.*

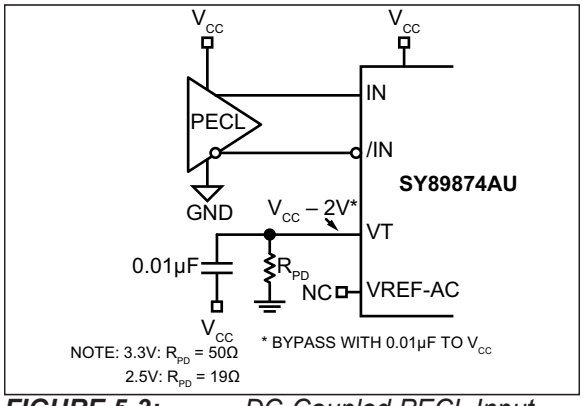


FIGURE 5-3: *DC-Coupled PECL Input Interface.*

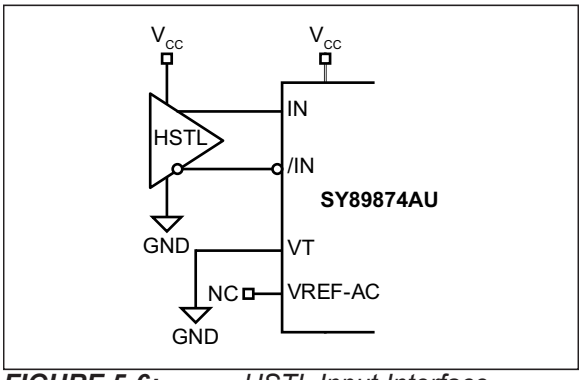


FIGURE 5-6: *HSTL Input Interface.*

6.0 SINGLE-ENDED INPUT INTERFACE APPLICATIONS

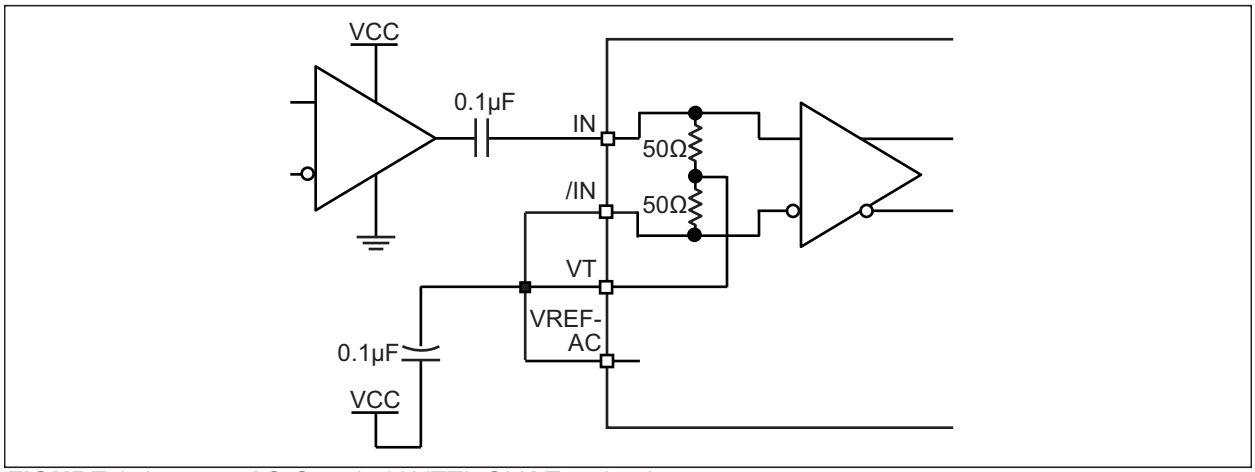


FIGURE 6-1: *AC-Coupled LVTTL CLK Termination.*

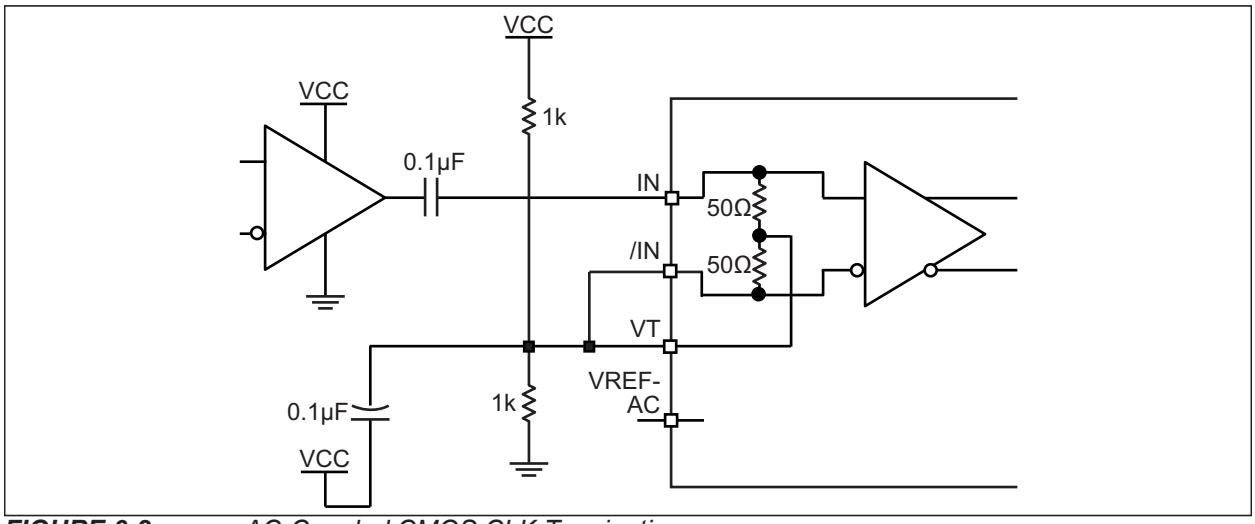


FIGURE 6-2: *AC-Coupled CMOS CLK Termination.*

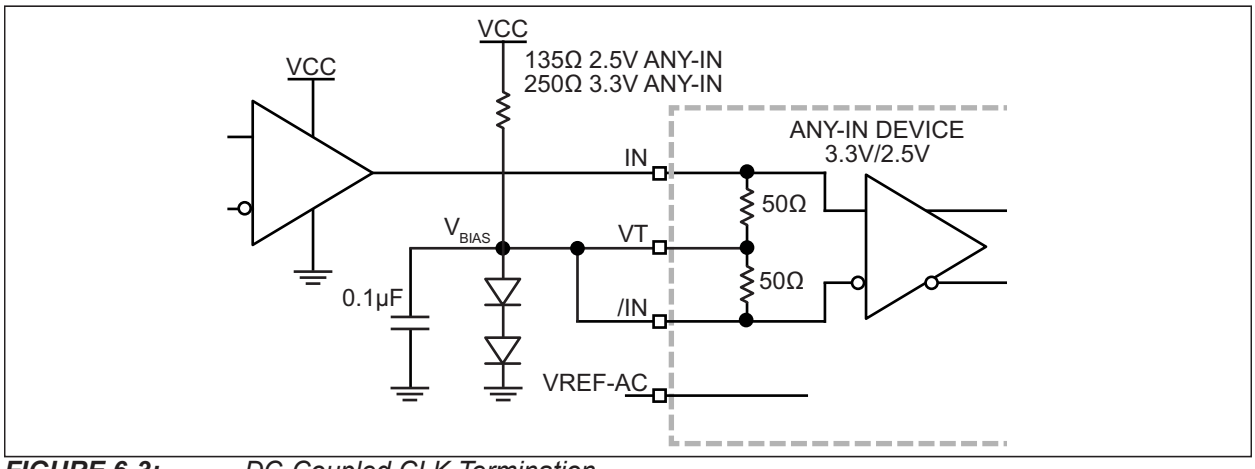


FIGURE 6-3: *DC-Coupled CLK Termination.*

7.0 LVPECL OUTPUT TERMINATION RECOMMENDATIONS

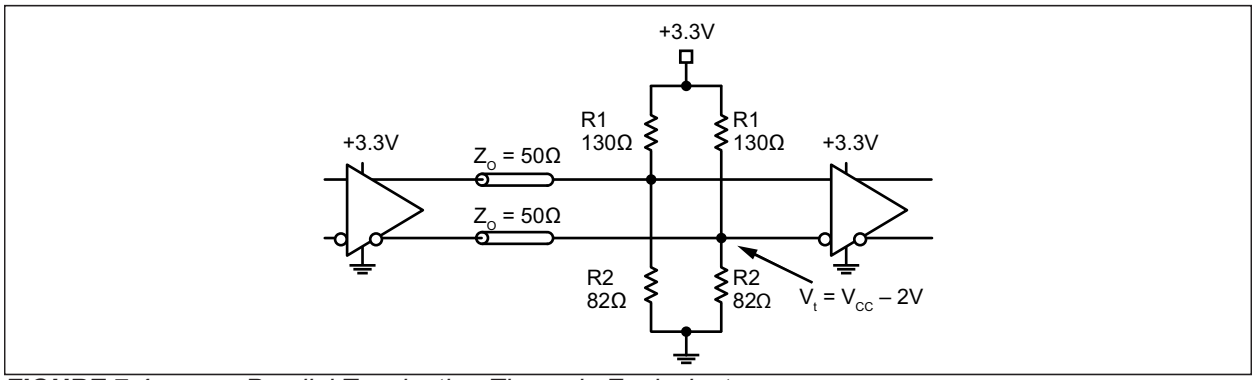


FIGURE 7-1: *Parallel Termination-Thevenin Equivalent.*

Note: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

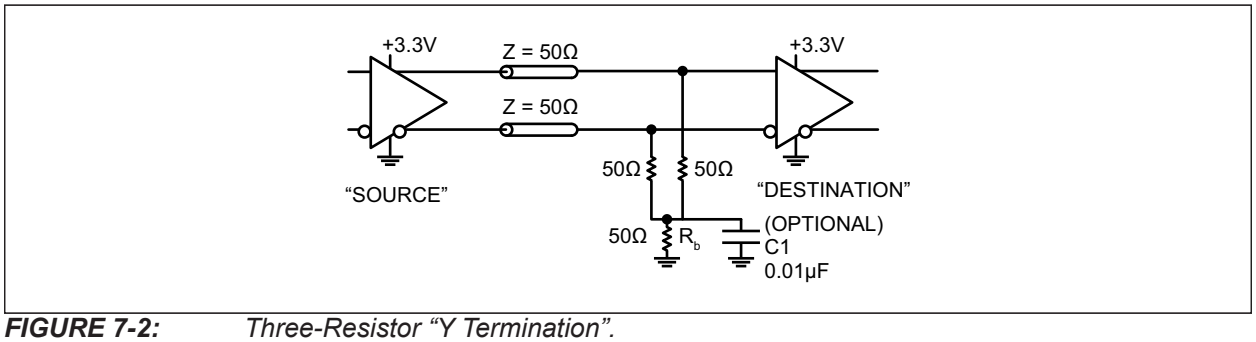


FIGURE 7-2: *Three-Resistor "Y Termination".*

Note 1: Power-saving alternative to Thevenin termination.

2: Place termination resistors as close to destination inputs as possible.

3: The R_b resistor sets the DC bias voltage, equal to V_T. For +3.3V systems: R_b = 46Ω to 50Ω. For +2.5V systems: R_b = 19Ω.

4: C1 is an optional bypass capacitor that compensates for any t_r/t_f mismatches.

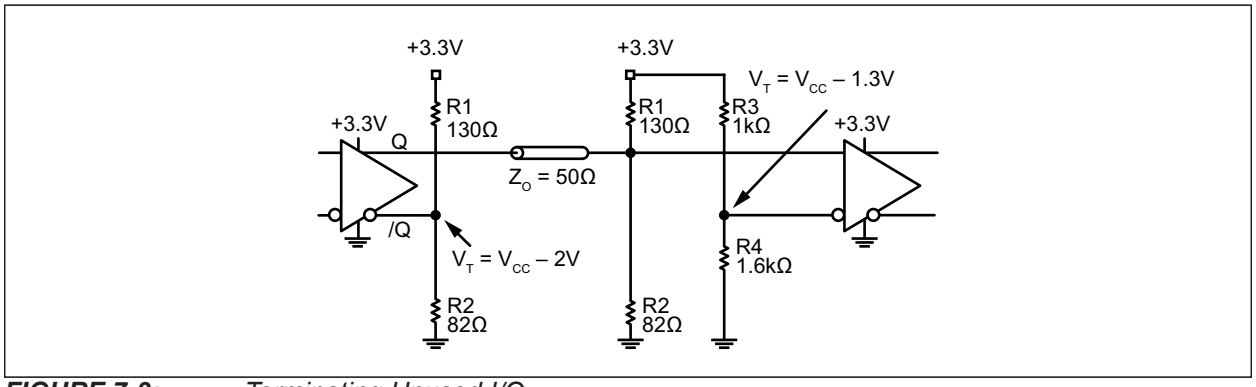


FIGURE 7-3: *Terminating Unused I/O.*

Note 1: Unused output (/Q) must be terminated to balance the output.

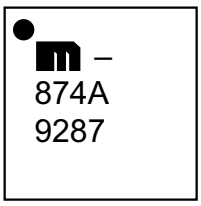
2: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25 kΩ, R4 = 1.2 kΩ.

8.0 PACKAGING INFORMATION

8.1 Package Marking Information

16-Lead QFN*

Example



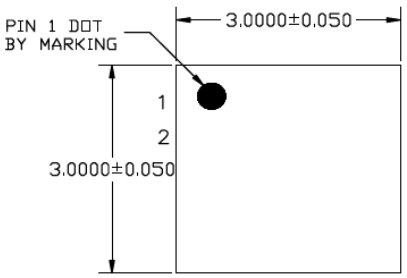
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

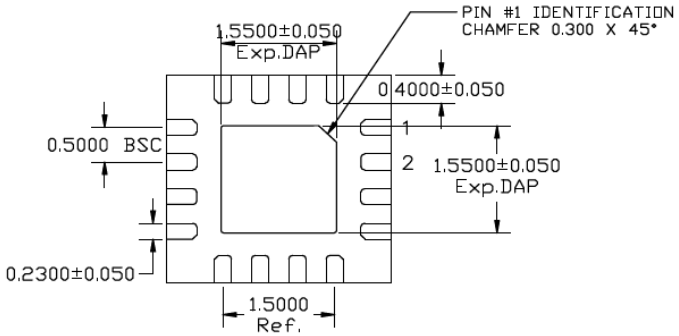
Underbar (_) and/or Overbar (‾) symbol may not be to scale.

TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

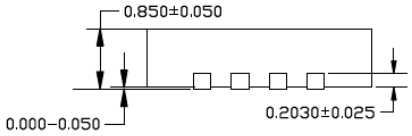
DRAWING #	QFN33-16LD-PL-1	UNIT	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3

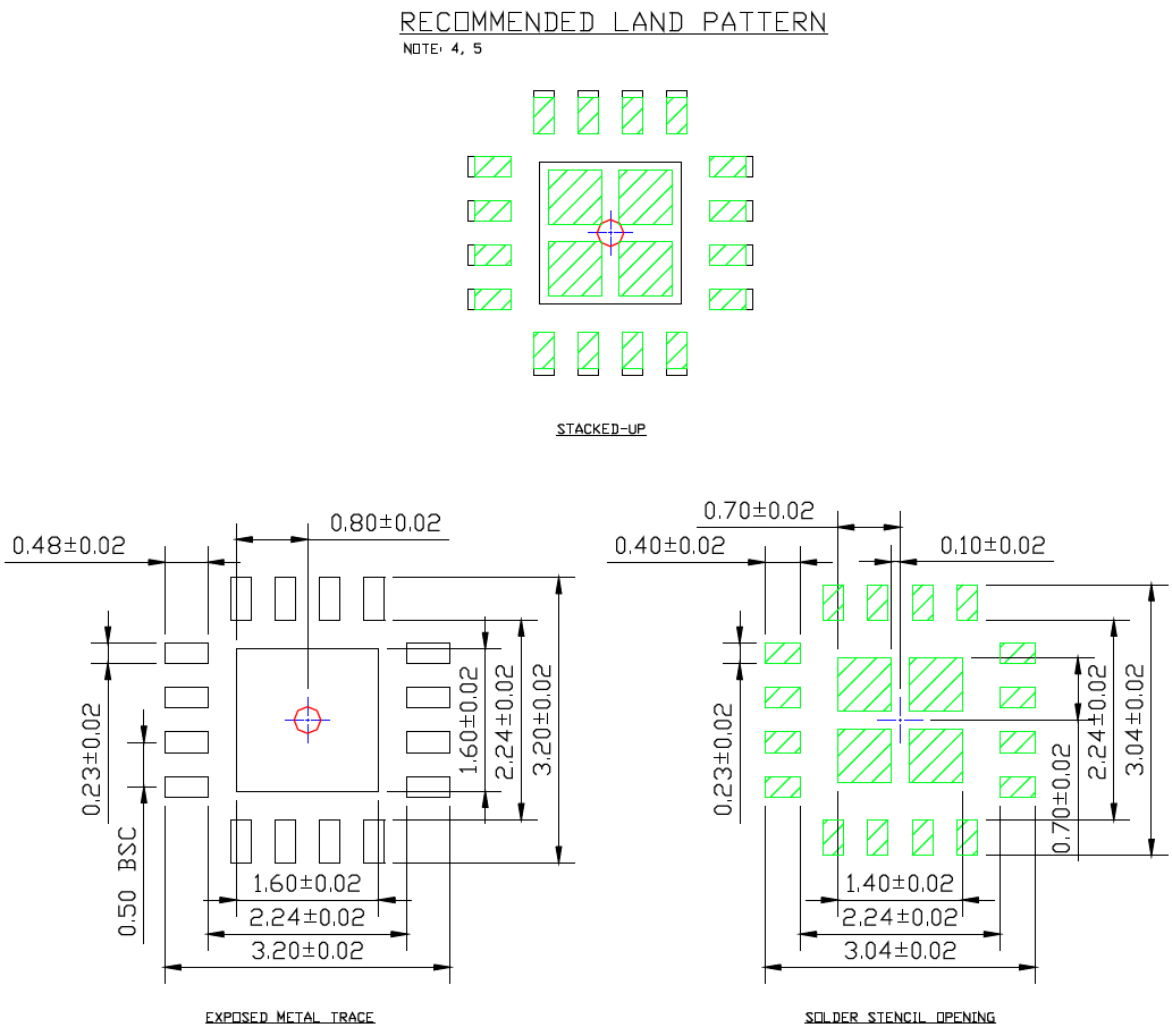


SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern drawing # QFN33-16LD-PL-1



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2019)

- Converted Micrel document SY89874AU to Microchip data sheet DS20006200A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	-XX
Device	Supply Voltage	Package	Temp. Range	Packing

Device:	SY89874A:		2.5 GHz, Any-In to LVPECL, Programmable Clock Divider/Fanout Buffer with Internal Termination
Supply Voltage:	U	=	2.5V/3.3V
Package:	M	=	16-Lead 3 mm x 3 mm QFN
Temperature Range:	G	=	–40°C to +85°C (NiPdAu Lead-Free)
Tape and Reel:	<blank>	=	110/Tube
	TR	=	1,000/Reel

Examples:

a) SY89874AUMG:
SY89874A, 2.5V/3.3V Supply Voltage,
16-Lead QFN, –40°C to +85°C Temperature Range,
110/Tube

b) SY89874AUMG-TR:
SY89874A, 2.5V/3.3V Supply Voltage,
16-Lead QFN, –40°C to +85°C Temperature Range,
1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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