A Product Line of
Diodes Incorporated

PI6CBE33085

Low-Power 8-Output ZDB / Fanout Clock Buffer for PCIe 5.0 and UPI

Features

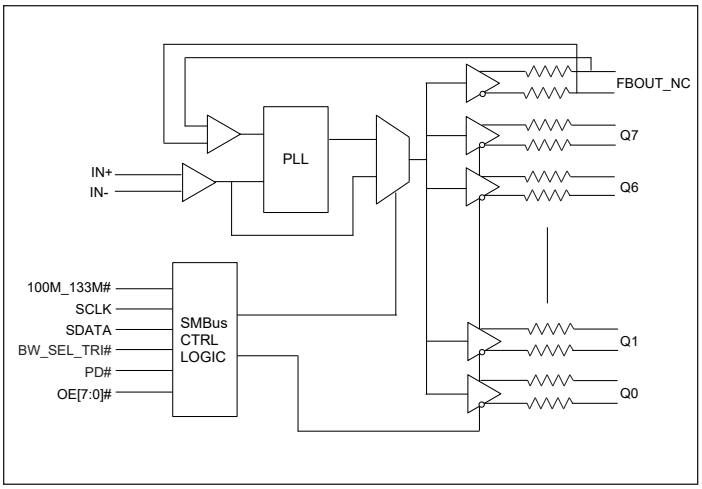
- Eight Differential Low-Power HCSL Outputs with On-Chip Termination
- Default Z_{OUT} = 85Ω
- Spread Spectrum Tolerant
- Individual Output Enable
- Selectable PLL Bandwidths
- Hardware/SMBus Control of ZDB and Fanout Buffer Modes
- 1 to 400MHz Fanout Buffer Operation
- 100MHz and 133.33MHz ZDB Mode
- Differential Output-to-output Skew <50ps
- Very Low Jitter Outputs
  - Differential Cycle-to-cycle Jitter <50ps
  - Fanout Buffer Mode Additive Phase Jitter:
    - PCIe® 5.0 CC: 17fs RMS typ
    - DB2000Q Additive Jitter: 28fs RMS typ
    - QPI/UPI 11.4GB/s: 20fs RMS typ
    - IF-UPI Additive Jitter: 60fs RMS typ
  - ZDB Mode Phase Jitter:
    - PCIe 5.0 CC: 18fs RMS typ
    - QPI/UPI 11.4GB/s: 80fs RMS typ
    - IF-UPI Additive Jitter: 60fs RMS typ
- 3.3V Core Supply Voltage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 48-TQFN, 6×6mm (ZL)

Description

The DIODES™ PI6CBE33085 is a low-power PCIe 1.0/2.0/3.0/4.0/5.0 clock buffer. It takes a reference input to fanout eight 100MHz low-power differential HCSL outputs with on-chip terminations for 85Ω output impedance. It supports both zero-delay and fanout buffer functions for various applications. An individual OE pin for each output provides easier power management.

It uses Diodes proprietary PLL design to achieve very-low jitter that meets PCIe 1.0/2.0/3.0/4.0/5.0 requirements. Other than PCIe 100MHz support, this device also supports 133.33MHz via a pin.

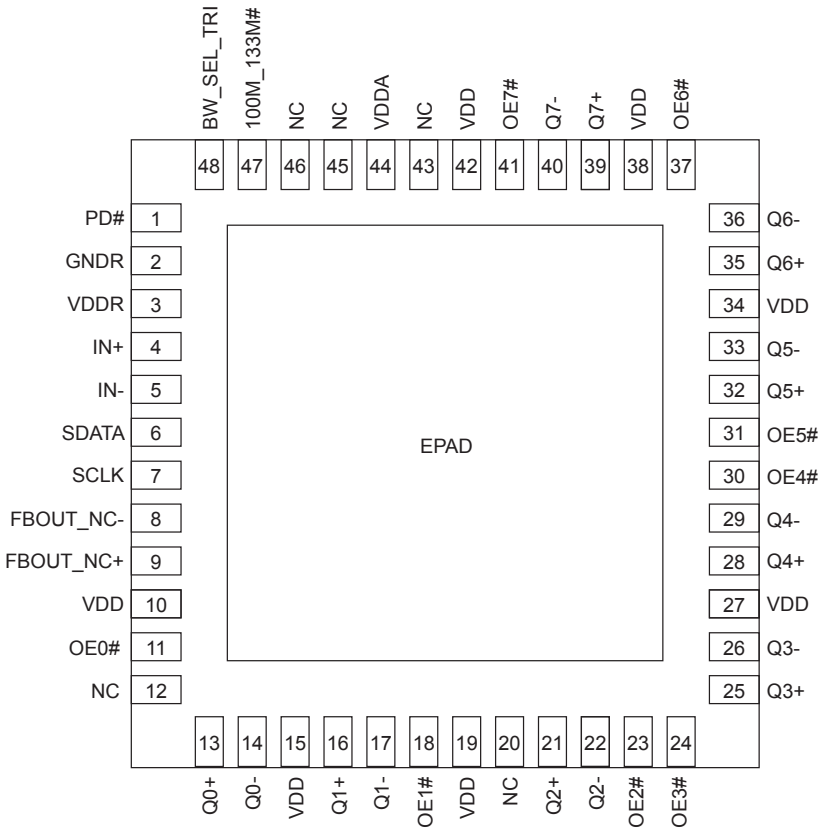
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin Number	Pin Name	Type		Description
1	PD#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode; subsequent high assertions exit Power Down Mode. This pin has internal pullup resistor.
2	GNDR	Power	—	Analog ground for receiver
3	VDDR	Power	—	Analog VDD for receiver
4	IN+	Input	HCSL	Differential true clock input
5	IN-	Input	HCSL	Differential complementary clock input
6	SDATA	Input/ Output	CMOS	SMBUS Data line, 3.3V tolerant
7	SCLK	Input	CMOS	SMBUS clock input, 3.3V tolerant
8	FBOUT_NC-	—	—	Complementary differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get zero propagation delay.

Pin Description Cont.

Pin Number	Pin Name	Type		Description
9	FBOUT_NC+	—	—	True differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get zero propagation delay.
10, 15, 19, 27, 34, 38, 42	V_{DD}	Power	—	Power supply, nominal 3.3V
11	OE0#	Input	CMOS	Active low input for enabling Q0 pair. This pin has an internal pulldown. 1 =disable outputs, 0 = enable outputs
12, 20, 43, 45, 46	NC	—	—	Do not connect this pin.
13	Q0+	Output	HCSL	Differential true clock output
14	Q0-	Output	HCSL	Differential complementary clock output
16	Q1+	Output	HCSL	Differential true clock output
17	Q1-	Output	HCSL	Differential complementary clock output
18	OE1#	Input	CMOS	Active low input for enabling Q1 pair. This pin has an internal pulldown. 1 =disable outputs, 0 = enable outputs
21	Q2+	Output	HCSL	Differential true clock output
22	Q2-	Output	HCSL	Differential complementary clock output
23	OE2#	Input	CMOS	Active low input for enabling Q2 pair. This pin has an internal pulldown. 1 =disable outputs, 0 = enable outputs
24	OE3#	Input	CMOS	Active low input for enabling Q3 pair. This pin has an internal pulldown. 1 =disable outputs, 0 = enable outputs
25	Q3+	Output	HCSL	Differential true clock output
26	Q3-	Output	HCSL	Differential complementary clock output
28	Q4+	Output	HCSL	Differential true clock output
29	Q4-	Output	HCSL	Differential complementary clock output
30	OE4#	Input	CMOS	Active low input for enabling Q4 pair. This pin has an internal pulldown. 1 =disable outputs, 0 = enable outputs
31	OE5#	Input	CMOS	Active low input for enabling Q5 pair. This pin has an internal pulldown. 1 =disable outputs, 0 = enable outputs
32	Q5+	Output	HCSL	Differential true clock output
33	Q5-	Output	HCSL	Differential complementary clock output
35	Q6+	Output	HCSL	Differential true clock output
36	Q6-	Output	HCSL	Differential complementary clock output
37	OE6#	Input	CMOS	Active low input for enabling Q6 pair. This pin has an internal pulldown. 1 =disable outputs, 0 = enable outputs
39	Q7+	Output	HCSL	Differential true clock output
41	OE7#	Input	CMOS	Active low input for enabling Q7 pair. This pin has an internal pulldown. 1 =disable outputs, 0 = enable outputs

Pin Description Cont.

Pin Number	Pin Name	Type		Description
40	Q7-	Output	HCSL	Differential complementary clock output
44	VDDA	Power	—	Analog VDD
47	100M_133M#	Input	CMOS	Latch to select frequency. This pin has internal pullup resistor. See Frequency Select Table
48	BW_SEL_TRI	Input	Tri-level	Latch to select low-loop bandwidth, bypass PLL, and high-loop bandwidth. This pin has internal pullup resistor
EPAD	EPAD	Power	—	Connect to ground

Power Management Table

PD#	IN	SMBus OE bit	OEn#	Qn+	Qn-	PLL Status
0	X	X	X	Low	Low	Off
1	Running	0	X	Low	Low	On(1)
1	Running	1	0	Running	Running	On(1)
1	Running	1	1	Low	Low	On(1)

Note:
1. If PLL Bypass mode is selected, the PLL will be off and outputs will be running.

PLL Operating Mode Select Table

PLL_OM	Operating Mode	PLL
0	PLL with Low Bandwidth	Running
M	PLL Bypass	off
1	PLL with High Bandwidth	Running

Frequency Select Table

100M_133M#	IN (MHz)	Qn (MHz)
0	133.33	133.33
1 (default)	100	100

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx} .....–0.5V to +4.6V
Input Voltage ..... –0.5V to V_{DD} +0.5V, not exceed 4.6V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) 2000V
Junction Temperature .....125°C max

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min..	Typ.	Max.	Units
V_{DD}, V_{DDA}, V_{DDR}	Power Supply Voltage	—	3.135	3.3	3.465	V
I_{DDA}	Analog Power Supply Current	V_{DDA}, PLL mode, All outputs active @ 100MHz	—	21	—	mA
I_{DD}	Power Supply Current	V_{DD} + V_{DD_R}, All outputs active @ 100MHz	—	100	—	mA
I_{DDA_PD}	Analog Power Supply Power Down(1) Current	V_{DDA}, PLL mode, All outputs LOW/LOW	—	0.6	—	mA
I_{DD_PD}	Power Supply Power Down(1) Current	V_{DD} + V_{DD_R}, All outputs LOW/LOW	—	2.5	—	mA
T_A	Ambient Temperature	Industrial grade	–40	—	85	°C

Note:
1. Input clock is not running.
2. Outputs drive 5 inch trace.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal Pullup Resistance	—	—	120	—	KΩ
R_{dn}	Internal Pulldown Resistance	—	—	120	—	KΩ
L_{PIN}	Pin Inductance	—	—	—	7	nH

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal Bus Voltage	—	2.7	—	3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1	—	3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}	—	—	
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V	—	—	0.8	V
		SMBus, V_{DDSMB} < 3.3V	—	—	0.8	
$I_{SMBSINK}$	SMBus Sink Current	SMBus, at V_{OLSMB}	4	—	—	mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$	—	—	0.4	V
f_{MAXSMB}	SMBus Operating Frequency	Maximum frequency	—	—	500	kHz
t_{RMSB}	SMBus Rise Time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)	—	—	1000	ns
t_{FMSB}	SMBus Fall Time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)	—	—	300	ns

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus	0.75 V_{DD}	—	V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	SADR0_TRI, SADR1_TRI, BW_SEL_TRI	0.4V_{DD}	0.5V_{DD}	0.6V_{DD}	V
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus	-0.3	—	0.25 V_{DD}	V
I_{IH}	Input High Current	Single-ended inputs, V_{IN} = V_{DD}	—	—	5	µA
I_{IL}	Input Low Current	Single-ended inputs, V_{IN} = 0V	-5	—	—	µA
I_{IH}	Input High Current	Single-ended inputs with pullup/pulldown resistor, V_{IN} = V_{DD}	—	—	50	µA
I_{IL}	Input Low Current	Single-ended inputs with pullup/pulldown resistor, V_{IN} = 0V	-50	—	—	µA
C_{IN}	Input Capacitance	—	1.5	—	5	pF

LVCMOS AC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{OELAT}	Output Enable Latency	Q start after OE# assertion Q stop after OE# deassertion	4	5	10	clocks
t_{PDLAT}	PD# Deassertion	Differential outputs enable after PD# deassertion	—	20	300	µs

HCSL Input Characteristics(1)

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IHDIF}	Diff. Input High Voltage(3)	IN+, IN-, single-end measurement	600	800	1150	mV
V_{ILDIF}	Diff. Input Low Voltage(3)	IN+, IN-, single-end measurement	-300	0	300	mV
V_{COM}	Diff. Input Common Mode Voltage		150	—	900	mV
V_{SWING}	Diff. Input Swing Voltage	Peak to peak value (V_{IHDIF} - V_{ILDIF})	300	—	2900	mV
f_{INBP}	Input Frequency	PLL Bypass mode	1	—	400	MHz
f_{IN100}	Input Frequency	100MHz PLL	98.5	100	102.5	MHz
f_{IN133}	Input Frequency	133MHz PLL	132	133.33	135	MHz
$f_{MODI-PCIe}$	Input SS Modulation Freq. PCIe	Allowable frequency for PCIe applications (Triangular Modulation)	30	—	33	kHz
t_{STAB}	Clock stabilization	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock	—	0.75	1.0	ms
t_{RF}	Diff. Input Slew Rate(2)	Measured differentially	0.4	—	—	V/ns
I_{IN}	Diff. Input Leakage Current	V_{IN} = V_{DD}, V_{IN} = GND	-5	0.01	5	uA
t_{DC}	Diff. Input Duty Cycle	Measured differentially	45	—	55	%
tj_{c-c}	Diff. Input Cycle to cycle jitter	Measured differentially	—	—	125	ps

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is (V_{IH}-V_{IL})/2

HCSL Output DC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output Voltage High(1)	Statistical measurement on single-ended signal using oscilloscope math function	660	—	850	mV
V_{OL}	Output Voltage Low(1)		-150	—	150	mV
V_{OMAX}	Output Voltage Maximum(1)	Measurement on single ended signal using absolute value	—	—	1150	mV
V_{OMIN}	Output Voltage Minimum(1)		-300	—	—	mV
V_{OC}	Output Cross Voltage(1,2,4)	—	250	—	550	mV
DV_{OC}	V_{OC} Magnitude Change(1,2,5)	—	—	—	140	mV

Note:

1. At default SMBUS amplitude settings.
2. Guaranteed by design and characterization—not 100% tested in production.
3. Measured from differential waveform.
4. This one is defined as voltage where Q+ = Q- measured on a component test board and only applied to the differential rising edge.
5. The total variation of all Vcross measurements in any particular system. This is a subset of Vcross_min/max allowed.

HCSL Output AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency	PLL mode	—	100	133.33	MHz
		PLL bypass mode	—	—	400	MHz
BW	PLL Bandwidth(1,8)	-3dB point in High Bandwidth Mode	—	—	4	MHz
		-3dB point in Low Bandwidth Mode	—	—	1.4	MHz
tj_{peak}	PLL Jitter Peaking	Peak pass band gain, low bandwidth	—	—	2	dB
		Peak pass band gain, high bandwidth		—	2.5	dB
t_{RF}	Slew Rate(1,2,3)	Scope averaging on fast setting	2	—	4.0	V/ns
Dt_{RF}	Slew Rate Matching(1,2,4)	Scope averaging on	—	—	20	%
t_{SKEW}	Output Skew(1,2)	Averaging on, V_T = 50%	—	—	50	ps
t_{PDELAY}	Propagation Delay	PLL Bypass mode, V_T = 50%, across temperature and VDD	2000	—	3000	ps
		PLL Bypass mode, V_T = 50%, norminal temperature and VDD	—	—	2500	ps
		PLL mode, V_T = 50%, norminal temperature and VDD	—	—	50	ps
		PLL mode, V_T = 50%, across temperature and VDD	—	—	100	ps
t_{DC}	Duty Cycle(1,2)	Measured differentially, PLL Mode	45	50	55	%
t_{DCD}	Duty Cycle Distortion(1,7)	Measured differentially, PLL Bypass Mode at 100MHz	-3.5	0	3.5	%
tj_{c-c}	Cycle-to-Cycle Jitter(1,2)	PLL mode	—	14	—	ps
		Additive jitter, Bypass mode	—	0.1	—	ps

HCSL Output AC Characteristics (PLL Mode PCIe Phase Jitter)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
$tj_{PH\_PLL\_CC}$	Integrated Phase Jitter PLL Mode (RMS)(1,5) Low Bandwidth (Common Clocked Architecture)	PCIe 1.0(6)	—	2.6	—	86	ps (p-p)
		PCIe 2.0 Low Band, 10kHz < f < 1.5MHz	—	0.08	—	3.1	ps
		PCIe 2.0 High Band, 1.5MHz < f < Nyquist (50MHz)	—	0.09	—	3	ps
		PCIe 3.0 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	—	0.05	—	1	ps
		PCIe 4.0 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	—	0.05	—	0.5	ps
		PCIe 5.0(11) (PLL BW of 500k to 1.8MHz. CDR =20MHz)	—	0.018	—	0.15	ps
$tj_{PH\_PLL\_SRIS}$	Integrated Phase Jitter PLL Mode (RMS)(1,5) Low Bandwidth (SRIS Architecture)	PCIe 1.0	—	8.71	—	—	ps (p-p)
		PCIe 2.0	—	0.81	—	—	ps
		PCIe 3.0	—	0.329	—	—	ps
		PCIe 4.0	—	0.222	—	—	ps
		PCIe 5.0(11)	—	0.084	—	—	ps
$tj_{PH\_PLL\_CC}$	Integrated Phase Jitter PLL Mode (RMS)(1,5) High Bandwidth (Common Clocked Architecture)	PCIe 1.0(6)	—	5.4	—	86	ps (p-p)
		PCIe 2.0 Low Band, 10kHz < f < 1.5MHz	—	0.09	—	3.1	ps
		PCIe 2.0 High Band, 1.5MHz < f < Nyquist (50MHz)	—	0.019	—	3	ps
		PCIe 3.0 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	—	0.1	—	1	ps
		PCIe 4.0 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	—	0.1	—	0.5	ps
		PCIe 5.0(11) (PLL BW of 500k to 1.8MHz. CDR =20MHz)	—	0.032	—	0.15	ps

HCSL Output AC Characteristics (PLL Mode PCIe Phase Jitter) Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
$tj_{PH\_PLL\_SRIS}$	Integrated Phase Jitter PLL Mode (RMS)(1,5) High Bandwidth (SRIS Architecture)	PCIe 1.0	—	8.61	—	—	ps (p-p)
		PCIe 2.0	—	0.88	—	—	ps
		PCIe 3.0	—	0.354	—	—	ps
		PCIe 4.0	—	0.271	—	—	ps
		PCIe 5.0(11)	—	0.097	—	—	ps

Note:

1. Guaranteed by design and characterization—not 100% tested in production.
2. Measured from differential waveform.
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within ±150mV window.
4. Slew rate matching is measured through ±75mV window centered around differential zero.
5. See http://www.pcisig.com for complete specs.
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10^{-12}.
7. Duty cycle distortion is the difference in duty cycle between the output and input clock when the device is operated in the PLL bypass mode.
8. The Min and Max values of each BW setting track each other, low BW max will never occur with high BW min.
9. Applies to all differential outputs.
10. For additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)^{*2} - (input jitter)^{*2}].
11. PCIe 5.0 v0.9 specification.

HCSL Output AC Characteristics (Fanout Buffer Mode Additive Phase Jitter)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
$tj_{PH\_A\_CC}$	Additive Integrated Phase Jitter (RMS)(1,5) (Common Clocked Architecture)	PCIe 1.0(6)	—	1.3	—	86	ps (p-p)
		PCIe 2.0 Low Band, 10kHz < f < 1.5MHz	—	0.023	—	3.1	ps
		PCIe 2.0 High Band, 1.5MHz < f < Nyquist (50MHz)	—	0.089	—	3	ps
		PCIe 3.0 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	—	0.044	—	1	ps
		PCIe 4.0 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	—	0.044	—	0.5	ps
		PCIe 5.0(11) (PLL BW of 500k to 1.8MHz. CDR =20MHz)	—	0.017	—	0.15	ps
$tj_{PH\_A\_SRIS}$	Additive Integrated Phase Jitter (RMS)(1,5,10) (SRIS Architecture)	PCIe 1.0	—	0.127	—	—	ps (p-p)
		PCIe 2.0	—	0.112	—	—	ps
		PCIe 3.0	—	0.029	—	—	ps
		PCIe 4.0	—	0.031	—	—	ps
		PCIe 5.0(11)	—	0.027	—	—	ps
$tj_{PH\_A\_12k-20M}$	Additive Integrated Phase Jitter (RMS)(1,5,10) 12kHz ~ 20MHz	133.33MHz	—	150	—	—	fs
		100MHz, SSC off	—	90	—	—	fs

Note:

1. Guaranteed by design and characterization—not 100% tested in production.
2. Measured from differential waveform.
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within ±150mV window.
4. Slew rate matching is measured through ±75mV window centered around differential zero.
5. See http://www.pcisig.com for complete specs.
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10^{-12}.
7. Duty cycle distortion is the difference in duty cycle between the output and input clock when the device is operated in the PLL bypass mode.
8. The Min and Max values of each BW setting track each other, low BW max will never occur with high BW min.
9. Applies to all differential outputs.
10. For additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)^{*2} - (input jitter)^{*2}].
11. PCIe 5.0 v0.9 specification.

HCSL Output AC Characteristics (Jitter)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
$tj_{PHPLL\_QPI\_UPI}$	Integrated Phase Jitter PLL Mode (RMS)(1,5)	QPI and UPI, 100M or 133.33MHz, 4.8Gbps, 6.4Gbps 12UI	—	0.16	—	0.5	ps
		QPI and UPI, 100MHz, 8.0Gbps, 12UI	—	0.1	—	0.3	ps
		QPI and UPI, 100MHz, <11.4Gbps, 12UI	—	0.08	—	0.2	ps
$tj_{PH\_QPI\_UPI}$	Fanout Buffer Mode Additive Integrated Phase Jitter (RMS)(1,5,10)	QPI and UPI, 100M or 133.33MHz, 4.8Gbps, 6.4Gbps 12UI	—	0.03	—	—	ps (p-p)
		QPI and UPI, 100MHz, 8.0Gbps, 12UI	—	0.03	—	—	ps
		QPI and UPI, 100MHz, <11.4Gbps, 12UI	—	0.02	—	—	ps
tj_{PH_IFUPI}	PLL Mode IF-UPI phase jitter	Low bandwidth	—	0.1	—	—	ps
		High bandwidth	—	0.17	—	—	ps
	Fanout Buffer Mode IF-UPI phase jitter		—	0.06	—	—	ps
$tj_{PH\_DB2000Q}$	Fanout Buffer Mode DB2000Q phase jitter		—	28	—	—	fs

Note:

1. Guaranteed by design and characterization—not 100% tested in production.
2. Measured from differential waveform.
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within ±150mV window.
4. Slew rate matching is measured through ±75mV window centered around differential zero.
5. See http://www.pcisig.com for complete specs.
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10^{-12}.
7. Duty cycle distortion is the difference in duty cycle between the output and input clock when the device is operated in the PLL bypass mode.
8. The Min and Max values of each BW setting track each other, low BW max will never occur with high BW min.
9. Applies to all differential outputs.
10. For additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)^{*2} - (input jitter)^{*2}].
11. PCIe 5.0 v0.9 specification.

SMBus Serial Data Interface

PI6CBE33085 is a slave-only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.
Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	1	0	0	1/0

Note: SMBus address is latched on SADR pin

SMBus Address

Pin		SMBus Address			
SADR1_tri	SADR0_tri	PI6CBE3312x	PI6CBE3308x	PI6CBE3306x	PI6CBE33045
0	0	D8	D8	D8	D8
0	M	DA	N/A	N/A	DA
0	1	DE	N/A	N/A	DE
M	0	C2	N/A	N/A	N/A
M	M	C4	N/A	N/A	N/A
M	1	C6	N/A	N/A	N/A
1	0	CA	N/A	N/A	N/A
1	M	CC	N/A	N/A	N/A
1	1	CE	N/A	N/A	N/A

Note: PI6CBE3308x and PI6CBE3306x do not have SMBus address select pins. Their address is D8.

How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	.....	Data Byte (N+X-1)	Ack	Stop bit

How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bits	1 bit	1 bit
.....	Data Byte (N+X-1)	NAck	Stop bit

Byte 0: PLL Operating Mode and Frequency Select Register

Bit	Control Function	Description	Type	Power-up Condition	0	1
7	PLLMODERB1	PLL Mode Readback Bit1	R	Latch	00 = Low BW ZDB 01= Fanout mode 10 = Reserved 11 = High BW ZDB	
6	PLLMODERB0	PLL Mode Readback Bit0	R	Latch		
5	Reserved	—		0	—	—
4	Reserved	—		0	—	—
3	PLL SW Control	PLL Mode control Bit0	RW(1)	0	Hardware Latch	SMBus Control
2	PLL mode	PLL Mode 1	RW	1	00 = Low BW ZDB 01= Fanout mode 10 = Reserved 11 = High BW ZDB	
1	PLL mode	PLL Mode 0	RW	1		
0	Frequency Select RB	Frequency select readback	R	Latch	133MHz	100MHz

Byte 1: Output Enable Register 1

Bit	Control Function	Description	Type	Power-up Condition	0	1
7	Q5_OE	Q5 output enable	RW	1	Output Low/ Low	OE Pin Control
6	Q4_OE	Q4 output enable	RW	1	Output Low/ Low	OE Pin Control
5	Q3_OE	Q3 output enable	RW	1	Output Low/ Low	OE Pin Control
4	Q2_OE	Q2 output enable	RW	1	Output Low/ Low	OE Pin Control
3	Reserved	—	RW	0	—	—
2	Q1_OE	Q1 output enable	RW	1	Output Low/ Low	OE Pin Control
1	Q0_OE	Q0 output enable	RW	1	Output Low/ Low	OE Pin Control
0	Reserved	—	RW	0	—	—

Byte 2: Output Enable Register 2

Bit	Control Function	Description	Type	Power-up Condition	0	1
7	Reserved	—	RW	0	—	—
6	Reserved	—	RW	0	—	—
5	Reserved	—	RW	0	—	—
4	Reserved	—	RW	0	—	—
3	Reserved	—	RW	0	—	—
2	Q7_OE	Q7 output enable	RW	1	Output Low/ Low	OE Pin Control
1	Reserved	—	RW	0	—	—
0	Q6_OE	Q6 output enable	RW	1	Output Low/ Low	OE Pin Control

Byte 3 and Byte 4: Reserved

Byte 5: Revision and Vendor ID Register

Bit	Control Function	Description	Type	Power-up Condition	0	1
7	RID3	Revision ID	R	0	rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Diodes = 0011	
2	PVID2		R	0		
1	PVID1		R	1		
0	PVID0		R	1		

Byte 6: Device ID Register

Bit	Control Function	Description	Type	Power-up Condition
7	NA	DID7	R	0hB5 for PI6CBE33085
6		DID6	R	
5		DID5	R	
4		DID4	R	
3		DID3	R	
2		DID2	R	
1		DID1	R	
0		DID0	R	

Byte 7: Byte Count Register

Bit	Control Function	Description	Type	Power-up Condition	0	1
7	Reserved	—		0	—	—
6	Reserved	—		0	—	—
5	Reserved	—		0	—	—
4	BC4	Wring to the register configures how many bytes will be read back on a block read	RW	0	—	—
3	BC3		RW	1	—	—
2	BC2		RW	0	—	—
1	BC1		RW	0	—	—
0	BC0		RW	0	—	—

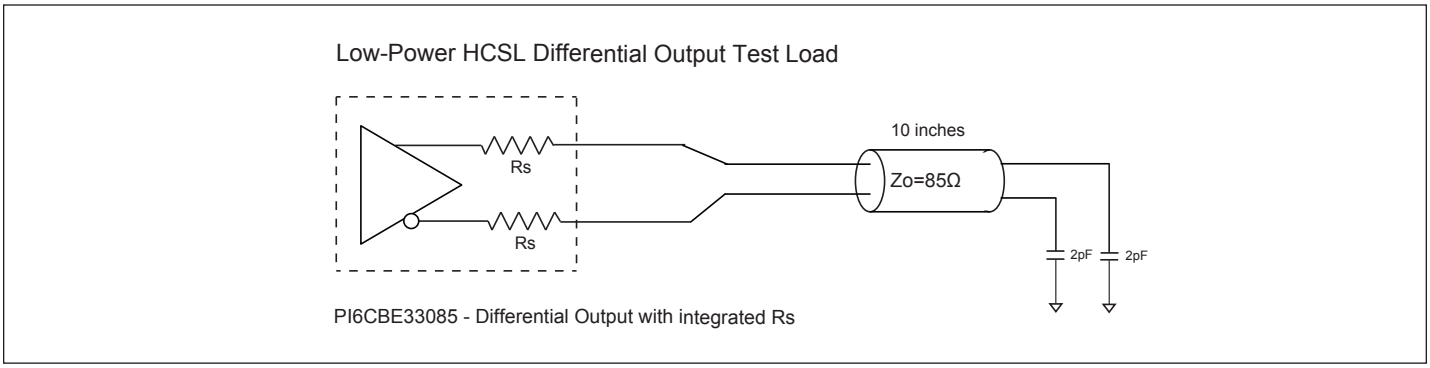


Figure 1. Low-Power HCSL Test Circuit

Test Loads

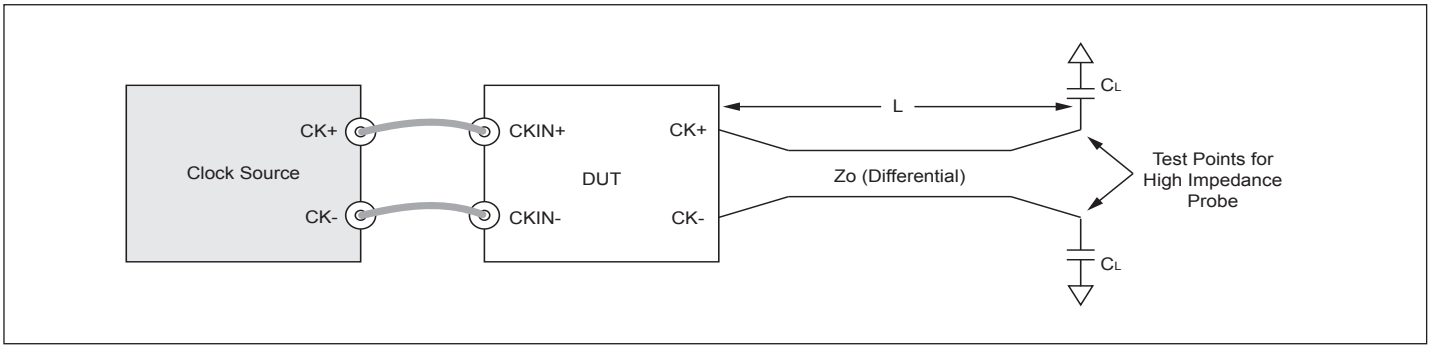


Figure 2. Test Load for AC/DC Measurements

AC/DC Measurements Table

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)
SMA100B	PI6CBE33xx5	Internal	85	25.4	2

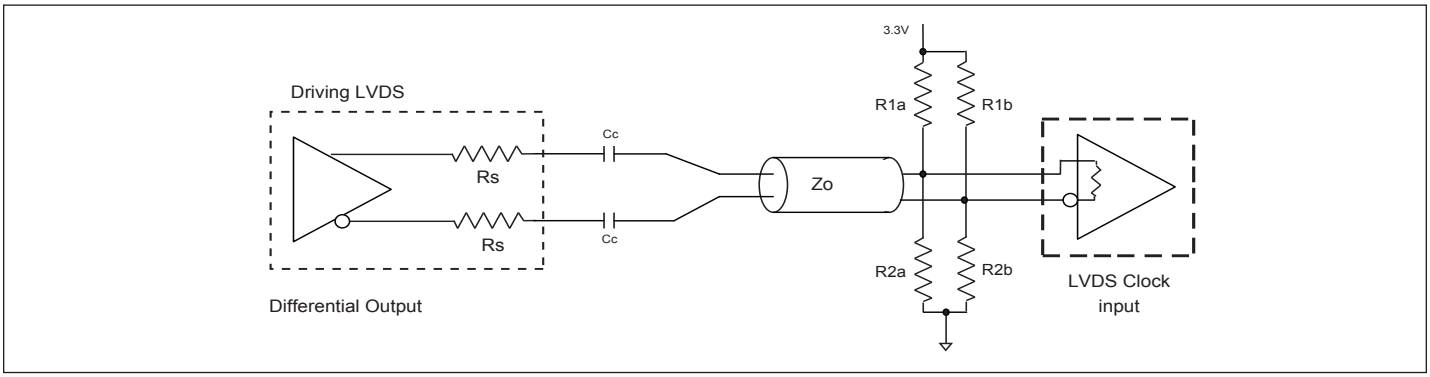


Figure 3. Differential Output Driving LVDS

Alternate Differential Output Terminations (Z_O =85Ω)

Component	Receiver with Termination	Receiver without Termination	Unit
R_{1a}, R_{1b}	10,000	130	Ω
R_{2a}, R_{2b}	5600	64	Ω
C_C	0.1	0.1	µF
V_{CM}	1.2	1.2	V

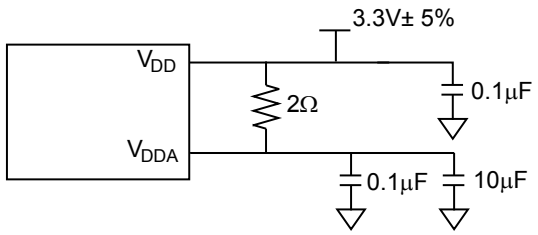


Figure 4. Power Supply Filter

Thermal Characteristics

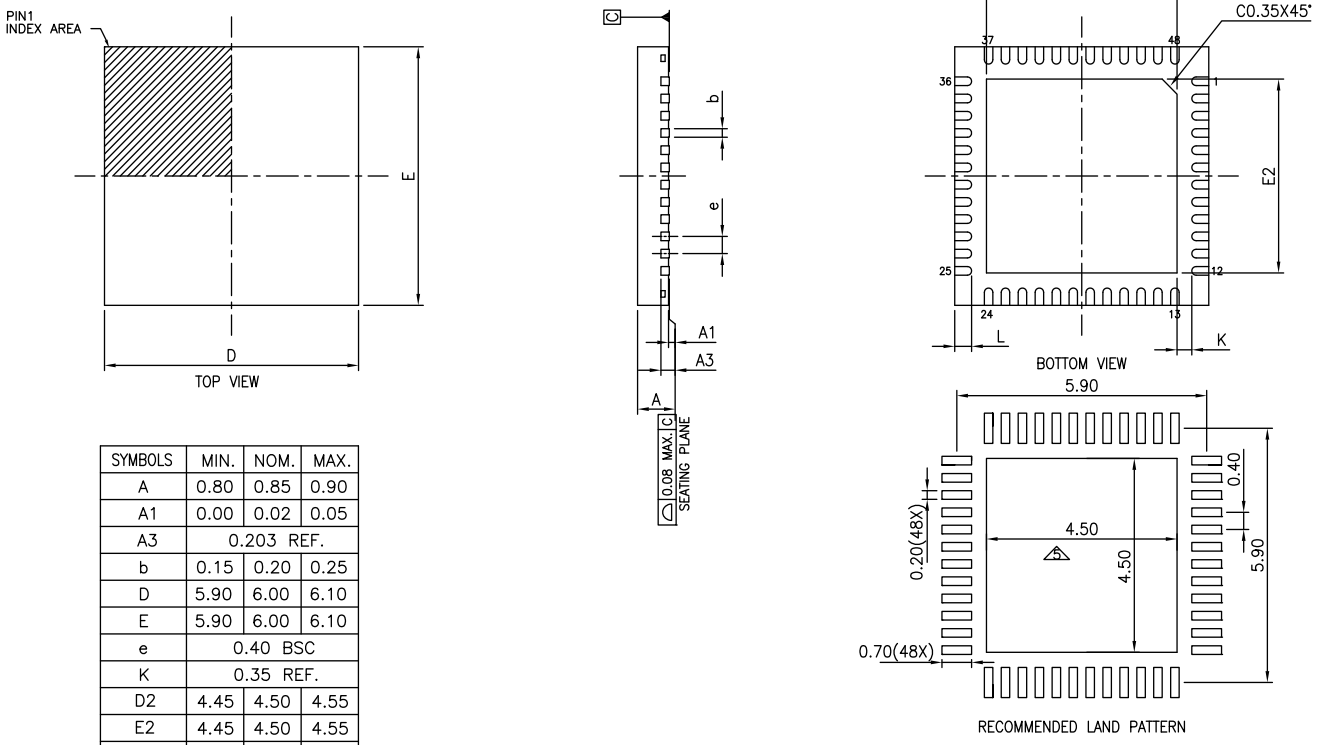
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air				°C/W
θ_{JC}	Thermal Resistance Junction to Case					°C/W

Part Marking

Z: Die Rev
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above Fab Code means Cu Wire

Packaging Mechanical

48-TQFN (ZL)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e		0.40 BSC	
K		0.35 REF.	
D2	4.45	4.50	4.55
E2	4.45	4.50	4.55
L	0.35	0.40	0.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

PERICOM Enabling Serial Connectivity

DATE: 10/26/15

DESCRIPTION: 48-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL (ZL48)

DOCUMENT CONTROL #: PD-2201 REVISION: A

15-0244

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

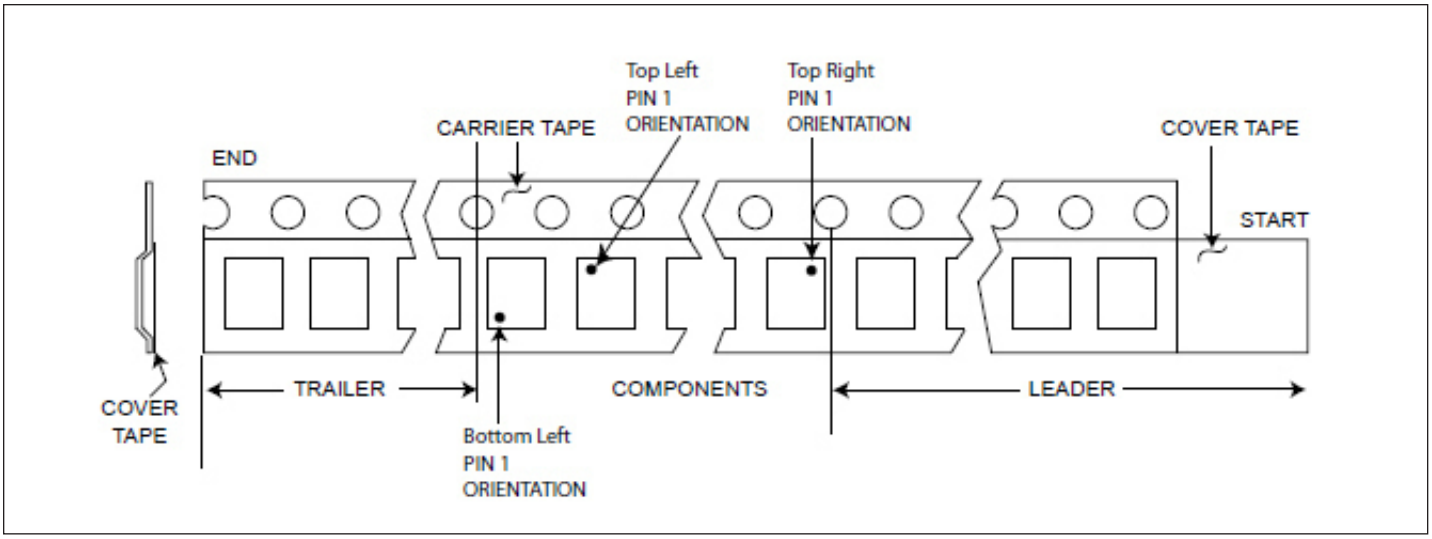
Ordering Information

Ordering Code	Package Code	Package Description	Temperature	Pin 1 Orientation
PI6CBE33085ZLIEX	ZL	48-Contact, Very Thin Quad Flat No-Lead (TQFN)	-40~85°C	Top Right Corner
PI6CBE33085ZLIEX-13R	ZL	48-Contact, Very Thin Quad Flat No-Lead (TQFN)	-40~85°C	Top Left Corner

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel
7. For packaging detail, go to our website at: https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf

Pin 1 Orientation



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