

2.5/3.3V 200-MHz Multi-Output Zero Delay Buffer

Features

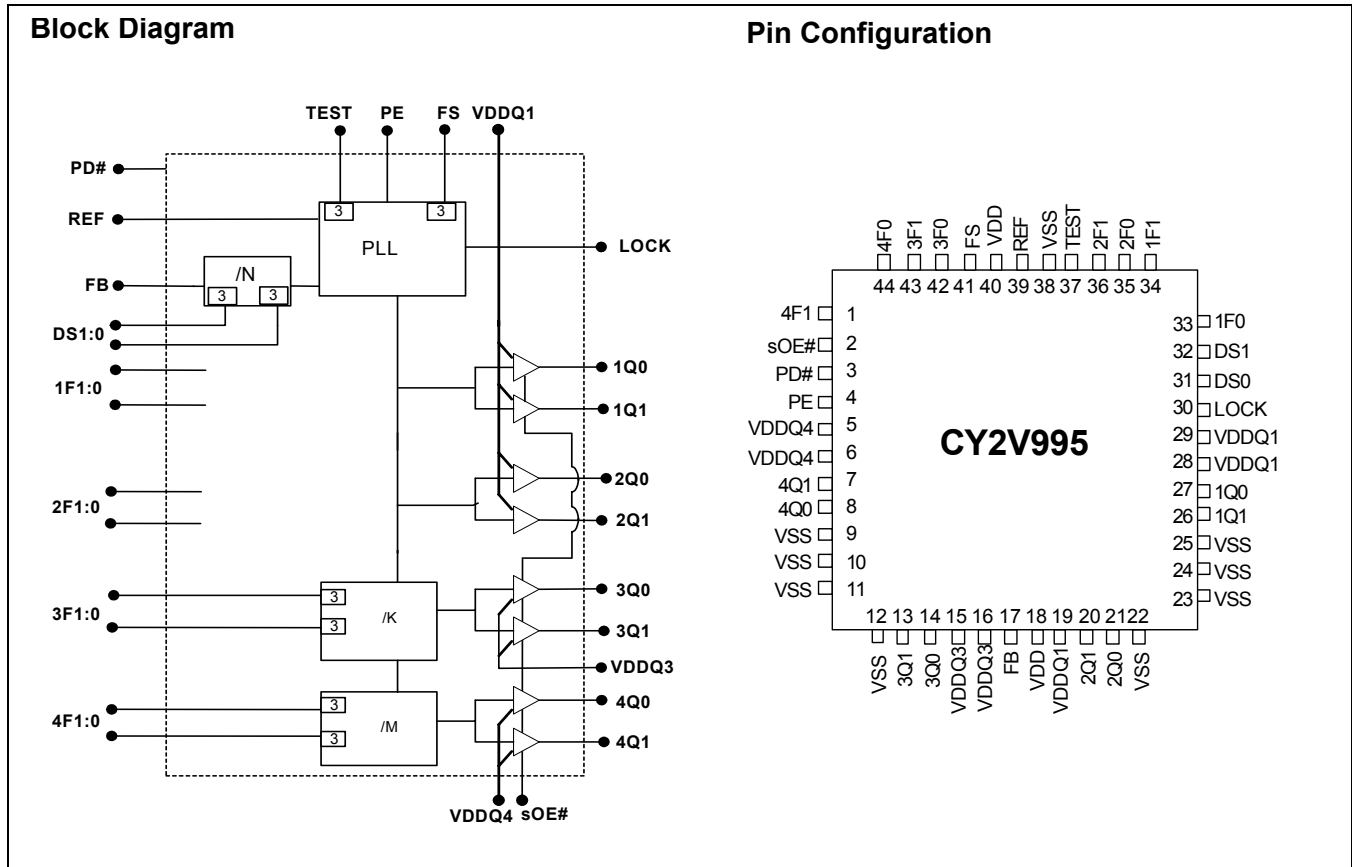
- 2.5V or 3.3V operation
- Split output bank power supplies
- Output frequency range: 6 MHz to 200 MHz
- Output-output skew: < 150 ps
- Cycle-cycle jitter: < 100 ps
- Selectable positive or negative edge synchronization
- 8 LVTTTL outputs driving 50Ω terminated lines
- LVCMOS/LVTTTL over-voltage tolerant reference input
- Selectable phase-locked loop (PLL) frequency range and lock indicator
- (1-6,8,10,12)x multiply and (1/2,1/4)x divide ratios
- Spread-Spectrum-compatible
- Power-down mode
- Industrial temperature range: -40°C to +85°C
- 44-pin TQFP package

Description

The CY2V995 is a low-voltage, low-power, eight output, 200-MHz clock driver. It features function necessary to optimize the timing of high-performance computer and communication systems.

The user can program the frequency of the output banks through nF[0:1] and DS[0:1] pins. Any one of the outputs can be connected to feedback input to achieve different reference frequency multiplication and divide ratios and zero input-output delay.

The device also features split output bank power supplies which enable the user to run two banks (1Qn and 2Qn) at a power supply level different from that of the other two banks (3Qn and 4Qn). Additionally, the PE pin controls the synchronization of the output signals to either the rising or the falling edge of the reference clock.



Pin Description

| Pin | Name | I/O ^[1] | Type | Description |
|-------------------------------|-----------------------------------|--------------------|------------------|--|
| 39 | REF | I | LVTTL/ LVCMOS | Reference Clock Input. |
| 17 | FB | I | LVTTL | Feedback Input. |
| 37 | TEST | I | 3-Level | When MID or HIGH, disables PLL (except for conditions of note 3). REF goes to all outputs. Set LOW for normal operation. |
| 2 | sOE# | I, PD | LVTTL | Synchronous Output Enable. When HIGH, it stops clock outputs (except 2Q0 and 2Q1) in a LOW state (for PE = H or M) – 2Q0 and 2Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and sOE# is high, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set sOE# LOW for normal operation. |
| 4 | PE | I, PU | LVTTL | Selects Positive or Negative Edge Control and High or Low output drive strength. When LOW / HIGH the outputs are synchronized with the negative/positive edge of the reference clock, respectively. Please see <i>Table 8</i> . |
| 34, 33, 36, 35, 43, 42, 1, 44 | nF[1:0] | I | 3-Level | Select frequency of the outputs. Please see <i>Tables 3, 4, 5, and 7</i> . |
| 41 | FS | I | 3-Level | Selects VCO operating frequency range. Please see <i>Table 6</i> . |
| 26,27,20,21, 13,14,7,8 | nQ[1:0] | O | LVTTL | Four banks of two outputs. Please see <i>Table 5</i> for frequency settings. |
| 32, 31 | DS[1:0] | I | 3-Level | Select feedback divider. Please see <i>Table 1</i> . |
| 3 | PD# | I, PU | LVTTL | Power-down and reference divider control. When LOW, shuts off entire chip. Please see <i>Table 2</i> for settings. |
| 30 | LOCK | O | LVTTL | PLL lock indication signal. HIGH indicates lock. LOW indicates that the PLL is not locked and outputs may not be synchronized to the input. |
| 5,6 | V _{DD} Q4 ^[2] | PWR | Power | Power supply for Bank 4 output buffers. Please see <i>Table 8</i> for supply level constraints |
| 15,16 | V _{DD} Q3 ^[2] | PWR | Power | Power supply for Bank 3 output buffers. Please see <i>Table 8</i> for supply level constraints |
| 19,28 | V _{DD} Q1 ^[2] | PWR | Power | Power supply for Bank 1 and Bank 2 output buffers. Please see <i>Table 8</i> for supply level constraints |
| 18,40 | V _{DD} ^[2] | PWR | Power | Power supply for the internal circuitry. Please see <i>Table 8</i> for supply level constraints |
| 9-12, 22-25, 38 | V _{SS} | PWR | Power | Ground |

Device Configuration

The outputs of the CY2V995 can be configured to run at frequencies ranging from 6 MHz to 200 MHz. The feedback input divider is controlled by the 3-level DS[0:1] pins as indicated in *Table 1*.

Table 1. Feedback Divider Settings

| DS[1:0] | N-Feedback Input Divider | Permitted Output Divider Connected to FB ^[4] |
|---------|--------------------------|---|
| LL | 2 | 1 or 2 |
| LM | 3 | 1 |
| LH | 4 | 1,2 or 4 |
| ML | 5 | 1 or 2 |
| MM | 1 | 1,2 or 4 |
| MH | 6 | 1 or 2 |
| HL | 8 | 1 or 2 |
| HM | 10 | 1 |
| HH | 12 | 1 |

Notes:

- 'PD' indicates an internal pull-down and 'PU' indicates an internal pull-up.
- A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.
- When TEST = MID and sOE# = HIGH, PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless nF[1:0] = LL.
- Permissible output division ratios connected to FB. The frequency of the REF input will be F_{NOM}/N when the part is configured for frequency multiplication by using an undivided output for FB and setting DS[1:0] to N (N = 1-6, 8, 10, 12).

Table 2. Power-down Mode

| PD# | CY2V995 |
|-----|------------|
| H | Enabled |
| L | Power Down |

In addition to the feedback dividers, the CY2V995 includes output dividers on Bank3 and Bank4, which are controlled by 3F[1:0] and 4F[1:0] as indicated in *Table 3* and *4*, respectively.

Table 3. Output Divider Settings – Bank 3

| 3F[1:0] | K – Bank3 Output Divider |
|-------------------|--------------------------|
| LL ^[5] | 2 |
| HH | 4 |
| Other | 1 |

Table 4. Output Divider Settings – Bank 4

| 4F[1:0] | M – Bank4 Output Divider |
|-------------------|--------------------------|
| LL ^[5] | 2 |
| HH | Inverted ^[6] |
| Other | 1 |

The divider settings, output frequencies, and possible configurations of connecting FB to ANY output are summarized in *Table 5*.

Table 5. Output Frequency Settings

| Configuration | Output Frequency | | |
|---------------|--------------------------|------------------------------------|--------------------------------|
| | FB Input Connected to | 1Q[0:1] and 2Q[0:1] ^[7] | 3Q[0:1] |
| 1Qn or 2Qn | N x F _{REF} | N / x (1 / K) x F _{REF} | N x (1 / M) x F _{REF} |
| 3Qn | N x K x F _{REF} | N x F _{REF} | N x (K / M) x F _{REF} |
| 4Qn | N x M x F _{REF} | N x (M / K) x F _{REF} | N x F _{REF} |

The 3-level FS control pin setting determines the nominal operating frequency range of the divide-by-one outputs of the device. The CY2V995 PLL operating frequency range that corresponds to each FS level is given in *Table 6*.

Notes:

- LL disables outputs if TEST = MID and sOE# = HIGH.
- When 4Q[0:1] are set to run inverted (HH mode), sOE# disables these outputs HIGH when PE = HIGH or MID, sOE# disables them LOW when PE = LOW.
- These outputs are undivided copies of the VCO clock. Therefore, the formulas in this column can be used to calculate the VCO operating frequency (F_{NOM}) at a given reference frequency (F_{REF}) and divider and feedback configuration. The user must select a configuration and a reference frequency that will generate a VCO frequency that is within the range specified by FS pin. Please see *Table 6*.
- V_{DD}Q1/3/4 must not be set at a level higher than that of V_{DD}. They can be set at different levels from each other, e.g. V_{DD} = 3.3V, V_{DD}Q1 = 3.3V, V_{DD}Q3 = 2.5V and V_{DD}Q4 = 2.5V.

Table 6. Frequency Range Select

| FS | PLL Frequency Range |
|----|---------------------|
| L | 24 to 50 MHz |
| M | 48 to 100 MHz |
| H | 96 to 200 MHz |

The PE pin determines Whether the outputs synchronize to the rising or the falling edge of the reference signal, as indicated in *Table 7*.

Table 7. PE Settings

| PE | Synchronization |
|----|-----------------|
| L | Negative |
| H | Positive |

The CY2V995 features split power supply buses for Banks 1 and 2, Bank 3 and Bank 4, which enables the user to obtain both 3.3V and 2.5V output signals from one device. The core power supply (V_{DD}) must be set a level which is equal or higher than that on any one of the output power supplies.

Table 8. Power Supply Constraints

| V _{DD} | V _{DD} Q1 ^[8] | V _{DD} Q3 ^[8] | V _{DD} Q4 ^[8] |
|-----------------|-----------------------------------|-----------------------------------|-----------------------------------|
| 3.3V | 3.3V or 2.5V | 3.3V or 2.5V | 3.3V or 2.5V |
| 2.5V | 2.5V | 2.5V | 2.5V |

Governing Agencies

The following agencies provide specifications that apply to the CY2V995. The agency name and relevant specification is listed below.

| Agency Name | Specification |
|-------------|--------------------------------------|
| JEDEC | JESD 51 (Theta JA) |
| | JESD 65 (Skew, Jitter) |
| IEEE | 1596.3 (Jiter Specs) |
| UL-194_V0 | 94 (Moisture Grading) |
| MIL | 883E Method 1012.1 (Therma Theta JC) |

Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|-----------------------|-----------------------------------|-----------------------------|-----------------------|-----------------------|------|
| V _{DD} | Operating Voltage | Functional @ 2.5V ± 5% | 2.25 | 2.75 | V |
| V _{DD} | Operating Voltage | Functional @ 3.3V ± 10% | 2.97 | 3.63 | V |
| V _{IN(MIN)} | Input Voltage | Relative to V _{SS} | V _{SS} - 0.3 | - | V |
| V _{IN(MAX)} | Input Voltage | Relative to V _{DD} | - | V _{DD} + 0.3 | V |
| V _{REF(MAX)} | Reference Input Voltage | V _{DD} = 3.3V | | 5.5 | V |
| V _{REF(MAX)} | Reference Input Voltage | V _{DD} = 2.5V | | 4.6 | V |
| T _S | Temperature, Storage | Non Functional | -65 | +150 | °C |
| T _A | Temperature, Operating Ambient | Functional | -40 | +85 | °C |
| T _J | Temperature, Junction | Functional | - | 155 | °C |
| ESD _{HBM} | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | - | V |
| ∅ _{JC} | Dissipation, Junction to Case | Mil-Spec 883E Method 1012.1 | 42 | | °C/W |
| ∅ _{JA} | Dissipation, Junction to Ambient | JEDEC (JESD 51) | 74 | | °C/W |
| UL-94 | Flammability Rating | @1/8 in. | V - 0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |
| F _{IT} | Failure in Time | Manufacturing Testing | 10 | | ppm |

DC Specifications @ 2.5V

| Parameter | Description | Conditions | Min. | Max. | Unit |
|---------------------------------|--------------------------|--|--------------------------|--------------------------|------|
| V _{DD} | 2.5 Operating Voltage | 2.5V ± 5% | 2.375 | 2.625 | V |
| V _{IL} | Input LOW Voltage | REF, FB, PE, PD#, and sOE# Inputs | - | 0.7 | V |
| V _{IH} | Input HIGH Voltage | | 1.7 | - | V |
| V _{IHH} ^[9] | Input HIGH Voltage | 3-Level Inputs (TEST, FS, nF[1:0], DS[1:0]) (These pins are normally wired to VDD, GND or unconnected) | V _{DD} - 0.4 | - | V |
| V _{IMM} ^[9] | Input MID Voltage | | V _{DD} /2 - 0.2 | V _{DD} /2 + 0.2 | V |
| V _{ILL} ^[9] | Input LOW Voltage | | - | 0.4 | V |
| I _{IL} | Input Leakage Current | V _{IN} = V _{DD} /G _{ND} , V _{DD} = Max (REF and FB inputs) | -5 | 5 | μA |
| I ₃ | 3-Level Input DC Current | HIGH, V _{IN} = V _{DD} | - | 200 | μA |
| | | MID, V _{IN} = V _{DD} /2 | -50 | 50 | μA |
| | | LOW, V _{IN} = V _{SS} | -200 | - | μA |
| I _{PU} | Input Pull-up Current | V _{IN} = V _{SS} , V _{DD} = Max | -25 | - | μA |
| I _{PD} | Input Pull-down Current | V _{IN} = V _{DD} , V _{DD} = Max, (sOE#) | - | 100 | μA |
| V _{OL} | Output LOW Voltage | I _{OL} = 12mA, (nQ[0:1]) | - | 0.4 | V |
| | | I _{OL} = 2mA (LOCK) | | 0.4 | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -12mA, (nQ[0:1]) | 2.0 | - | V |
| | | I _{OH} = -2mA (LOCK) | 2.0 | | V |
| I _{DDQ} | Quiescent Supply Current | V _{DD} = Max, TEST = MID, REF = LOW, sOE# = LOW, Outputs not loaded | - | 2 | mA |
| I _{DDPD} | Power-down Current | PD#, sOE# = LOW Test, nF[1:0], DS[1:0] = HIGH V _{DD} = Max | 10(typ.) | 25 | μA |
| I _{DD} | Dynamic Supply Current | @100 MHz | | 150 | mA |
| C _{IN} | Input Pin Capacitance | | | 4 | pF |

Note:

9. These Inputs are normally wired to VDD, GND or unconnected. Internal termination resistors bias unconnected inputs to VDD/2.

DC Specifications @ 3.3V

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|--------------------------|---|------------------------|------------------------|------|
| V _{DD} | 3.3 Operating Voltage | 3.3V ± 10% | 2.97 | 3.63 | V |
| V _{IL} | Input LOW Voltage | REF, PE, PD#, FB and sOE# Inputs | – | 0.8 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | – | V |
| V _{IHH} ^[9] | Input HIGH Voltage | 3-Level Inputs (TEST, FS, nF[1:0], DS[1:0]) (These pins are normally wired to VDD,GND or unconnected) | V _{DD} –0.6 | – | V |
| V _{IMM} ^[9] | Input MID Voltage | | V _{DD} /2–0.3 | V _{DD} /2+0.3 | V |
| V _{ILL} ^[9] | Input LOW Voltage | | – | 0.6 | V |
| I _{IL} | Input Leakage Current | V _{IN} = V _{DD} /G _{ND} , V _{DD} = Max (REF and FB inputs) | –5 | 5 | µA |
| I ₃ | 3-Level Input DC Current | HIGH, V _{IN} = V _{DD} | – | 200 | µA |
| | | MID, V _{IN} = V _{DD} /2 | –50 | 50 | µA |
| | | LOW, V _{IN} = V _{SS} | –200 | – | µA |
| I _{PU} | Input Pull-Up Current | V _{IN} = V _{SS} , V _{DD} = Max | –25 | – | µA |
| I _{PD} | Input Pull-Down Current | V _{IN} = V _{DD} , V _{DD} = Max, (sOE#) | – | 100 | µA |
| V _{OL} | Output LOW Voltage | I _{OL} = 12mA, (nQ[0:1]) | – | 0.4 | V |
| | | I _{OL} = 2mA (LOCK) | | 0.4 | |
| V _{OH} | Output HIGH Voltage | I _{OH} = –12mA, (nQ[0:1]) | 2.4 | – | V |
| | | I _{OH} = –2mA (LOCK) | 2.4 | | |
| I _{DDQ} | Quiescent Supply Current | V _{DD} = Max, TEST = MID, REF = LOW, sOE# = LOW, Outputs not loaded | – | 2 | mA |
| I _{DDPD} | Power-down Current | PD#, sOE# = LOW Test, nF[1:0], DS[1:0] = HIGH V _{DD} = Max | 10(typ.) | 25 | µA |
| I _{DD} | Dynamic Supply Current | @100 MHz | 230 | | mA |
| C _{IN} | Input Pin Capacitance | | 4 | | pF |

AC Input Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|---------------------------|-------------|------|------|------|
| T _R , T _F | Input Rise/Fall Time | 0.8V – 2.0V | – | 10 | ns/V |
| T _{PWC} | Input Clock Pulse | HIGH or LOW | 2 | – | ns |
| T _{DCIN} | Input Duty Cycle | | 10 | 90 | % |
| F _{REF} | Reference Input Frequency | FS = LOW | 2 | 50 | MHz |
| | | FS = MID | 4 | 100 | |
| | | FS = HIGH | 8 | 200 | |

Switching Characteristics

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------|-----------------------------------|---|------|------|------|
| F _{OR} | Output frequency range | | 6 | 200 | MHz |
| VCO _{LR} | VCO Lock Range | | 200 | 400 | MHz |
| VCO _{LBW} | VCO Loop Bandwidth | | 0.25 | 3.5 | MHz |
| t _{SKEWPR} | Matched-Pair Skew ^[10] | Skew between the earliest and the latest output transitions within the same bank. | – | 150 | ps |

Note:

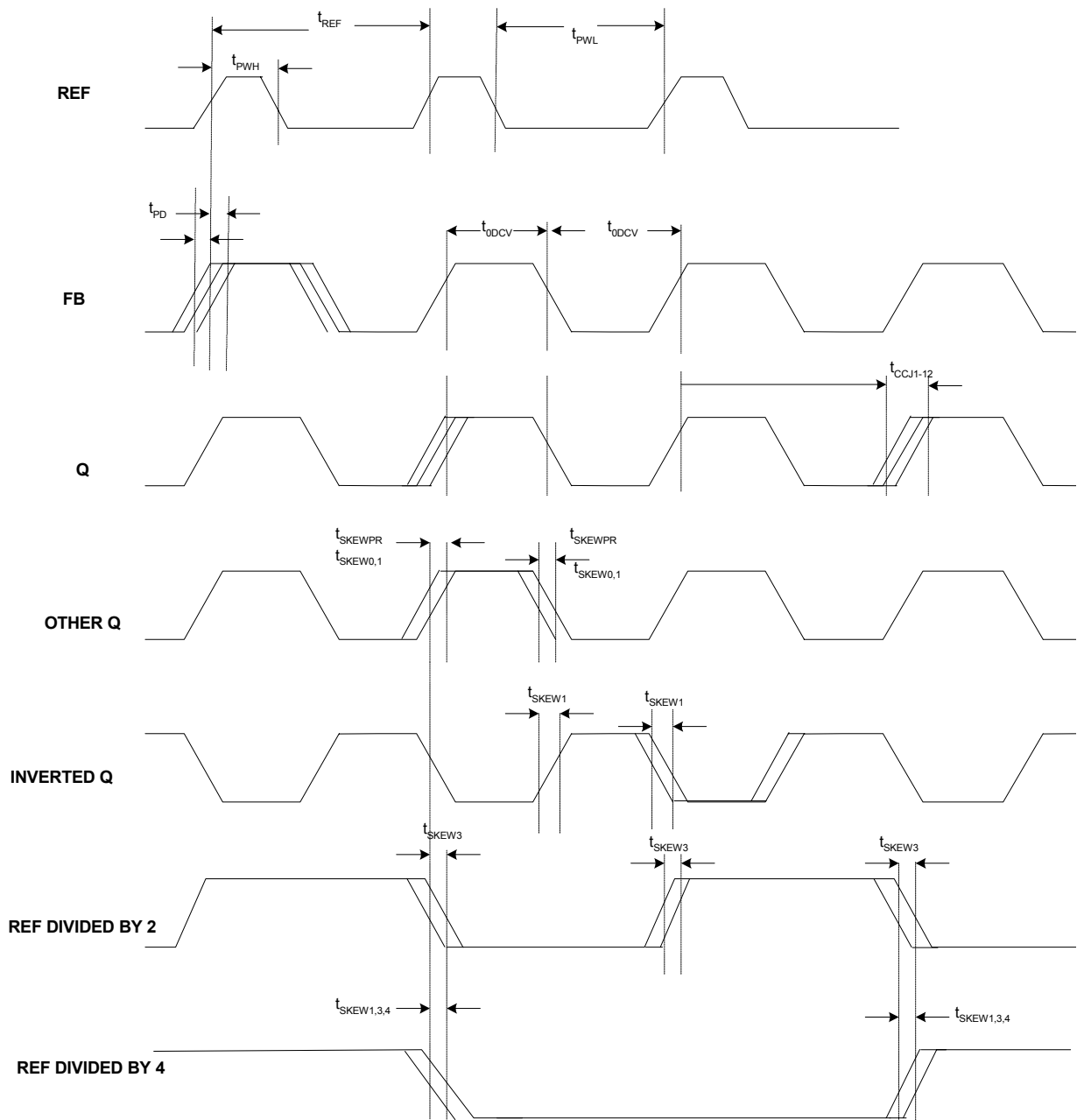
10. Test Load = 20 pF, terminated to VCC/2. All outputs are equally loaded.

Switching Characteristics (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|--------------------------------|---|---|------|------|------|
| t _{SKEW0} | Output-Output Skew ^[10] | Skew between the earliest and the latest output transitions among all outputs. | – | 200 | ps |
| t _{SKEW1} | | Skew between the earliest and the latest output transitions among all same class outputs. | – | 200 | ps |
| t _{SKEW2} | | Skew between the nominal output rising edge to the inverted output falling edge | – | 500 | ps |
| t _{SKEW3} | | Skew between non-inverted outputs running at different frequencies | – | 500 | ps |
| t _{SKEW4} | | Skew between nominal to inverted outputs running at different frequencies | – | 500 | ps |
| t _{SKEW5} | | Skew between nominal outputs at different power supply levels | – | 650 | ps |
| t _{PART} | Part-Part Skew | Skew between the outputs of any two devices under identical settings and conditions (VDDQ, VDD, temp, air flow, frequency, etc) | – | 750 | ps |
| t _{PD0} | Ref to FB Propagation Delay ^[11] | | –250 | +250 | ps |
| t _{ODCV} | Output Duty Cycle | Measured at VDD/2 | 45 | 55 | % |
| t _{PWH} | Output High Time Deviation from 50% | Measured at 2.0V for VDD = 3.3V and at 1.7V for VDD = 2.5V. | – | 1.5 | ns |
| t _{PWL} | Output Low Time Deviation from 50% | Measured at 0.8V for VDD = 3.3V and at 0.7V for VDD = 2.5V. | – | 2.0 | ns |
| t _R /t _F | Output Rise/Fall Time | Measured at 0.8V-2.0V for VDD = 3.3V and 0.7V–1.7V for VDD = 2.5V | 0.15 | 1.5 | ns |
| t _{LOCK} | PLL lock time ^[12, 13] | | – | 0.5 | ms |
| t _{CCJ} | Cycle-Cycle Jitter | Divide by 1 output frequency, FS = L, FB = divide by any | – | 100 | ps |
| | | Divide by 1 output frequency, FS = M/H, FB = divide by any | – | 150 | ps |

Notes:

11. t_{PD} is measured at 1.5V for VDD = 3.3V and at 1.25V for VDD = 2.5V with REF rise/fall times of 0.5 ns between 0.8V–2.0V.
12. t_{LOCK} is the time that is required before outputs synchronize to REF. This specification is valid with stable power supplies which are within normal operating limits.
13. Lock detector circuit may be unreliable for input frequencies lower than 4MHz, or for input signals which contain significant jitter.

AC Timing Definitions


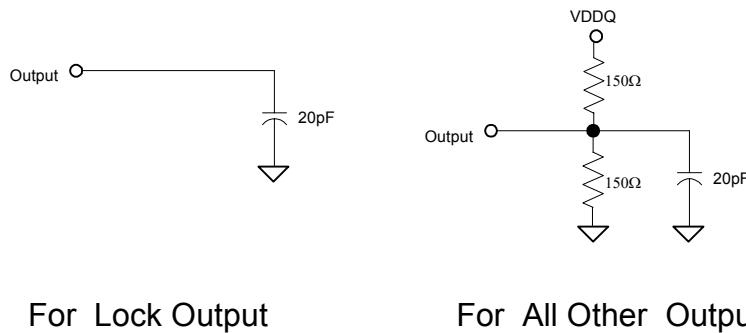
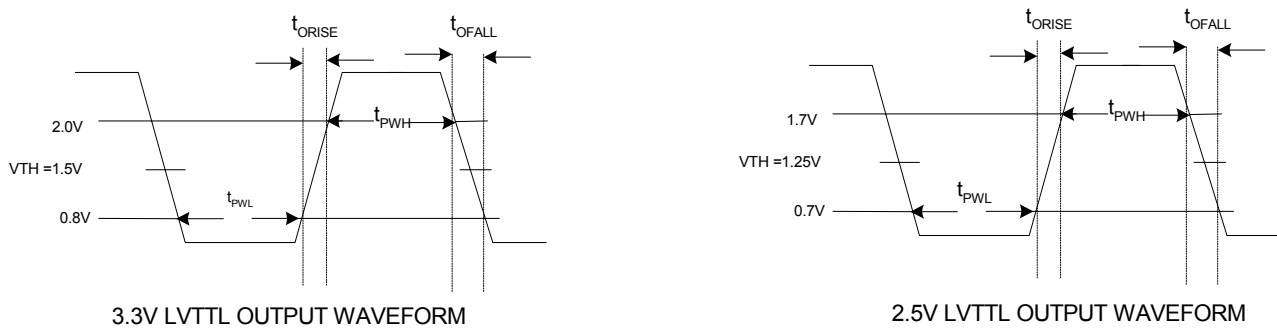
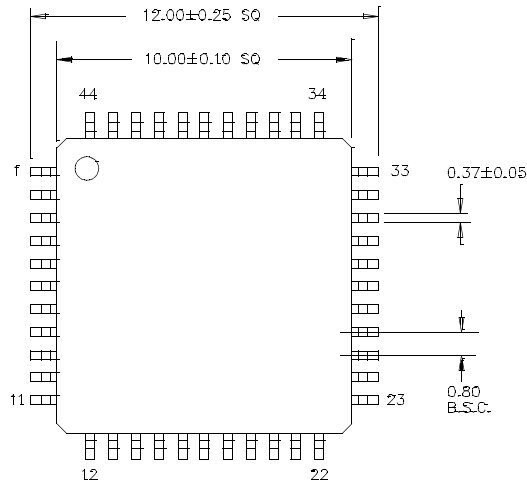
AC Test Loads and Waveforms

Figure 1.

Figure 2.

Figure 3.
Ordering Information

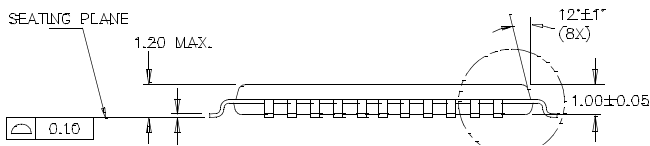
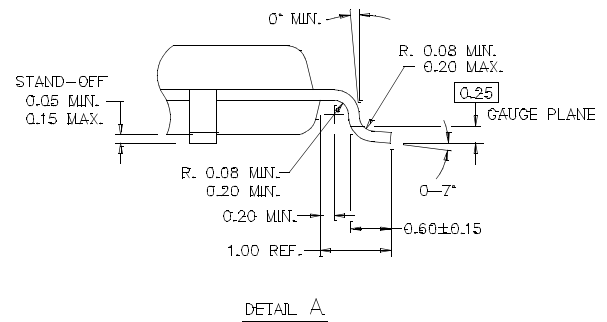
| Part Number | Package Type | Product Flow |
|-------------|-------------------------|--------------------------|
| CY2V995AC | 44 TQFP | Commercial, 0° to 70°C |
| CY2V995ACT | 44 TQFP – Tape and Reel | Commercial, 0° to 70°C |
| CY2V995AI | 44 TQFP | Industrial, -40° to 85°C |
| CY2V995AIT | 44 TQFP – Tape and Reel | Industrial, -40° to 85°C |

Package Drawing and Dimensions

44-lead Thin Plastic Quad Flat Pack (10 x 10 x 1.0 mm) A44SB



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Document History Page

| Document Title: CY2V995 2.5/3.3V 200-MHz Multi-output Zero Delay Buffer | | | | |
|---|---------|------------|-----------------|--|
| Document Number: 38-07435 | | | | |
| REV. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 122627 | 01/13/03 | RGL | New Data Sheet |
| *A | 200501 | See ECN | RGL | Changed Pin 5 from VDD to VDDQ4, Pin 16 from VDD to VDDQ3 and Pin 29 from VDD to VDDQ1 |