

FEATURES

- Two 1.6 GHz, differential clock inputs
- 5 programmable dividers, 1 to 32, all integers
- 3 independent 1.2 GHz LVPECL outputs
- Additive output jitter 225 fs rms
- 2 independent 800 MHz/250 MHz LVDS/CMOS clock outputs
- Additive output jitter: 275 fs rms
- Serial control port
- Space-saving 48-lead LFCSP

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (-55°C to $+85^{\circ}\text{C}$)
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- Defense and aerospace applications

GENERAL DESCRIPTION

The **AD9512-EP** provides a multi-output clock distribution in a design that emphasizes low jitter and low phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements can also benefit from this device.

There are five independent clock outputs. Three outputs are LVPECL (1.2 GHz), and two are selectable as either LVDS (800 MHz) or CMOS (250 MHz) levels.

Each output has a programmable divider that can be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output can be varied by means of a divider phase select function that serves as a coarse timing adjustment.

FUNCTIONAL BLOCK DIAGRAM

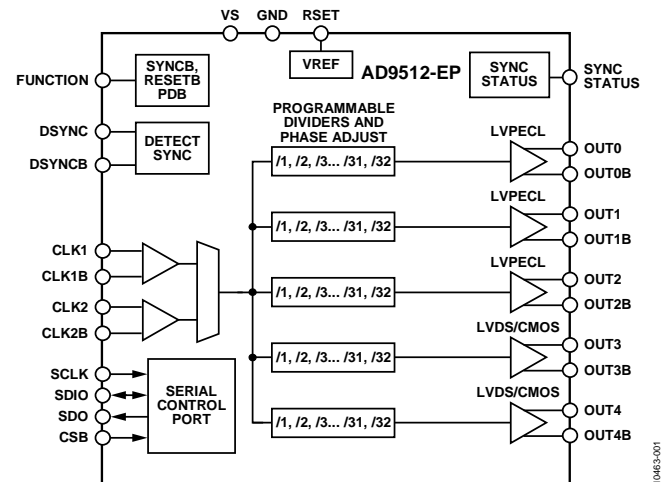


Figure 1.

The **AD9512-EP** is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The **AD9512-EP** is available in a 48-lead LFCSP and can be operated from a single 3.3 V supply. The temperature range is -55°C to $+85^{\circ}\text{C}$.

Additional application and technical information can be found in the **AD9512** data sheet.

Note that the delay block element that exists in Channel 4 of the **AD9512** standard product is not supported in this **AD9512-EP** version.

TABLE OF CONTENTS

| | | | |
|---------------------------------|---|--|----|
| Features | 1 | Clock Output Additive Time Jitter..... | 8 |
| Enhanced Product Features | 1 | Serial Control Port | 10 |
| Applications..... | 1 | FUNCTION Pin | 10 |
| Functional Block Diagram | 1 | SYNC STATUS Pin | 11 |
| General Description | 1 | Power..... | 11 |
| Revision History | 2 | Absolute Maximum Ratings | 12 |
| Specifications..... | 3 | Thermal Resistance | 12 |
| Clock Inputs | 3 | Pin Configuration and Function Descriptions..... | 13 |
| Clock Outputs | 3 | Typical Performance Characteristics | 15 |
| Timing Characteristics | 4 | Outline Dimensions | 18 |
| Clock Output Phase Noise | 5 | Ordering Guide | 18 |

REVISION HISTORY

11/2018—Rev. 0 to Rev. A

| | |
|----------------------------------|----|
| Changes to Figure 2..... | 13 |
| Updated Outline Dimensions | 18 |
| Changes to Ordering Guide | 18 |

3/2012—Revision 0: Initial Version

SPECIFICATIONS

The typical value is given for $V_S = 3.3 \text{ V} \pm 5\%$; $T_A = 25^\circ\text{C}$, $R_{SET} = 4.12 \text{ k}\Omega$, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (-55°C to $+85^\circ\text{C}$) variation.

CLOCK INPUTS

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|------------------|----------------|------------|--|
| CLOCK INPUTS (CLK1, CLK2) ¹ | | | | | |
| Input Frequency | 0 | | 1.6 | GHz | |
| Input Sensitivity | | 150 ² | | mV p-p | Jitter performance can be improved with higher slew rates (greater swing). |
| Input Level | | | 2 ³ | V p-p | Larger swings turn on the protection diodes and can degrade jitter performance. |
| Input Common-Mode Voltage, V_{CM} | 1.45 | 1.6 | 1.7 | V | Self-biased; enables ac coupling; at full temperature range. At -40°C to $+85^\circ\text{C}$. |
| | 1.5 | 1.6 | 1.7 | V | |
| Input Common-Mode Range, V_{CMR} | 1.3 | | 1.8 | V | With 200 mV p-p signal applied; dc-coupled. |
| Input Sensitivity, Single-Ended | | 150 | | mV p-p | CLK2 ac-coupled; CLK2B ac bypassed to RF ground. |
| Input Resistance | 4.0 | 4.8 | 5.6 | k Ω | Self-biased. |
| Input Capacitance | | 2 | | pF | |

¹ CLK1 and CLK2 are electrically identical; each can be used as either differential or single-ended input.

² With a 50 Ω termination, this is -12.5 dBm .

³ With a 50 Ω termination, this is $+10 \text{ dBm}$.

CLOCK OUTPUTS

Table 2.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------|--------------|--------------|------|--|
| LVPECL CLOCK OUTPUTS | | | | | |
| OUT0, OUT1, OUT2; Differential | | | | | Termination = 50 Ω to $V_S - 2 \text{ V}$ |
| Output Frequency | | | 1200 | MHz | Output level 0x3D (0x3E) (0x3F)[3:2] = 10b |
| Output High Voltage (V_{OH}) | $V_S - 1.22$ | $V_S - 0.98$ | $V_S - 0.93$ | V | See Figure 10 |
| Output Low Voltage (V_{OL}) | $V_S - 2.10$ | $V_S - 1.80$ | $V_S - 1.67$ | V | |
| Output Differential Voltage (V_{OD}) | 660 | 810 | 965 | mV | |
| LVDS CLOCK OUTPUTS | | | | | |
| OUT3, OUT4; Differential | | | | | Termination = 100 Ω differential; default |
| Output Frequency | | | 800 | MHz | Output level 0x40 (0x41)[2:1] = 01b |
| Differential Output Voltage (V_{OD}) | 250 | 360 | 450 | mV | 3.5 mA termination current |
| Delta V_{OD} | | | 25 | mV | See Figure 11 |
| Output Offset Voltage (V_{OS}) | 1.05 | 1.23 | 1.375 | V | At full temperature range |
| | 1.125 | 1.23 | 1.375 | V | At -40°C to $+85^\circ\text{C}$ |
| Delta V_{OS} | | | 25 | mV | |
| Short-Circuit Current (I_{SA} , I_{SB}) | | 14 | 24 | mA | Output shorted to GND |
| CMOS CLOCK OUTPUTS | | | | | |
| OUT3, OUT4 | | | | | Single-ended measurements; |
| Output Frequency | | | 250 | MHz | B outputs: inverted, termination open |
| Output Voltage High (V_{OH}) | $V_S - 0.1$ | | | V | With 5 pF load each output; see Figure 12 |
| Output Voltage Low (V_{OL}) | | | 0.1 | V | At 1 mA load |
| | | | | V | At 1 mA load |

TIMING CHARACTERISTICS

Table 3.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|------|------|-------|---|
| LVPECL | | | | | Termination = 50 Ω to $V_S - 2V$ Output level 0x3D (0x3E) (0x3F)[3:2] = 10b |
| Output Rise Time, t_{RP} | | 130 | 180 | ps | 20% to 80%, measured differentially |
| Output Fall Time, t_{FP} | | 130 | 180 | ps | 80% to 20%, measured differentially |
| PROPAGATION DELAY, t_{PECL} , CLK-TO-LVPECL OUT ¹ | | | | | |
| Divide = Bypass | 320 | 490 | 635 | ps | At full temperature range |
| | 335 | 490 | 635 | ps | At -40°C to +85°C |
| Divide = 2 to 32 | 360 | 545 | 695 | ps | At full temperature range |
| | 375 | 545 | 695 | ps | At -40°C to +85°C |
| Variation with Temperature | | 0.5 | | ps/°C | |
| OUTPUT SKEW, LVPECL OUTPUTS | | | | | |
| OUT1 to OUT0 on Same Device, t_{SKP}^2 | 70 | 100 | 140 | ps | |
| OUT1 to OUT2 on Same Device, t_{SKP}^2 | 15 | 45 | 80 | ps | |
| OUT0 to OUT2 on Same Device, t_{SKP}^2 | 45 | 65 | 90 | ps | |
| All LVPECL OUT Across Multiple Devices, $t_{SKP_AB}^3$ | | | 275 | ps | |
| Same LVPECL OUT Across Multiple Devices, $t_{SKP_AB}^3$ | | | 130 | ps | |
| LVDS | | | | | Termination = 100 Ω differential Output level 0x40 (0x41) [2:1] = 01b 3.5 mA termination current |
| Output Rise Time, t_{RL} | | 200 | 350 | ps | 20% to 80%, measured differentially |
| Output Fall Time, t_{FL} | | 210 | 350 | ps | 80% to 20%, measured differentially |
| PROPAGATION DELAY, t_{LVDS} , CLK-TO-LVDS OUT ¹ | | | | | |
| OUT3 to OUT4 | | | | | |
| Divide = Bypass | 0.97 | 1.33 | 1.59 | ns | At full temperature range |
| | 0.99 | 1.33 | 1.59 | ns | At -40°C to +85°C |
| Divide = 2 to 32 | 1.02 | 1.38 | 1.64 | ns | At full temperature range |
| | 1.04 | 1.38 | 1.64 | ns | At -40°C to +85°C |
| Variation with Temperature | | 0.9 | | ps/°C | |
| OUTPUT SKEW, LVDS OUTPUTS | | | | | |
| OUT3 to OUT4 on Same Device, t_{SKV}^2 | -85 | | +270 | ps | |
| All LVDS OUTs Across Multiple Devices, $t_{SKV_AB}^3$ | | | 450 | ps | |
| Same LVDS OUT Across Multiple Devices, $t_{SKV_AB}^3$ | | | 325 | ps | |
| CMOS | | | | | B outputs are inverted; termination = open |
| Output Rise Time, t_{RC} | | 681 | 865 | ps | 20% to 80%; $C_{LOAD} = 3$ pF |
| Output Fall Time, t_{FC} | | 646 | 992 | ps | 80% to 20%; $C_{LOAD} = 3$ pF |
| PROPAGATION DELAY, t_{CMOS} , CLK-TO-CMOS OUT ¹ | | | | | |
| Divide = Bypass | 1.0 | 1.39 | 1.71 | ns | At full temperature range |
| | 1.02 | 1.39 | 1.71 | ns | At -40°C to +85°C |
| Divide = 2 to 32 | 1.05 | 1.44 | 1.76 | ns | At full temperature range |
| | 1.07 | 1.44 | 1.76 | ns | At -40°C to +85°C |
| Variation with Temperature | | 1 | | ps/°C | |
| OUTPUT SKEW, CMOS OUTPUTS | | | | | |
| OUT3 to OUT4 on Same Device, t_{SKC}^2 | -140 | +145 | +300 | ps | |
| All CMOS OUT Across Multiple Devices, $t_{SKC_AB}^3$ | | | 650 | ps | |
| Same CMOS OUT Across Multiple Devices, $t_{SKC_AB}^3$ | | | 500 | ps | |
| LVPECL-TO-LVDS OUT | | | | | Everything the same; different logic type |
| Output Skew, t_{SKP_V} | 0.73 | 0.92 | 1.14 | ns | LVPECL to LVDS on same device |
| LVPECL-TO-CMOS OUT | | | | | Everything the same; different logic type |
| Output Skew, t_{SKP_C} | 0.87 | 1.14 | 1.43 | ns | LVPECL to CMOS on same device |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|------|--|
| LVDS-TO-CMOS OUT Output Skew, t_{skv_c} | 158 | 353 | 506 | ps | Everything the same; different logic type LVDS to CMOS on same device |

¹ The measurements are for CLK1. For CLK2, add approximately 25 ps.

² This is the difference between any two similar delay paths within a single device operating at the same voltage and temperature.

³ This is the difference between any two similar delay paths across multiple devices operating at the same voltage and temperature.

CLOCK OUTPUT PHASE NOISE

Table 4.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|-------------------------------------|-----|------|-----|--------|--------------------------|
| CLK1-TO-LVPECL ADDITIVE PHASE NOISE | | | | | Input slew rate > 1 V/ns |
| CLK1 = 622.08 MHz, OUT = 622.08 MHz | | | | | |
| Divide Ratio = 1 | | | | | |
| at 10 Hz Offset | | -125 | | dBc/Hz | |
| at 100 Hz Offset | | -132 | | dBc/Hz | |
| at 1 kHz Offset | | -140 | | dBc/Hz | |
| at 10 kHz Offset | | -148 | | dBc/Hz | |
| at 100 kHz Offset | | -153 | | dBc/Hz | |
| >1 MHz Offset | | -154 | | dBc/Hz | |
| CLK1 = 622.08 MHz, OUT = 155.52 MHz | | | | | |
| Divide Ratio = 4 | | | | | |
| at 10 Hz Offset | | -128 | | dBc/Hz | |
| at 100 Hz Offset | | -140 | | dBc/Hz | |
| at 1 kHz Offset | | -148 | | dBc/Hz | |
| at 10 kHz Offset | | -155 | | dBc/Hz | |
| at 100 kHz Offset | | -161 | | dBc/Hz | |
| >1 MHz Offset | | -161 | | dBc/Hz | |
| CLK1 = 622.08 MHz, OUT = 38.88 MHz | | | | | |
| Divide Ratio = 16 | | | | | |
| at 10 Hz Offset | | -135 | | dBc/Hz | |
| at 100 Hz Offset | | -145 | | dBc/Hz | |
| at 1 kHz Offset | | -158 | | dBc/Hz | |
| at 10 kHz Offset | | -165 | | dBc/Hz | |
| at 100 kHz Offset | | -165 | | dBc/Hz | |
| >1 MHz Offset | | -166 | | dBc/Hz | |
| CLK1 = 491.52 MHz, OUT = 61.44 MHz | | | | | |
| Divide Ratio = 8 | | | | | |
| at 10 Hz Offset | | -131 | | dBc/Hz | |
| at 100 Hz Offset | | -142 | | dBc/Hz | |
| at 1 kHz Offset | | -153 | | dBc/Hz | |
| at 10 kHz Offset | | -160 | | dBc/Hz | |
| at 100 kHz Offset | | -165 | | dBc/Hz | |
| >1 MHz Offset | | -165 | | dBc/Hz | |
| CLK1 = 491.52 MHz, OUT = 245.76 MHz | | | | | |
| Divide Ratio = 2 | | | | | |
| at 10 Hz Offset | | -125 | | dBc/Hz | |
| at 100 Hz Offset | | -132 | | dBc/Hz | |
| at 1 kHz Offset | | -140 | | dBc/Hz | |
| at 10 kHz Offset | | -151 | | dBc/Hz | |
| at 100 kHz Offset | | -157 | | dBc/Hz | |
| >1 MHz Offset | | -158 | | dBc/Hz | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|------|-----|--------|--------------------------|
| CLK1 = 245.76 MHz, OUT = 61.44 MHz Divide Ratio = 4 | | | | | |
| at 10 Hz Offset | | -138 | | dBc/Hz | |
| at 100 Hz Offset | | -144 | | dBc/Hz | |
| at 1 kHz Offset | | -154 | | dBc/Hz | |
| at 10 kHz Offset | | -163 | | dBc/Hz | |
| at 100 kHz Offset | | -164 | | dBc/Hz | |
| >1 MHz Offset | | -165 | | dBc/Hz | |
| CLK1-TO-LVDS ADDITIVE PHASE NOISE | | | | | |
| CLK1 = 622.08 MHz, OUT = 622.08 MHz Divide Ratio = 1 | | | | | |
| at 10 Hz Offset | | -100 | | dBc/Hz | |
| at 100 Hz Offset | | -110 | | dBc/Hz | |
| at 1 kHz Offset | | -118 | | dBc/Hz | |
| at 10 kHz Offset | | -129 | | dBc/Hz | |
| at 100 kHz Offset | | -135 | | dBc/Hz | |
| at 1 MHz Offset | | -140 | | dBc/Hz | |
| >10 MHz Offset | | -148 | | dBc/Hz | |
| CLK1 = 622.08 MHz, OUT = 155.52 MHz Divide Ratio = 4 | | | | | |
| at 10 Hz Offset | | -112 | | dBc/Hz | |
| at 100 Hz Offset | | -122 | | dBc/Hz | |
| at 1 kHz Offset | | -132 | | dBc/Hz | |
| at 10 kHz Offset | | -142 | | dBc/Hz | |
| at 100 kHz Offset | | -148 | | dBc/Hz | |
| at 1 MHz Offset | | -152 | | dBc/Hz | |
| >10 MHz Offset | | -155 | | dBc/Hz | |
| CLK1 = 491.52 MHz, OUT = 245.76 MHz Divide Ratio = 2 | | | | | |
| at 10 Hz Offset | | -108 | | dBc/Hz | |
| at 100 Hz Offset | | -118 | | dBc/Hz | |
| at 1 kHz Offset | | -128 | | dBc/Hz | |
| at 10 kHz Offset | | -138 | | dBc/Hz | |
| at 100 kHz Offset | | -145 | | dBc/Hz | |
| at 1 MHz Offset | | -148 | | dBc/Hz | |
| >10 MHz Offset | | -154 | | dBc/Hz | |
| CLK1 = 491.52 MHz, OUT = 122.88 MHz Divide Ratio = 4 | | | | | |
| at 10 Hz Offset | | -118 | | dBc/Hz | |
| at 100 Hz Offset | | -129 | | dBc/Hz | |
| at 1 kHz Offset | | -136 | | dBc/Hz | |
| at 10 kHz Offset | | -147 | | dBc/Hz | |
| at 100 kHz Offset | | -153 | | dBc/Hz | |
| t 1 MHz Offset | | -156 | | dBc/Hz | |
| >10 MHz Offset | | -158 | | dBc/Hz | |
| CLK1 = 245.76 MHz, OUT = 245.76 MHz Divide Ratio = 1 | | | | | |
| at 10 Hz Offset | | -108 | | dBc/Hz | |
| at 100 Hz Offset | | -118 | | dBc/Hz | |
| at 1 kHz Offset | | -128 | | dBc/Hz | |
| at 10 kHz Offset | | -138 | | dBc/Hz | |
| at 100 kHz Offset | | -145 | | dBc/Hz | |
| at 1 MHz Offset | | -148 | | dBc/Hz | |
| >10 MHz Offset | | -155 | | dBc/Hz | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|------|-----|--------|--------------------------|
| CLK1 = 245.76 MHz, OUT = 122.88 MHz Divide Ratio = 2 | | | | | |
| at 10 Hz Offset | | -118 | | dBc/Hz | |
| at 100 Hz Offset | | -127 | | dBc/Hz | |
| at 1 kHz Offset | | -137 | | dBc/Hz | |
| at 10 kHz Offset | | -147 | | dBc/Hz | |
| at 100 kHz Offset | | -154 | | dBc/Hz | |
| at 1 MHz Offset | | -156 | | dBc/Hz | |
| >10 MHz Offset | | -158 | | dBc/Hz | |
| CLK1-TO-CMOS ADDITIVE PHASE NOISE | | | | | |
| CLK1 = 245.76 MHz, OUT = 245.76 MHz | | | | | |
| Divide Ratio = 1 | | | | | |
| at 10 Hz Offset | | -110 | | dBc/Hz | |
| at 100 Hz Offset | | -121 | | dBc/Hz | |
| at 1 kHz Offset | | -130 | | dBc/Hz | |
| at 10 kHz Offset | | -140 | | dBc/Hz | |
| at 100 kHz Offset | | -145 | | dBc/Hz | |
| at 1 MHz Offset | | -149 | | dBc/Hz | |
| > 10 MHz Offset | | -156 | | dBc/Hz | |
| CLK1 = 245.76 MHz, OUT = 61.44 MHz | | | | | |
| Divide Ratio = 4 | | | | | |
| at 10 Hz Offset | | -122 | | dBc/Hz | |
| at 100 Hz Offset | | -132 | | dBc/Hz | |
| at 1 kHz Offset | | -143 | | dBc/Hz | |
| at 10 kHz Offset | | -152 | | dBc/Hz | |
| at 100 kHz Offset | | -158 | | dBc/Hz | |
| at 1 MHz Offset | | -160 | | dBc/Hz | |
| >10 MHz Offset | | -162 | | dBc/Hz | |
| CLK1 = 78.6432 MHz, OUT = 78.6432 MHz | | | | | |
| Divide Ratio = 1 | | | | | |
| at 10 Hz Offset | | -122 | | dBc/Hz | |
| at 100 Hz Offset | | -132 | | dBc/Hz | |
| at 1 kHz Offset | | -140 | | dBc/Hz | |
| at 10 kHz Offset | | -150 | | dBc/Hz | |
| at 100 kHz Offset | | -155 | | dBc/Hz | |
| at 1 MHz Offset | | -158 | | dBc/Hz | |
| >10 MHz Offset | | -160 | | dBc/Hz | |
| CLK1 = 78.6432 MHz, OUT = 39.3216 MHz | | | | | |
| Divide Ratio = 2 | | | | | |
| at 10 Hz Offset | | -128 | | dBc/Hz | |
| at 100 Hz Offset | | -136 | | dBc/Hz | |
| at 1 kHz Offset | | -146 | | dBc/Hz | |
| at 10 kHz Offset | | -155 | | dBc/Hz | |
| at 100 kHz Offset | | -161 | | dBc/Hz | |
| >1 MHz Offset | | -162 | | dBc/Hz | |

CLOCK OUTPUT ADDITIVE TIME JITTER

Table 5.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|--------|---|
| LVPECL OUTPUT ADDITIVE TIME JITTER | | | | | |
| CLK1 = 622.08 MHz Any LVPECL (OUT0 to OUT2) = 622.08 MHz Divide Ratio = 1 | | 40 | | fs rms | BW = 12 kHz to 20 MHz (OC-12) |
| CLK1 = 622.08 MHz Any LVPECL (OUT0 to OUT2) = 155.52 MHz Divide Ratio = 4 | | 55 | | fs rms | BW = 12 kHz to 20 MHz (OC-3) |
| CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 | | 215 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 100 MHz Both LVDS (OUT3, OUT4) = 100 MHz | | 215 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz Interferer(s) Interferer(s) |
| CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 100 MHz Both LVDS (OUT3, OUT4) = 100 MHz | | 222 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz Interferer(s) Interferer(s) |
| CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both LVDS (OUT3, OUT4) = 50 MHz | | 225 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz Interferer(s) Interferer(s) |
| CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both CMOS (OUT3, OUT4) = 50 MHz (B Outputs Off) | | 225 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz Interferer(s) Interferer(s) |
| CLK1 = 400 MHz Any LVPECL (OUT0 to OUT2) = 100 MHz Divide Ratio = 4 Other LVPECL = 50 MHz Both CMOS (OUT3, OUT4) = 50 MHz (B Outputs On) | | 225 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz Interferer(s) Interferer(s) |
| LVDS OUTPUT ADDITIVE TIME JITTER | | | | | |
| CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide Ratio = 4 | | 264 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| CLK1 = 400 MHz LVDS (OUT4) = 100 MHz Divide Ratio = 4 | | 319 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| CLK1 = 400 MHz LVDS (OUT3) = 100 MHz Divide Ratio = 4 LVDS (OUT4) = 50 MHz All LVPECL = 50 MHz | | 395 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz Interferer(s) Interferer(s) |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|--------|---|
| CLK1 = 400 MHz | | 395 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| LVDS (OUT4) = 100 MHz Divide Ratio = 4 LVDS (OUT3) = 50 MHz All LVPECL = 50 MHz | | | | | Interferer(s) Interferer(s) |
| CLK1 = 400 MHz | | 367 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| LVDS (OUT3) = 100 MHz Divide Ratio = 4 CMOS (OUT4) = 50 MHz (B Outputs Off) All LVPECL = 50 MHz | | | | | Interferer(s) Interferer(s) |
| CLK1 = 400 MHz | | 367 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| LVDS (OUT4) = 100 MHz Divide Ratio = 4 CMOS (OUT3) = 50 MHz (B Outputs Off) All LVPECL = 50 MHz | | | | | Interferer(s) Interferer(s) |
| CLK1 = 400 MHz | | 548 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| LVDS (OUT3) = 100 MHz Divide Ratio = 4 CMOS (OUT4) = 50 MHz (B Outputs On) All LVPECL = 50 MHz | | | | | Interferer(s) Interferer(s) |
| CLK1 = 400 MHz | | 548 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| LVDS (OUT4) = 100 MHz Divide Ratio = 4 CMOS (OUT3) = 50 MHz (B Outputs On) All LVPECL = 50 MHz | | | | | Interferer(s) Interferer(s) |
| CMOS OUTPUT ADDITIVE TIME JITTER | | | | | |
| CLK1 = 400 MHz | | 275 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| Both CMOS (OUT3, OUT4) = 100 MHz (B Output On) Divide Ratio = 4 | | | | | |
| CLK1 = 400 MHz | | 400 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| CMOS (OUT3) = 100 MHz (B Output On) Divide Ratio = 4 All LVPECL = 50 MHz LVDS (OUT4) = 50 MHz | | | | | Interferer(s) Interferer(s) |
| CLK1 = 400 MHz | | 374 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| CMOS (OUT3) = 100 MHz (B Output On) Divide Ratio = 4 All LVPECL = 50 MHz CMOS (OUT4) = 50 MHz (B Output Off) | | | | | Interferer(s) Interferer(s) |
| CLK1 = 400 MHz | | 555 | | fs rms | Calculated from SNR of ADC method; $f_c = 100$ MHz with $A_{IN} = 170$ MHz |
| CMOS (OUT3) = 100 MHz (B Output On) Divide Ratio = 4 All LVPECL = 50 MHz CMOS (OUT4) = 50 MHz (B Output On) | | | | | Interferer(s) Interferer(s) |

SERIAL CONTROL PORT

Table 6.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|---------|--|
| CSB, SCLK (INPUTS) | | | | | CSB and SCLK have 30 k Ω internal pull-down resistors |
| Input Logic 1 Voltage | 2.0 | | | V | |
| Input Logic 0 Voltage | | | 0.8 | V | |
| Input Logic 1 Current | | 110 | | μ A | |
| Input Logic 0 Current | | | 1 | μ A | |
| Input Capacitance | | 2 | | pF | |
| SDIO (WHEN INPUT) | | | | | |
| Input Logic 1 Voltage | 2.0 | | | V | |
| Input Logic 0 Voltage | | | 0.8 | V | |
| Input Logic 1 Current | | 10 | | nA | |
| Input Logic 0 Current | | 10 | | nA | |
| Input Capacitance | | 2 | | pF | |
| SDIO, SDO (OUTPUTS) | | | | | |
| Output Logic 1 Voltage | 2.7 | | | V | |
| Output Logic 0 Voltage | | | 0.4 | V | |
| TIMING | | | | | |
| Clock Rate (SCLK, 1/t _{SCLK}) | | | 25 | MHz | |
| Pulse Width High, t _{PWH} | 16 | | | ns | |
| Pulse Width Low, t _{PWL} | 16 | | | ns | |
| SDIO to SCLK Setup, t _{DS} | 2 | | | ns | |
| SCLK to SDIO Hold, t _{DH} | 1 | | | ns | |
| SCLK to Valid SDIO and SDO, t _{DV} | 6 | | | ns | |
| CSB to SCLK Setup and Hold, t _S , t _H | 2 | | | ns | |
| CSB Minimum Pulse Width High, t _{PWH} | 3 | | | ns | |

FUNCTION PIN

Table 7.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|-----------------------|-----|-----|-----|-------------------------|---|
| INPUT CHARACTERISTICS | | | | | The FUNCTION pin has a 30 k Ω internal pull-down resistor. This pin is normally held high. Do not let input float. |
| Logic 1 Voltage | 2.0 | | | V | |
| Logic 0 Voltage | | | 0.8 | V | |
| Logic 1 Current | | 110 | | μ A | |
| Logic 0 Current | | | 1 | μ A | |
| Capacitance | | 2 | | pF | |
| RESET TIMING | | | | | |
| Pulse Width Low | 50 | | | ns | |
| SYNC TIMING | | | | | |
| Pulse Width Low | 1.5 | | | High speed clock cycles | High speed clock is CLK1 or CLK2, whichever is being used for distribution. |

SYNC STATUS PIN

Table 8.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|----------------------------------|-----|-----|-----|------|--------------------------|
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage High (V_{OH}) | 2.7 | | | V | |
| Output Voltage Low (V_{OL}) | | | 0.4 | V | |

POWER

Table 9.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|------|---|
| POWER-UP DEFAULT MODE POWER DISSIPATION | | 550 | 600 | mW | Power-up default state; does not include power dissipated in output load resistors. No clock. |
| POWER DISSIPATION | | | 800 | mW | All outputs on. Three LVPECL outputs at 800 MHz, two CMOS out at 62 MHz (5 pF load). Does not include power dissipated in external resistors. |
| | | | 850 | mW | All outputs on. Three LVPECL outputs at 800 MHz, two CMOS out at 125 MHz (5 pF load). Does not include power dissipated in external resistors. |
| Full Sleep Power-Down | | 35 | 60 | mW | Maximum sleep is entered by setting 0x0A[1:0] = 01b and 0x58[4] = 1b. This powers off all band gap references. Does not include power dissipated in terminations. |
| Power-Down (PDB) | | 60 | 80 | mW | Set FUNCTION pin for PDB operation by setting 0x58[6:5] = 11b. Pull PDB low. Does not include power dissipated in terminations. |
| POWER DELTA | | | | | |
| CLK1, CLK2 Power-Down | 10 | 15 | 25 | mW | |
| Divider, DIV 2 to 32 to Bypass | 23 | 27 | 33 | mW | For each divider. |
| LVPECL Output Power-Down (PD2, PD3) | 50 | 65 | 75 | mW | For each output. Does not include dissipation in termination (PD2 only). |
| LVDS Output Power-Down | 80 | 92 | 110 | mW | For each output. |
| CMOS Output Power-Down (Static) | 56 | 70 | 85 | mW | For each output. Static (no clock). |
| CMOS Output Power-Down (Dynamic) | 115 | 150 | 190 | mW | For each CMOS output, single-ended. Clocking at 62 MHz with 5 pF load. |
| CMOS Output Power-Down (Dynamic) | 125 | 165 | 210 | mW | For each CMOS output, single-ended. Clocking at 125 MHz with 5 pF load. |

ABSOLUTE MAXIMUM RATINGS

Table 10.

| Parameter | With Respect to | Rating |
|------------------------------|-----------------|-------------------------|
| VS | GND | −0.3 V to +3.6 V |
| DSYNC/DSYNCB | GND | −0.3 V to $V_S + 0.3$ V |
| RSET | GND | −0.3 V to $V_S + 0.3$ V |
| CLK1, CLK1B, CLK2, CLK2B | GND | −0.3 V to $V_S + 0.3$ V |
| CLK1 | CLK1B | −1.2 V to +1.2 V |
| CLK2 | CLK2B | −1.2 V to +1.2 V |
| SCLK, SDIO, SDO, CSB | GND | −0.3 V to $V_S + 0.3$ V |
| OUT0, OUT1, OUT2, OUT3, OUT4 | GND | −0.3 V to $V_S + 0.3$ V |
| FUNCTION | GND | −0.3 V to $V_S + 0.3$ V |
| SYNC STATUS | GND | −0.3 V to $V_S + 0.3$ V |
| Junction Temperature | | 150°C |
| Storage Temperature Range | | −65°C to +150°C |
| Lead Temperature (10 sec) | | 300°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 11. Thermal Resistance¹

| Package Type | θ_{JA} | Unit |
|--------------|---------------|------|
| CP-48-13 | 28.5 | °C/W |

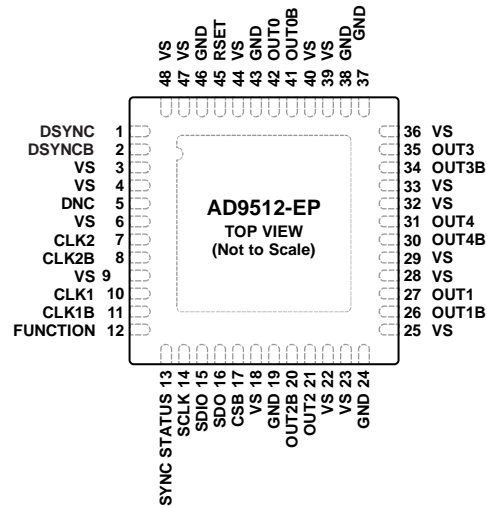
¹ Thermal impedance measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. DNC = DO NOT CONNECT TO THIS PIN.
 2. THE EXPOSED PADDLE ON THIS PACKAGE IS AN ELECTRICAL CONNECTION AS WELL AS A THERMAL ENHANCEMENT. FOR THE DEVICE TO FUNCTION PROPERLY, THE PADDLE MUST BE ATTACHED TO GROUND, GND.

Figure 2. Pin Configuration

Table 12. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|--|-------------|---|
| 1 | DSYNC | Detect Sync. Used for multichip synchronization. |
| 2 | DSYNCB | Detect Sync Complement. Used for multichip synchronization. |
| 3, 4, 6, 9, 18, 22, 23, 25, 28, 29, 32, 33, 36, 39, 40, 44, 47, 48 | VS | Power Supply (3.3 V). |
| 5 | DNC | Do Not Connect. Do not connect to this pin. |
| 7 | CLK2 | Clock Input. |
| 8 | CLK2B | Complementary Clock Input. Used in conjunction with CLK2. |
| 10 | CLK1 | Clock Input. |
| 11 | CLK1B | Complementary Clock Input. Used in conjunction with CLK1. |
| 12 | FUNCTION | Multipurpose Input. Can be programmed as a reset (RESETB), sync (SYNCB), or power-down (PDB) pin. |
| 13 | SYNC STATUS | Output Used to Monitor the Status of Multichip Synchronization. |
| 14 | SCLK | Serial Data Clock. |
| 15 | SDIO | Serial Data I/O. |
| 16 | SDO | Serial Data Output. |
| 17 | CSB | Serial Port Chip Select. |
| 19, 24, 37, 38, 43, 46 | GND | Ground. |
| 20 | OUT2B | Complementary LVPECL Output. |
| 21 | OUT2 | LVPECL Output. |
| 26 | OUT1B | Complementary LVPECL Output. |
| 27 | OUT1 | LVPECL Output. |
| 30 | OUT4B | Complementary LVDS/Inverted CMOS Output. |
| 31 | OUT4 | LVDS/CMOS Output. |
| 34 | OUT3B | Complementary LVDS/Inverted CMOS Output. |

| Pin No. | Mnemonic | Description |
|----------------|-----------------|---|
| 35 | OUT3 | LVDS/CMOS Output. |
| 41 | OUT0B | Complementary LVPECL Output. |
| 42 | OUT0 | LVPECL Output. |
| 45 | RSET | Current Set Resistor to Ground. Nominal value = 4.12 k Ω . |
| | EPAD | Exposed paddle. The exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground, GND. |

TYPICAL PERFORMANCE CHARACTERISTICS

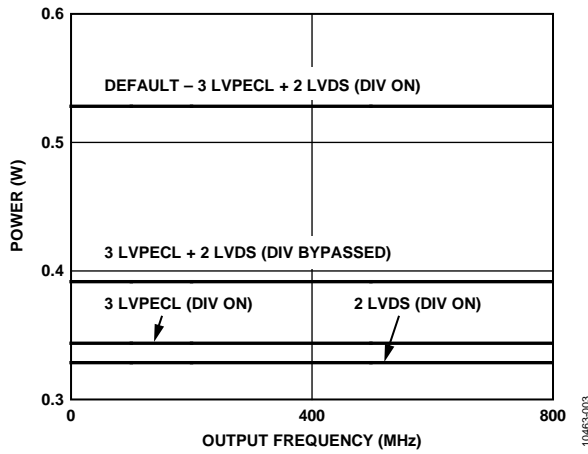


Figure 3. Power vs. Frequency—LVPECL, LVDS

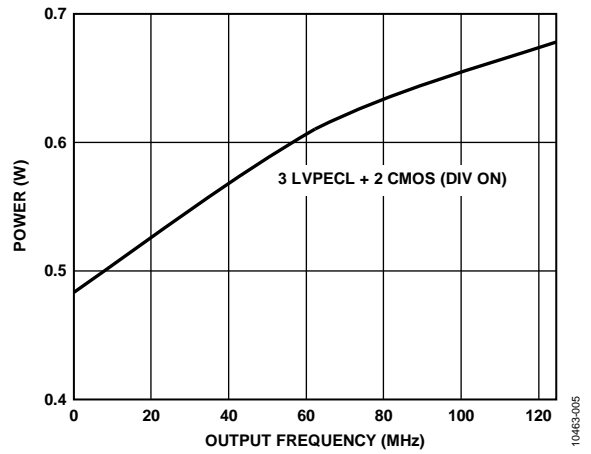


Figure 5. Power vs. Frequency—LVPECL, CMOS

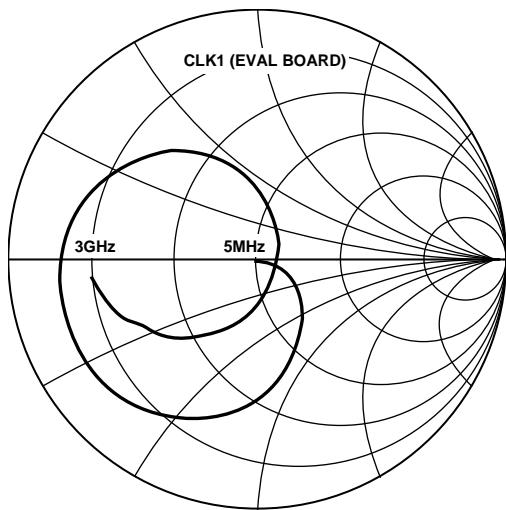


Figure 4. CLK1 Smith Chart (Evaluation Board)

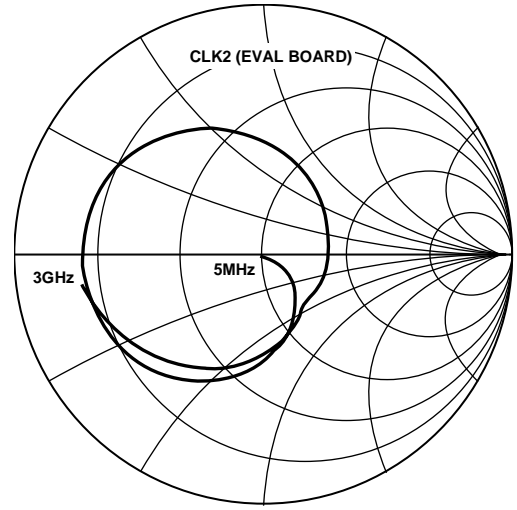


Figure 6. CLK2 Smith Chart (Evaluation Board)

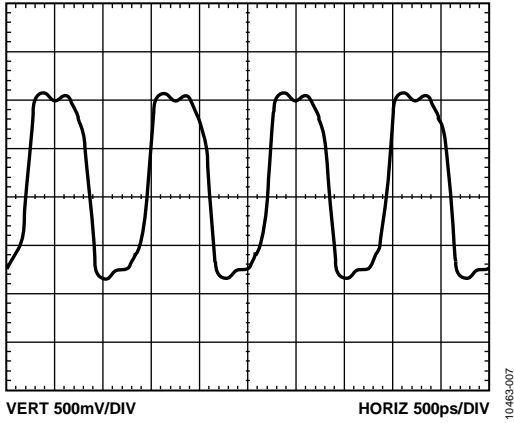


Figure 7. LVPECL Differential Output at 800 MHz

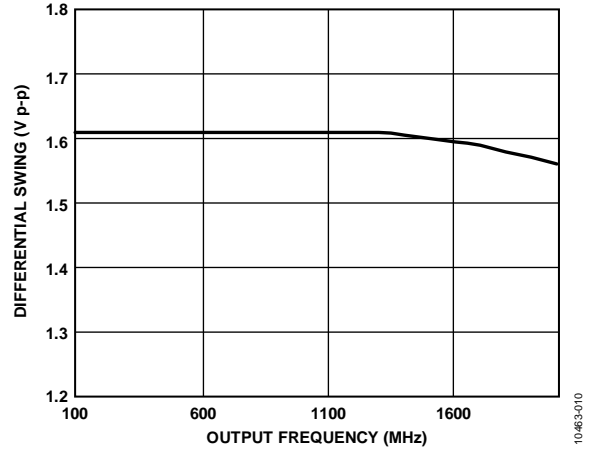


Figure 10. LVPECL Differential Output Swing vs. Frequency

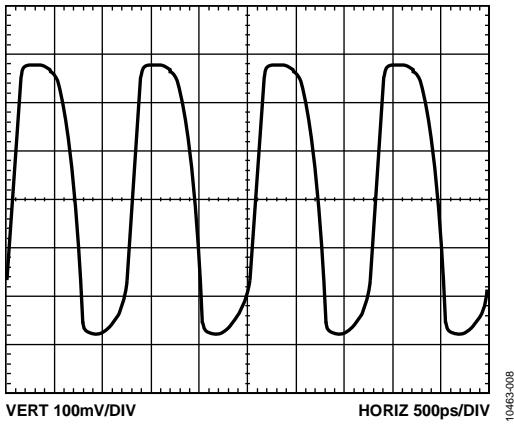


Figure 8. LVDS Differential Output at 800 MHz

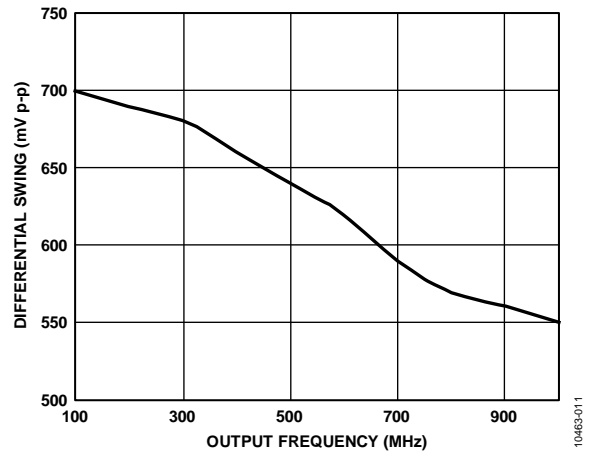


Figure 11. LVDS Differential Output Swing vs. Frequency

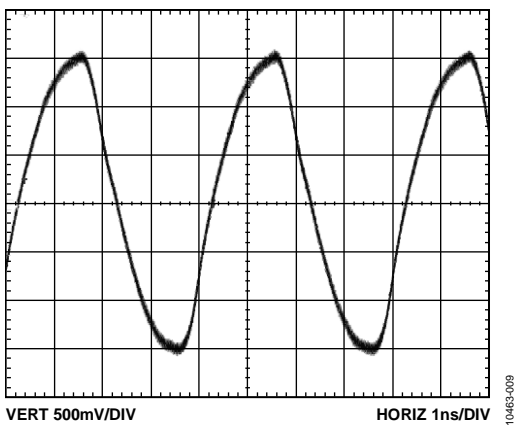


Figure 9. CMOS Single-Ended Output at 250 MHz with 10 pF Load

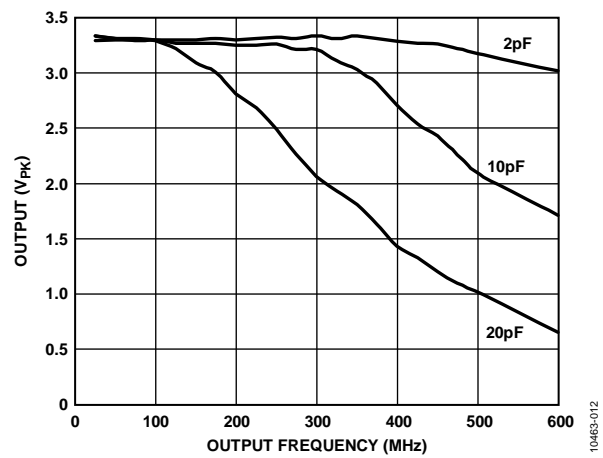


Figure 12. CMOS Single-Ended Output Swing vs. Frequency and Load

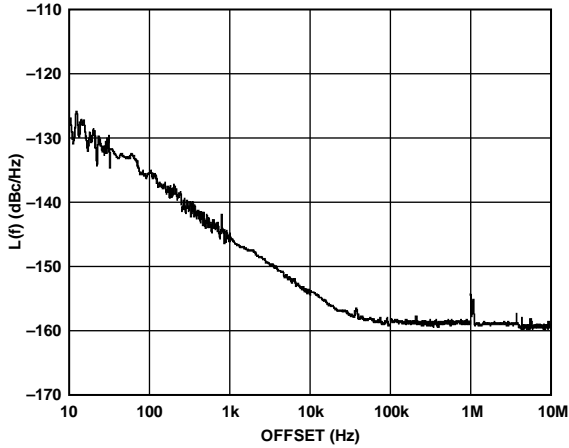


Figure 13. Additive Phase Noise—LVPECL DIV1, 245.76 MHz Distribution Section Only

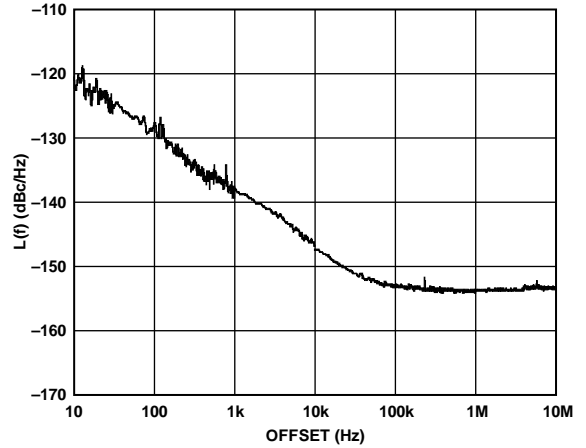


Figure 16. Additive Phase Noise—LVPECL DIV1, 622.08 MHz

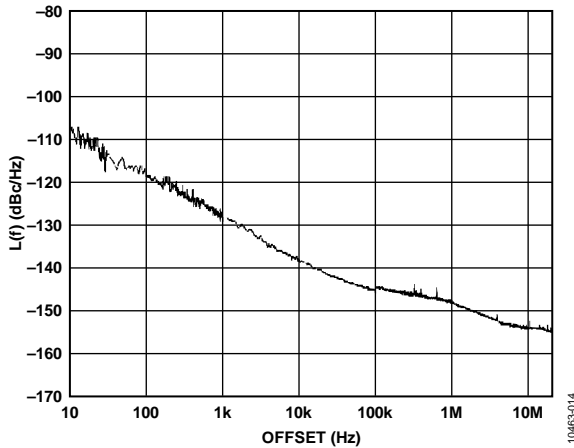


Figure 14. Additive Phase Noise—LVDS DIV1, 245.76 MHz

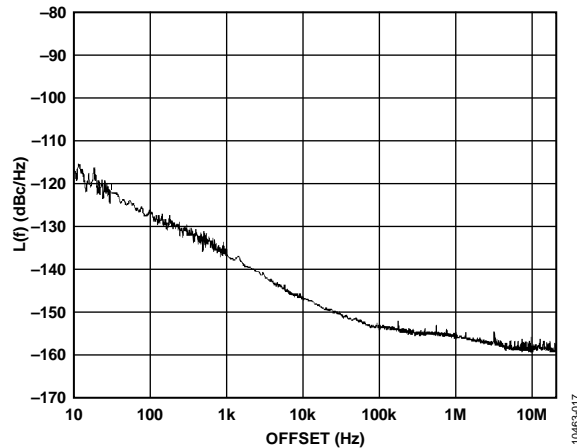


Figure 17. Additive Phase Noise—LVDS DIV2, 122.88 MHz

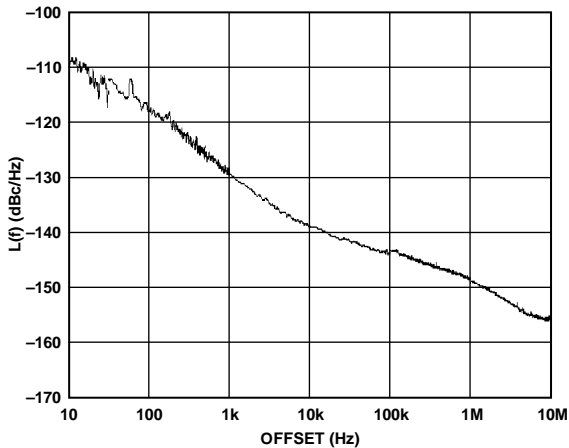


Figure 15. Additive Phase Noise—CMOS DIV1, 245.76 MHz

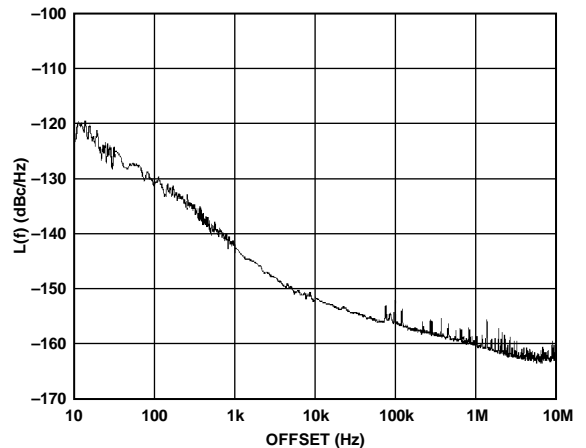


Figure 18. Additive Phase Noise—CMOS DIV4, 61.44 MHz

