



CYPRESS

B9940L

2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer

Features

- 200-MHz clock support
- LVPECL or LVCMOS/LVTTL clock input
- LVCMOS/LVTTL compatible inputs
- 18 clock outputs: drive up to 36 clock lines
- 150-ps max. output-to-output skew
- Dual- or single-supply operation:
 - 3.3V core and 3.3V outputs
 - 3.3V core and 2.5V outputs
 - 2.5V core and 2.5V outputs
- Pin-compatible with MPC940L
- Industrial temperature range: -40°C to 85°C
- 32-pin LQFP package

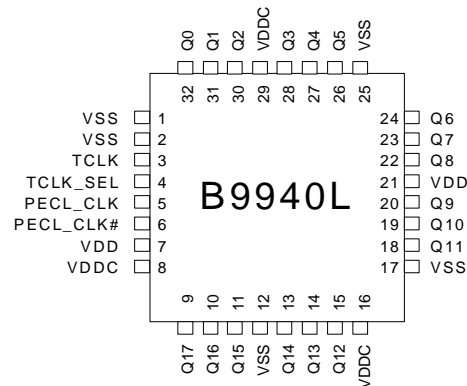
Description

The B9940L is a low-voltage clock distribution buffer with the capability to select either a differential LVPECL- or an LVCMOS/LVTTL-compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5V or 3.3V compatible and can drive two series-terminated 50Ω transmission lines. With this capability the B9940L has an effective fan-out of 1:36. Low output-to-output skews make the B9940L an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

Block Diagram



Pin Configuration



Pin Description^[1]

Pin	Name	PWR	I/O	Description
5	PECL_CLK		I, PU	PECL Input Clock
6	PECL_CLK#		I, PD	PECL Input Clock
3	TCLK		I, PD	External Reference/Test Clock Input
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDDC	O	Clock Outputs
4	TCLK_SEL		I, PD	Clock Select Input. When LOW, PECL clock is selected and when HIGH TCLK is selected.
8, 16, 29	VDDC			3.3V or 2.5V Power Supply for Output Clock Buffers
7, 21	VDD			3.3V or 2.5V Power Supply
1, 2, 12, 17, 25	VSS			Common Ground

Note:

1. PD = internal pull-down, PU = internal pull-up.

Maximum Ratings^[2]

Maximum Input Voltage Relative to V_{SS} : $V_{SS} - 0.3V$
 Maximum Input Voltage Relative to V_{DD} : $V_{DD} + 0.3V$
 Storage Temperature: $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature: $-40^{\circ}C$ to $+85^{\circ}C$
 Maximum ESD protection 2 kV
 Maximum Power Supply: 5.5V
 Maximum Input Current: ± 20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{DDC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All other inputs	V_{SS}	–	0.8	V
V_{IH}	Input High Voltage	All other inputs	2.0	–	V_{DD}	V
I_{IL}	Input Low Current ^[3]		–	–	–200	μA
I_{IH}	Input High Current ^[3]		–	–	200	μA
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		500	–	1000	mV
V_{CMR}	Common Mode Range ^[4] PECL_CLK	$V_{DD} = 3.3V$	$V_{DD} - 1.4$	–	$V_{DD} - 0.6$	V
		$V_{DD} = 2.5V$	$V_{DD} - 1.0$	–	$V_{DD} - 0.6$	V
V_{OL}	Output Low Voltage ^[5]	$I_{OL} = 20$ mA	–	–	0.5	V
V_{OH}	Output High Voltage ^[5]	$I_{OH} = -20$ mA, $V_{DDC} = 3.3V$	2.4	–	–	V
		$I_{OH} = -20$ mA, $V_{DDC} = 2.5V$	1.8	–	–	V
I_{DDQ}	Quiescent Supply Current		–	2	5	mA
Z_{out}	Output Impedance	$V_{DD} = 3.3V$	9	14	19	Ω
		$V_{DD} = 2.5V$	11	18	26	
C_{in}	Input Capacitance		–	4	–	pF

AC Parameters $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{DDC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$ ^[6]

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{max}	Maximum Input Frequency		–	–	200	MHz
t_{PD}	PECL_CLK to Q Delay ^[7, 9]	$V_{DD} = 3.3V$	2.0	3.5	4.0	ns
		$V_{DD} = 2.5V$	2.6	4.0	5.2	
t_{PD}	TTL_CLK to Q Delay ^[7, 9]	$V_{DD} = 3.3V$	1.8	3.3	3.8	ns
		$V_{DD} = 2.5V$	2.3	3.8	4.4	
F_{outDC}	Output Duty Cycle ^[7, 8, 9]	Measured at $V_{DD}/2$	45	–	55	%
T_{skew}	Output-to-Output Skew ^[7, 9]	$V_{DD} = 3.3V$, $F_{in} = 150$ MHz	–	–	150	ps
		$V_{DD} = 2.5V$, $F_{in} = 150$ MHz	–	–	200	
$T_{skew(pp)}$	Part-to-Part Skew ^[10]	PECL, $V_{DDC} = 3.3V$	–	–	1.4	ns
		PECL, $V_{DDC} = 2.5V$	–	–	2.2	

Notes:

- The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power suppl sequencing is NOT required.
- Inputs have pull-up/pull-down resistors that effect input current.
- The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
- Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.
- Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
- Outputs driving 50 Ω transmission lines.
- 50% input duty cycle.
- Outputs loaded with 30 pF each.
- Across temperature and voltage ranges, includes output skew.

Document History Page

Document Title: B9940L 2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer				
Document Number: 38-07105				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107509	06/14/01	NDP	Convert from IMI to Cypress
*A	116093	09/09/02	HWT	Converted from Word Doc to Framemaker Corrected the Ordering Information to match the DevMaster Corrected Output Impedance Type to 9/11,14/18, and 19/26 in DC parameters
*B	120824	11/21/02	RGL	Corrected minor typo
*C	122783	12/26/02	RBI	Add power up requirements to maximum ratings information