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## High Speed Translator Inverting Buffer to LVCMOS

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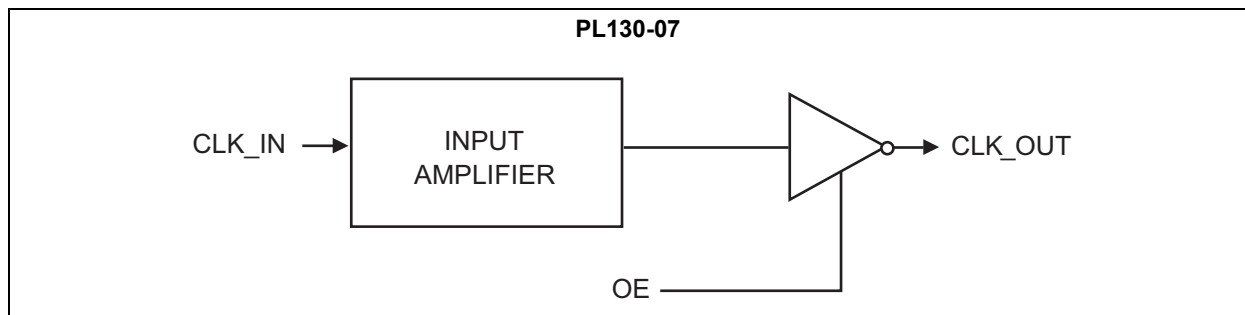
### Features

- LVCMOS Output
- Selectable Drive Capability
  - Drive 15 pF or 30 pF Output Load
- Single AC-Coupled Input (Min. 100 mV Swing)
- Accepts LVCMOS or Sine Wave Inputs
- Input Range from 10 MHz to 200 MHz
- OE High (PL130-07) or OE Low (PL130-07A) Enable
- 2.5V to 3.3V Operation
- Available in 8-Pin SOIC, 8-Pin TSSOP and 3 mm x 3 mm 16-Pin QFN

### General Description

The PL130-07 is a low cost, high performance, high speed, inverting buffer that reproduces any input frequency from 10 MHz to 200 MHz. It provides an LVCMOS output with 15 pF output load drive capability. Any input signal with at least 100 mV swing can be used as reference signal. This chip is ideal for conversion from sine wave to LVCMOS.

### Block Diagram



# PL130-07

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## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage ( $V_{DD}$ ) .....	+4.6V
Input Voltage (DC).....	-0.5V to $V_{DD} + 0.5V$
Output Voltage (DC).....	-0.5V to $V_{DD} + 0.5V$
HBM ESD Rating.....	2 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: AC ELECTRICAL CHARACTERISTICS**

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Frequency	—	10	—	200	MHz	—
Input Signal Swing	—	100	—	—	mV	CLK_IN Input
Output Frequency	—	10	—	200	MHz	—

**TABLE 1-2: CMOS OUTPUT ELECTRICAL CHARACTERISTICS**

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = 12\text{ mA}$
Output Low Voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 12\text{ mA}$
Output High Voltage at CMOS Level	$V_{OHC}$	$V_{DD} - 0.4$	—	—	V	$I_{OH} = -4\text{ mA}$
Output Drive Current	—	36	51	—	mA	At TTL Level (High Drive), <a href="#">Note 1</a>
		12	17	—	mA	At TTL Level (Standard Drive)
Quiescent Supply Current	$I_{DD}$	—	5.9	—	mA	No input signal, $V_{DD} = 2.5\text{V}$
		—	12.7	—	mA	No input signal, $V_{DD} = 3.3\text{V}$

**Note 1:** High Drive CMOS is selectable through DRIV\_SEL selector input on pin 8(SOIC) or 13(QFN).

**TABLE 1-3: CMOS SWITCHING CHARACTERISTICS**

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Clock Rise/Fall Time	$t_r/t_f$	—	1.15	—	ns	0.8V ~ 2.0V with 10 pF load
		—	3.7	—	ns	0.8V ~ 3.0V with 15 pF load
Output Clock Rise/Fall Time (High Drive, <a href="#">Note 1</a> )	$t_r/t_f$	—	0.5	—	ns	0.8V ~ 2.0V with 10 pF load
		—	1.5	—	ns	0.8V ~ 3.0V with 15 pF load

**Note 1:** High Drive CMOS is selectable through DRIV\_SEL selector input on pin 8(SOIC) or 13(QFN).

## TEMPERATURE SPECIFICATIONS (Note 1)

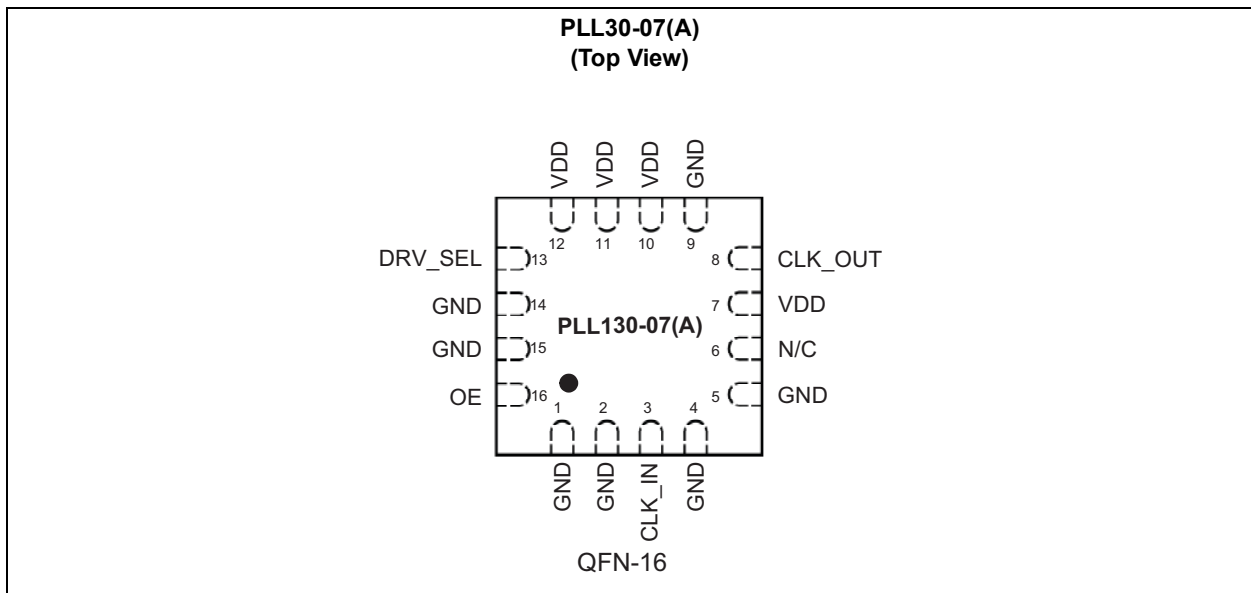
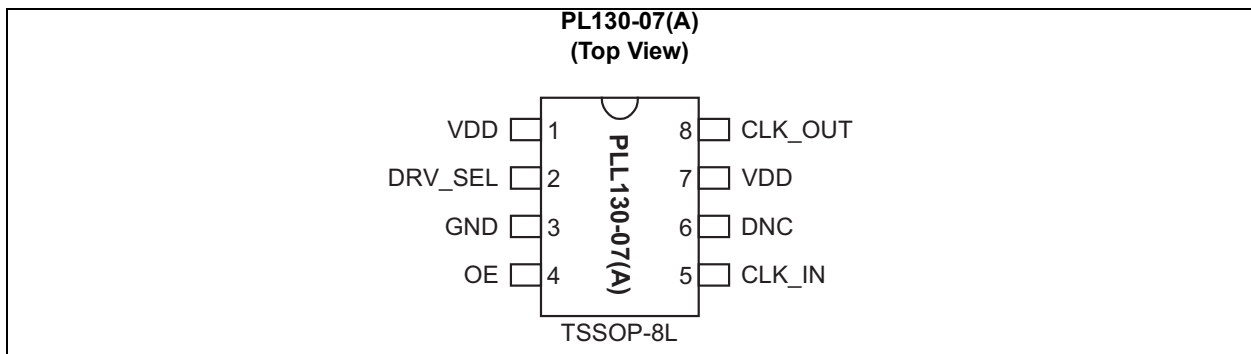
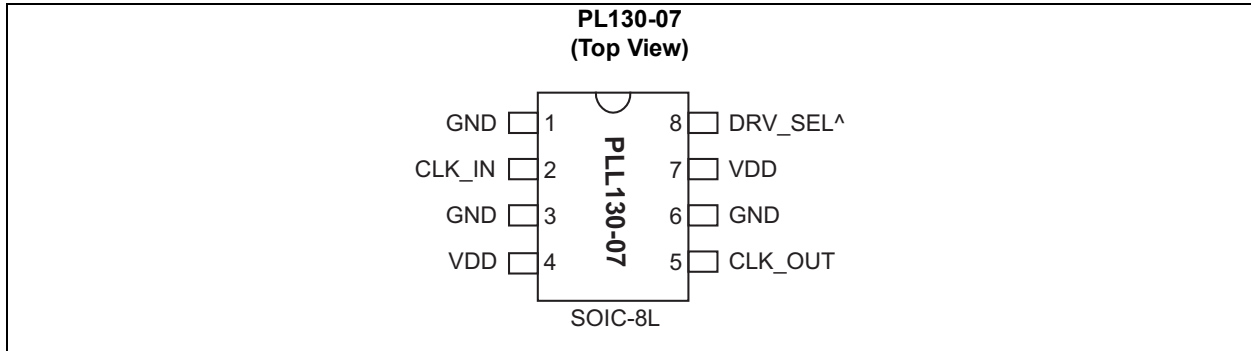
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Storage Temperature Range	$T_S$	-65	—	+150	°C	—
Ambient Operating Temperature	$T_A$	-40	—	+85	°C	Note 2
Junction Temperature	$T_J$	—	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 seconds

- Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e.,  $T_A$ ,  $T_J$ ,  $\theta_{JA}$ ). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.
- 2:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

### Pin Configurations



# PL130-07

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Name	SOIC-8L	TSSOP-8L	QFN-16L	Type	Description
GND	1, 3, 6	3	1, 2, 4, 5, 9, 14, 15	P	Ground.
V <sub>DD</sub>	4, 7	1, 7	7, 10, 11, 12	P	Power supply.
DRV_SEL	8	2	13	I	Drive Select input: '1' for standard drive, '0' for high drive output. Internal pull-up (default is '1').
CLK_IN	2	5	3	I	Clock input signal. The frequency of this signal will be reproduced at the output (after translation to CMOS level).
CLK_OUT	5	8	8	O	CMOS clock output.
OE	N/A	4	16	I	Output Enable. See <a href="#">Table 2-2</a> .

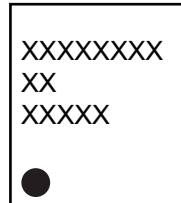
**TABLE 2-2: OE LOGIC TABLE**

Part Number	OE State	Output Buffer State
PL130-07	0	Tri-State
	1 (default)	Active
PL130-07A	0 (default)	Active
	1	Tri-State

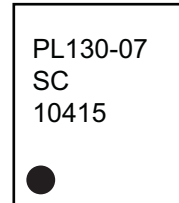
## 3.0 PACKAGING INFORMATION

### 3.1 Package Marking Information

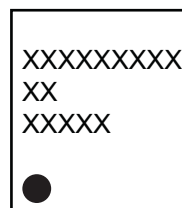
8-Lead SOIC\*



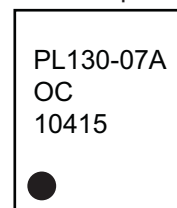
Example



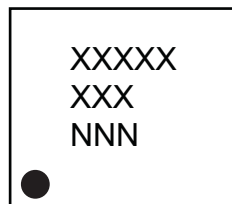
8-Lead TSSOP\*



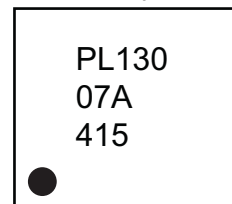
Example



16-Lead QFN\*



Example



<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar ( \_ ) and/or Overbar ( ¯ ) symbol may not be to scale.

# PL130-07

## 4.0 PACKAGING INFORMATION

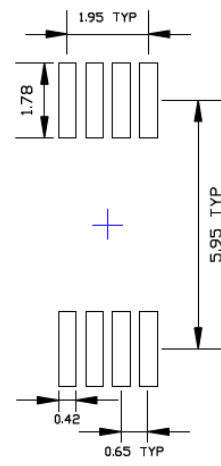
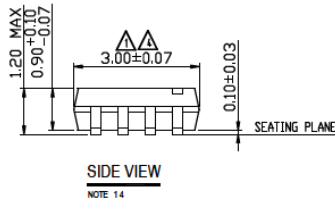
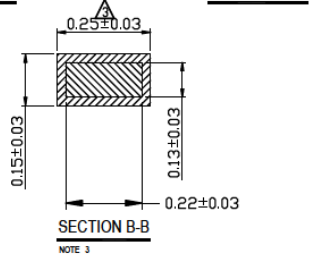
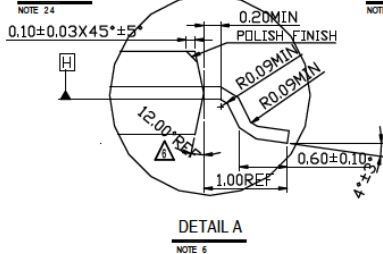
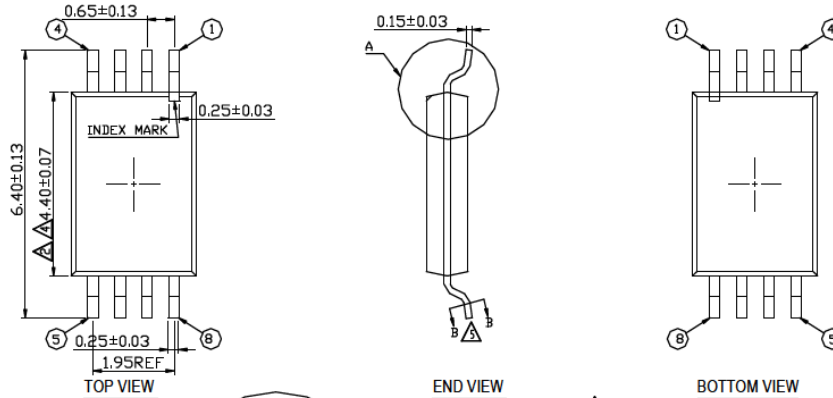
### 8-Lead TSSOP Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

**TITLE**

8 LEAD TSSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSSOP-8LD-PL-1	UNIT	MM
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- NOTE:**
- ⚠ DIMENSION (3.00±0.07) DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
  - ⚠ DIMENSION (4.40±0.07) DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
  - ⚠ DIMENSION (0.25±0.03) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE (0.25±0.03) DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07mm.
  - ⚠ DIMENSIONS (3.00±0.07) AND (4.40±0.07) TO BE DETERMINED AT DATUM PLANE H.
  - ⚠ CROSS SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25mm FROM THE LEAD TIP.
  - ⚠ PACKAGE EDGE ANGLES (8 X FOR 4 SIDES EACH FOR TOP & BOTTOM).



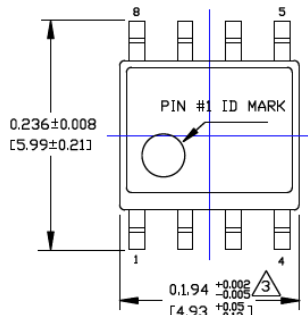
## 8-Lead SOIC Package Outline and Recommended Land Pattern

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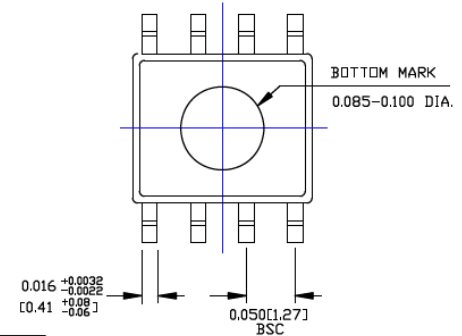
**TITLE**

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

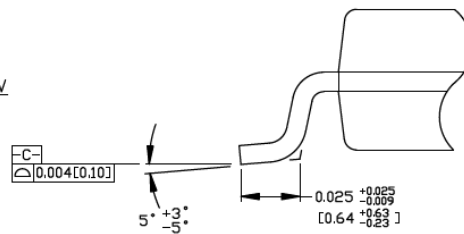
DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]
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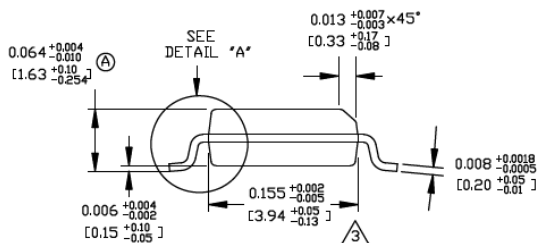
TOP VIEW



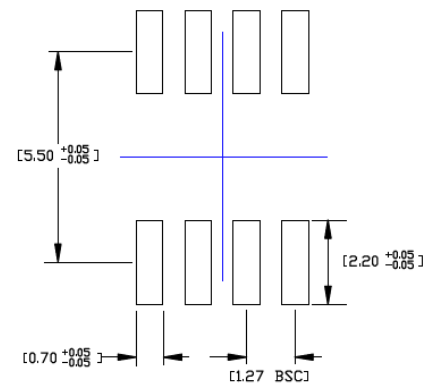
BOTTOM VIEW



DETAIL "A"



END VIEW



RECOMMENDED LAND PATTERN

- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
  2. CONTROLLING DIMENSION: INCHES.
- ⚠ DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

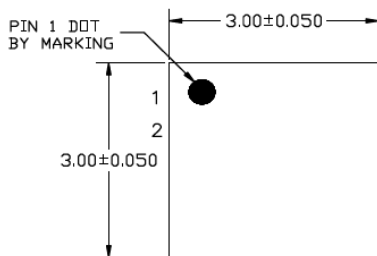
# PL130-07

## 16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

### TITLE

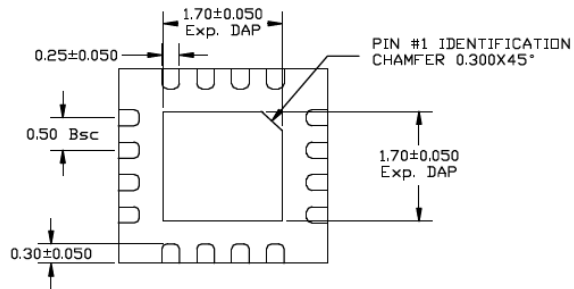
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN33-16LD-PL-3	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu



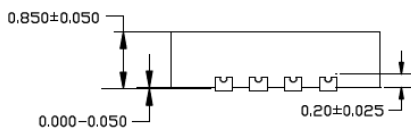
TOP VIEW

NOTE: 1, 2, 3



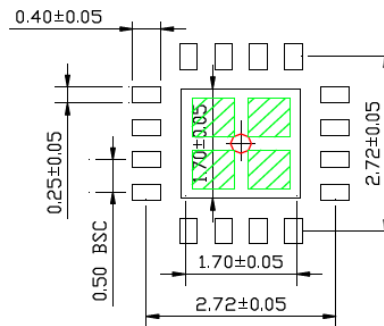
BOTTOM VIEW

NOTE: 1, 2, 3



SIDE VIEW

NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN

NOTE: 4, 5

### NOTE:

1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60mm IN SIZE, 0.20mm SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## APPENDIX A: REVISION HISTORY

### Revision A (July 2016)

- Converted Micrel document PL130-07 to Microchip data sheet DS20005598A.
- Minor text changes throughout.

### Revision B (September 2020)

- Added the word “Inverting” to the data sheet title and updated the [Block Diagram](#).

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	X	X	X	X
Device	OE State	Package Type	Temperature	Media Type
<b>Device:</b>	PL130-07:	High Speed Translator Inverting Buffer to LVC MOS		
<b>OE State:</b>	(blank) = High Enable A = Low Enable			
<b>Package Type:</b>	O = TSSOP-8L Q = QFN-16L S = SOIC-8L			
<b>Temperature</b>	C = Commercial Temperature Range I = Industrial Temperature Range			
<b>Media Type</b>	(blank) = Tube R = Tape & Reel			
<b>Examples:</b>				
a)	PL130-07OC:	High Speed Translator Inverting Buffer to LVC MOS, High Enable, TSSOP-8L, Commercial Temp. Range, Tube		
b)	PL130-07OC-R:	High Speed Translator Inverting Buffer to LVC MOS, High Enable, TSSOP-8L, Commercial Temp. Range, Tape & Reel		
c)	PL130-07AOI:	High Speed Translator Inverting Buffer to LVC MOS, Low Enable, TSSOP-8L, Industrial Temp. Range, Tube		
d)	PL130-07AQI-R:	High Speed Translator Buffer to LVC MOS, Low Enable, QFN-16L, Industrial Temp. Range, Tape & Reel		
e)	PL130-07SC:	High Speed Translator Inverting Buffer to LVC MOS, High Enable, SOIC-8L, Commercial		

NOTES:

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