

## FEATURES/BENEFITS

- Pin and function compatible to the 74F373, 74FCT373 and 74ABT373
- Industrial temperature  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- CMOS power levels:  $<7.5\text{mW}$  static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

### FCT-T 373T

- JEDEC-FCT spec compatible
- Std., A, C, and D speed grades with 3.7ns for D
- $I_{OL} = 48\text{mA}$  Ind., 32mA Mil.

### FCT-T 2373T

- Built-in  $25\Omega$  series resistor outputs reduce reflection and other system noise
- Std., C and D speed grades with 3.7ns for D
- $I_{OL} = 12\text{mA}$  Ind.

## DESCRIPTION

The QSFCT373T is an 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2373 is a  $25\Omega$  resistor output version useful for driving transmission lines and reducing system noise. The 2373 series parts can replace 373 devices in existing designs to reduce noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

**Figure 1. Functional Block Diagram**

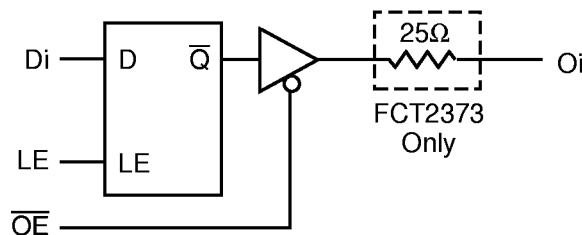


Figure 2. Pin Configurations (All Pins Top View)

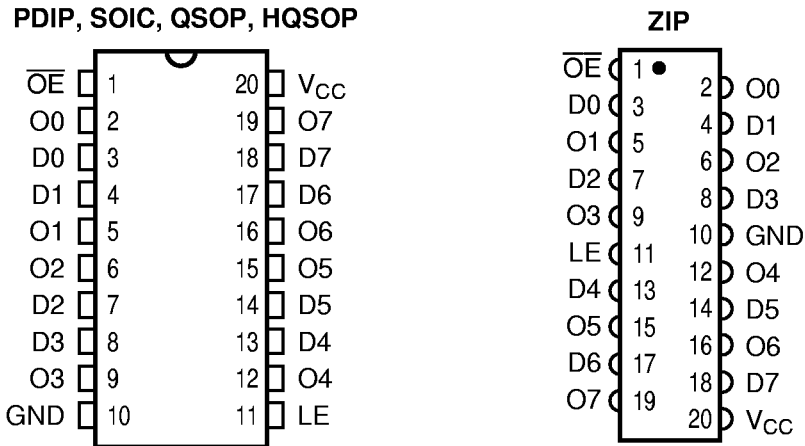


Table 1. Pin Description

| Name            | I/O | Description   |
|-----------------|-----|---------------|
| Di              | I   | Data Inputs   |
| O <sub>i</sub>  | O   | Data Outputs  |
| LE              | I   | Latch Enable  |
| $\overline{OE}$ | I   | Output Enable |

Table 2. Function Table

| $\overline{OE}$ | Inputs<br>LE | Di | Internal<br>Q<br>Value | Outputs<br>O <sub>i</sub> | Function        |
|-----------------|--------------|----|------------------------|---------------------------|-----------------|
| H               | X            | X  | X                      | Hi-Z                      | Disable Outputs |
| L               | L            | X  | H                      | H                         | Enable Outputs  |
| L               | L            | X  | L                      | L                         |                 |
| L               | H            | L  | L                      | L                         | Pass Inputs     |
| L               | H            | H  | H                      | H                         |                 |
| L               | L            | X  | Q                      | Q                         | Hold Prior Data |

**Table 3. Absolute Maximum Ratings**

|   |               |
|---|---------------|
| Supply Voltage to Ground .....                          | -0.5V to 7.0V |
| DC Output Voltage $V_{OUT}$ .....                       | -0.5V to 7.0V |
| DC Input Voltage $V_{IN}$ .....                         | -0.5V to 7.0V |
| AC Input Voltage (for a pulse width $\leq 20$ ns) ..... | -3.0V         |
| DC Input Diode Current with $V_{IN} < 0$ .....          | -20mA         |
| DC Output Diode Current with $V_{OUT} < 0$ .....        | -50mA         |
| DC Output Current Max. Sink Current/Pin .....           | 120mA         |
| Maximum Power Dissipation .....                         | 0.5 watts     |
| $T_{STG}$ Storage Temperature .....                     | -65° to 150°C |

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**Table 4. Capacitance<sup>(1)</sup>**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

| Pins <sup>(2)</sup>               | SOIC | QSOP | PDIP | ZIP | Unit |
|-----------------------------------|------|------|------|-----|------|
| 1, 3, 4, 7, 8, 11, 13, 14, 17, 18 | 4    | 4    | 5    | 7   | pF   |
| 2, 5, 6, 9, 12, 15, 16, 19        | 8    | 8    | 9    | 10  | pF   |

**Notes:**

1. Capacitance is characterized but not tested.
2. Pin reference for 20-pin package.

**Table 5. Power Supply Characteristics**

| Symbol          | Parameter                           | Test Conditions <sup>(1)</sup>   | Min | Max  | Unit       |
|-----------------|-------------------------------------|--|-----|------|------------|
| $I_{CC}$        | Quiescent Power Supply Current      | $V_{CC} = \text{Max.}$ , $\text{freq} = 0$<br>$0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$ | —   | 1.5  | mA         |
| $\Delta I_{CC}$ | Supply Current per Input @ TTL HIGH | $V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , $\text{freq} = 0^{(2)}$  | —   | 2.0  | mA         |
| $Q_{CCD}$       | Supply Current per Input per MHz    | $V_{CC} = \text{Max.}$ , Outputs Open and Enabled<br>One Bit Toggling @ 50% Duty Cycle<br>Other Inputs at GND or $V_{CC}^{(3,4)}$      | —   | 0.25 | mA/<br>MHz |

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

**Table 6. DC Electrical Characteristics Over Operating Range**

Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol                   | Parameter                                      | Test Conditions  | Min        | Typ <sup>(1)</sup> | Max          | Unit          |
|--------------------------|--|--|------------|--------------------|--------------|---------------|
| $V_{IH}$                 | Input HIGH Voltage                             | Logic HIGH for All Inputs  | 2.0        | —                  | —            | V             |
| $V_{IL}$                 | Input LOW Voltage                              | Logic LOW for All Inputs   | —          | —                  | 0.8          | V             |
| $\Delta V_T$             | Input Hysteresis                               | $V_{TLH} - V_{THL}$ for All Inputs   | —          | 0.2                | —            | V             |
| $ I_{IH} $<br>$ I_{IL} $ | Input Current<br>Input HIGH or LOW             | $V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$   | —          | —                  | 5            | $\mu\text{A}$ |
| $ I_{OZ} $               | Off-State Output<br>Current (Hi-Z)             | $V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$  | —          | —                  | 5            | $\mu\text{A}$ |
| $I_{OS}$                 | Short Circuit Current<br>(FCT373)              | $V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$                                     | -60        | —                  | —            | mA            |
| $I_{OR}$                 | Current Drive<br>(FCT2373 – 25 $\Omega$ )      | $V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(3)}$                                      | 50         | —                  | —            | mA            |
| $V_{IC}$                 | Input Clamp Voltage                            | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^\circ\text{C}^{(3)}$              | —          | -0.7               | -1.2         | V             |
| $V_{OH}$                 | Output HIGH Voltage                            | $V_{CC} = \text{Min.}$<br>$I_{OH} = -12\text{mA}$ (MIL)<br>$I_{OH} = -15\text{mA}$ (IND) | 2.4<br>2.4 | —<br>—             | —<br>—       | V             |
| $V_{OL}$                 | Output LOW Voltage<br>(FCT373)                 | $V_{CC} = \text{Min.}$<br>$I_{OL} = 32\text{mA}$ (MIL)<br>$I_{OL} = 48\text{mA}$ (IND)   | —<br>—     | —<br>—             | 0.50<br>0.50 | V             |
| VOL                      | Output LOW Voltage<br>(FCT2373 – 25 $\Omega$ ) | $V_{CC} = \text{Min.}$<br>$I_{OL} = 12\text{mA}$ (MIL)<br>$I_{OL} = 12\text{mA}$ (IND)   | —<br>—     | —<br>—             | 0.50<br>0.50 | V             |
| $R_{OUT}$                | Output Resistance<br>(FCT2373 – 25 $\Omega$ )  | $V_{CC} = \text{Min.}$<br>$I_{OL} = 12\text{mA}$ (MIL)<br>$I_{OL} = 12\text{mA}$ (IND)   | —<br>20    | 25<br>28           | —<br>40      | $\Omega$      |

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**QS54/74FCT373T, 2373T**

**Table 7. Switching Characteristics Over Operating Range**

Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$       Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$   
 $C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

| Symbol                 | Description <sup>(1)</sup>                        |  | 373<br>2373 |            | 373A<br>2373A |            | 373C<br>2373C |            | 373D<br>2373D |          | Unit |
|------------------------|---|--|-------------|------------|---------------|------------|---------------|------------|---------------|----------|------|
|                        |   |  | Min         | Max        | Min           | Max        | Min           | Max        | Min           | Max      |      |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>Data to Oi, 373              | IND<br>MIL                               | 1.5<br>2    | 8<br>8.5   | 1.5<br>1.5    | 5.2<br>5.6 | 1.5<br>1.5    | 4.2<br>5.1 | 1.5<br>—      | 3.7<br>— | ns   |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>Data to Oi, 2373             | IND<br>MIL                               | 1.5<br>2    | 8<br>8.5   | 1.5<br>1.5    | 5.2<br>5.6 | 1.5<br>1.5    | 4.2<br>5.1 | 1.5<br>—      | 3.7<br>— | ns   |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>LE to Oi, 373                | IND<br>MIL                               | 2<br>2      | 13<br>14   | 2<br>2        | 8.5<br>9.8 | 2<br>2        | 5.5<br>8   | 2<br>—        | 4.9<br>— | ns   |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>LE to Oi, 2373               | IND<br>MIL                               | 2<br>2      | 13<br>14   | 2<br>2        | 8.5<br>9.8 | 2<br>2        | 5.5<br>8   | 2<br>—        | 4.9<br>— | ns   |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>$\overline{OE}$ to Yi, 373  | IND<br>MIL                               | 1.5<br>1.5  | 11<br>12.5 | 1.5<br>1.5    | 6.5<br>7.5 | 1.5<br>1.5    | 5.5<br>6.3 | 1.5<br>—      | 5.5<br>— | ns   |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>$\overline{OE}$ to Yi, 2373 | IND<br>MIL                               | 1.5<br>1.5  | 11<br>12.5 | 1.5<br>1.5    | 6.5<br>7.5 | 1.5<br>1.5    | 6.2<br>7.2 | 1.5<br>—      | 6.2<br>— | ns   |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>$\overline{OE}$ to Yi      | IND <sup>(2)</sup><br>MIL <sup>(2)</sup> | 1.5<br>1.5  | 7<br>8.5   | 1.5<br>1.5    | 5.5<br>6.5 | 1.5<br>1.5    | 5.0<br>5.9 | 1.5<br>—      | 5.0<br>— | ns   |
| $t_S$                  | Data Setup Time                                   | IND<br>MIL                               | 2<br>2      | —<br>—     | 2<br>2        | —<br>—     | 2<br>2        | —<br>—     | 2<br>—        | —<br>—   | ns   |
| $t_H$                  | Data Hold Time                                    | IND<br>MIL                               | 1.5<br>1.5  | —<br>—     | 1.5<br>1.5    | —<br>—     | 1.5<br>1.5    | —<br>—     | 1.5<br>—      | —<br>—   | ns   |
| $t_W$                  | LE Pulse Width<br>HIGH or LOW                     | IND <sup>(2)</sup><br>MIL <sup>(2)</sup> | 6<br>6      | —<br>—     | 5<br>6        | —<br>—     | 4<br>6        | —<br>—     | 4<br>—        | —<br>—   | ns   |

**Notes:**

1. Minimums guaranteed but not tested for all parameters except  $t_S$  and  $t_H$ .
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.