

## 74VHC541 Octal Buffer/Line Driver with 3-STATE Outputs

### General Description

The VHC541 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

This device is similar in function to the VHC244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

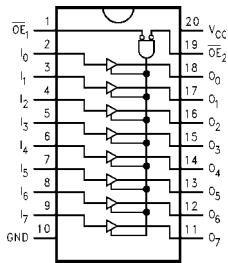
- High Speed:  $t_{PD} = 3.5 \text{ ns}$  (typ) at  $V_{CC} = 5V$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A}$  (max) at  $T_A = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Power down protection is provided on all inputs
- Low noise:  $V_{OLP} = 0.9V$  (typ)
- Pin and function compatible with 74HC541

### Ordering Code:

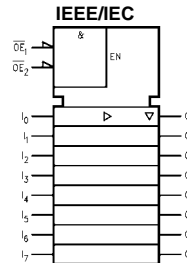
Order Number	Package Number	Package Description
74VHC541M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC541SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC541N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

### Connection Diagram



### Logic Symbol



### Pin Descriptions

Pin Names	Descriptions
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0 - I_7$	Inputs
$O_0 - O_7$	3-STATE Outputs

### Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current ( $I_{OK}$ )	$\pm 20$ mA
DC Output Current ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}/GND$ Current ( $I_{CC}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{CC}$ )	2.0V to +5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC} = 3.3V \pm 0.3V$	0 ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ~ 20 ns/V

**Note 1:** Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Min	Typ	Max	Min	Max			
$V_{IH}$	HIGH Level Input Voltage	2.0 3.0 – 5.5	1.50 0.7 $V_{CC}$			1.50 0.7 $V_{CC}$		V		
$V_{IL}$	LOW Level Input Voltage	2.0 3.0 – 5.5			0.50 0.3 $V_{CC}$	0.50 0.3 $V_{CC}$		V		
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$
4.5	3.94			3.80						
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44		V	
4.5			0.36		0.44					
$I_{OZ}$	3-STATE Output Off-State Current	5.5			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	
$I_{IN}$	Input Leakage Current	0 – 5.5			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	5.5			4.0		40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	

**Noise Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	Conditions
			Typ	Limits		
$V_{OLP}$ (Note 3)	Quiet Output Maximum Dynamic $V_{OL}$	5.0	0.9	1.2	V	$C_L = 50 \text{ pF}$
$V_{OLV}$ (Note 3)	Quiet Output Minimum Dynamic $V_{OL}$	5.0	-0.8	-1.0	V	$C_L = 50 \text{ pF}$
$V_{IHD}$ (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50 \text{ pF}$
$V_{ILD}$ (Note 3)	Maximum HIGH Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50 \text{ pF}$

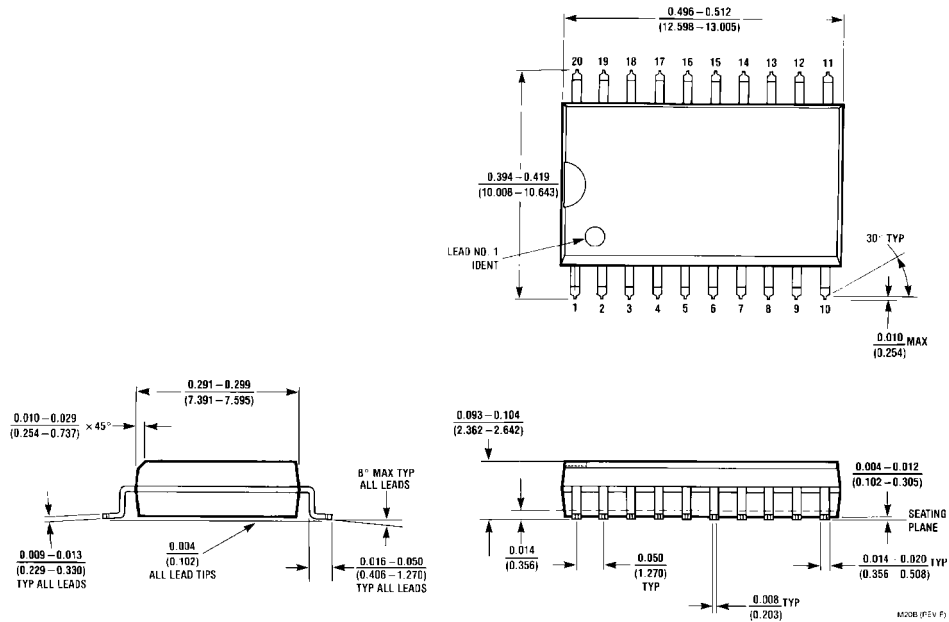
**Note 3:** Parameter guaranteed by design.

AC Electrical Characteristics									
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay Time	3.3 ± 0.3	5.0	7.0	1.0	8.5	ns	C <sub>L</sub> = 15 pF	
t <sub>PHL</sub>			7.5	10.5	1.0	12.0		C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	3.5	5.0	1.0	6.0	ns	C <sub>L</sub> = 15 pF	
			5.0	7.0	1.0	8.0		C <sub>L</sub> = 50 pF	
t <sub>PZL</sub>	3-STATE Output Enable Time	3.3 ± 0.3	6.8	10.5	1.0	12.5	ns	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 15 pF	
t <sub>PZH</sub>			9.3	14.0	1.0	16.0		C <sub>L</sub> = 50 pF	
		5.0 ± 0.5	4.7	7.2	1.0	8.5	ns	C <sub>L</sub> = 15 pF	
			6.2	9.2	1.0	10.5		C <sub>L</sub> = 50 pF	
t <sub>PLZ</sub>	3-STATE Output Disable Time	3.3 ± 0.3	11.2	15.4	1.0	17.5	ns	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 50 pF	
t <sub>PHZ</sub>		5.0 ± 0.5	6.0	8.8	1.0	10.0		C <sub>L</sub> = 50 pF	
t <sub>OSSLH</sub>	Output to Output Skew	3.3 ± 0.3		1.5		1.5	ns	(Note 4) C <sub>L</sub> = 50 pF	
t <sub>OSSLH</sub>		5.0 ± 0.5		1.0		1.0		C <sub>L</sub> = 50 pF	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF	V <sub>CC</sub> = Open	
C <sub>OUT</sub>	Output Capacitance		6				pF	V <sub>CC</sub> = 5.0V	
C <sub>PD</sub>	Power Dissipation Capacitance		18				pF	(Note 5)	

**Note 4:** Parameter guaranteed by design.  $t_{OSSLH} = |t_{PLHmax} - t_{PLHmin}|$ ;  $t_{OSSLH} = |t_{PHLmax} - t_{PHLmin}|$ .

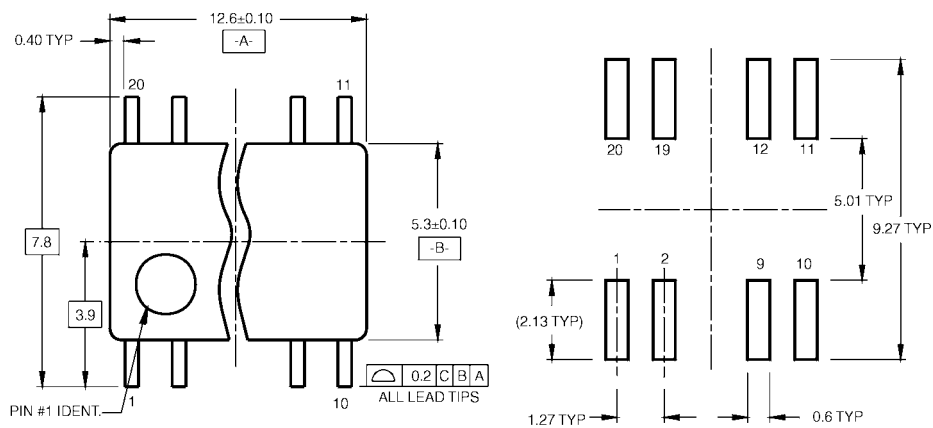
**Note 5:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR.)} = C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$  (per bit).

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

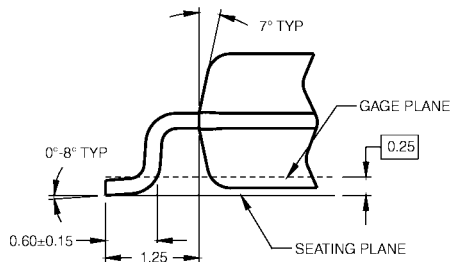
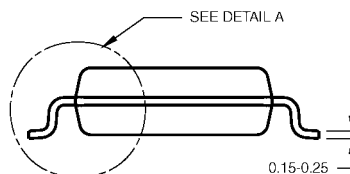
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



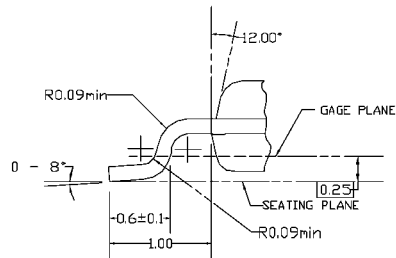
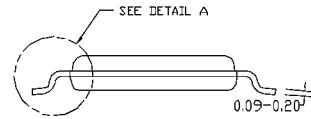
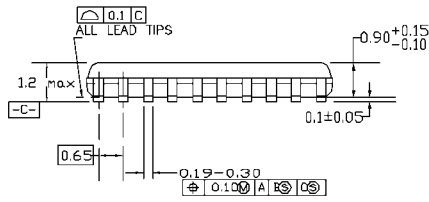
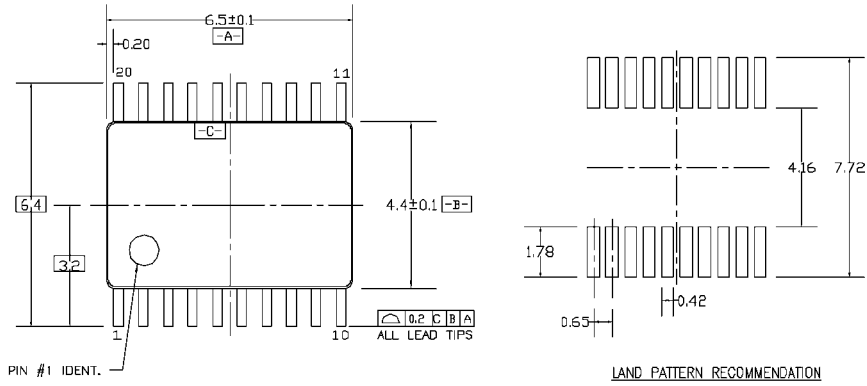
DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

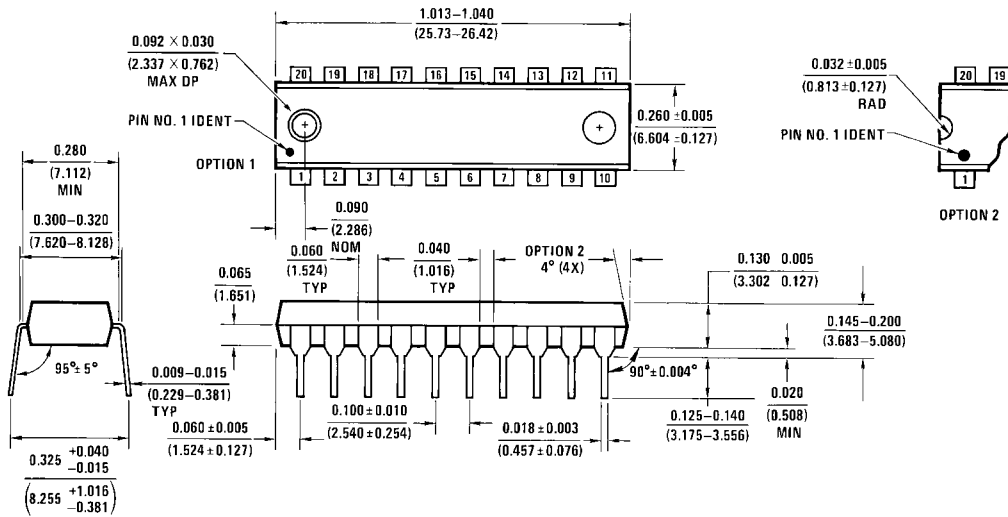
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A**

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