3.3 Volt CMOS Bus Interface 8-Bit Latches

QS74FCT3573
QS74FCT32573

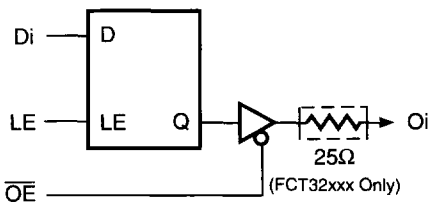
FEATURES/BENEFITS

- Pin and function compatible to the 74F573 74LVT573 and 74FCT573T
- Available in SOIC and QSOP
- Undershoot clamp diodes on all inputs
- Ground bounce controlled outputs
- Low power QCMOS: 0.03 µW typ static
- JEDEC spec compatible
- I_{OL} = 24 mA Com.
- TTL-compatible input and output levels
- Extended temperature –40°C to +85°C
- 2.7V to 3.6V Supply Voltage
- 5V compatible input pins

DESCRIPTION

The QSFCT3573 is an 8-bit high-speed CMOS TTL-compatible buffered latch with three-state outputs that are ideal for driving high-capacitance loads such as memory and address buses. All inputs have clamp diodes for undershoot noise suppression and all outputs have ground bounce suppression (see QSI Application Note AN-001). Input pins can be driven by 3.3V or 5V components allowing voltage transition in mixed supply systems. Ultra-low power QCMOS technology makes this product ideal for portable computing systems or communications devices.

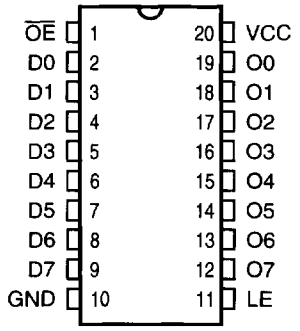
FUNCTIONAL BLOCK DIAGRAM



6

PIN CONFIGURATIONS (All Pins Top View)

SOIC, QSOP



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
LE	I	Latch Enable
$\overline{OE}$	I	Output Enable

FUNCTION TABLE

Inputs $\overline{OE}$	Inputs LE	Inputs Di	Internal Q Value	Outputs Oi	Function
H	X	X	X	Hi-Z	Disable Outputs
L	L	X	L	L	Enable Outputs
L	L	X	H	H	Enable Outputs
X	H	L	L	L	Pass Input Data
X	H	H	H	H	Pass Input Data
L	L	X	Q	Q	Hold Prior Data

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage to Ground	–0.5V to +4.6V
DC Output Voltage V_{OUT}	–0.5V to Vcc + 0.5V[2]
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with V_{IN} < 0	±20 mA
DC Output Diode Current with V_{OUT} < 0	±50 mA
DC Output Current Max. Sink Current/Pin	±60 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.
2. Not to exceed 4.6V

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	Unit
1-9, 11	4	4	pF
12-19	6	6	pF

Note: Capacitance is characterized but not tested.

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min	Max	Unit
Vcc	Supply Voltage	2.7	3.6	V
V_{IN}	Input Voltage	0	Vcc	V
V_{OUT}	Output Voltage	0	Vcc	V
T_A	Ambient Operating Temperature	–40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate [1]	0	8	ns/V

Notes:
1. As measured between 0.8V and 2V.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Recommended operating conditions apply unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Input Pins	2.0	—	5.5	V
		I/O Pins	2.0	—	V_{CC}+0.5	V
V_{IL}	Input LOW Voltage	Input Pins	–0.5	—	0.8	V
ΔV_T	Input Hysterisis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., 0 ≤ V_{IN} < V_{CC}	—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., 0 ≤ V_{IN} ≤ V_{CC}	—	—	5	µA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND(2,3)	–60	—	–225	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA(3)	—	–0.7	—	V
V_{OH}	Output HIGH Voltage	V_I = V_{IH} or V_{IL}, V_{CC} = Min, I_{OH} = –100 µA	V_{CC}–0.2	—	—	V
		V_I = V_{IH} or V_{IL}, V_{CC} = 3V, I_{OH} = –8 mA	2.4	—	—	V
V_{OL}	Output LOW Voltage (FCT3XXX)	V_I = V_{IH} or V_{IL}, V_{CC} = Min, I_{OL} = 100 µA	—	—	0.2	V
		V_I = V_{IH} or V_{IL}, V_{CC} = 3V, I_{OL} = 16 mA	—	—	0.4	V
		V_I = V_{IH} or V_{IL}, V_{CC} = 3V, I_{OL} = 24 mA	—	—	0.5	V
V_{OL}	Output LOW Voltage (FCT32XXX–25Ω)	V_I = V_{IH} or V_{IL}, V_{CC} = 3V, I_{OL} = 8 mA	—	—	0.5	V
R_{OUT}	Output Resistance(4) (FCT32XXX–25Ω)	V_{CC} = 3V, I_{OL} = 8 mA	—	40	—	Ω

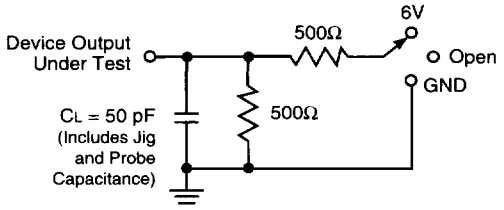
Notes:

1. Typical values indicate V_{CC} = 3.3V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.
4. R_{OUT} represents total output impedance and includes added series termination resistance.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ VIN ≤ 0.2V or Vcc-0.2V ≤ VIN ≤ Vcc	—	0.01	20	µA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., freq = 0, VIN = Vcc – 0.6V	—	1.0	20	µA
QCCD	Supply Current per Input per MHz	Vcc = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or Vcc[2,3]	—	40	85	µA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. For flip-flops, QCCD is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
3. Ic can be computed using the above parameters as explained in the Technical Overview section.



Test	Switch
tPHL/tPLH	Open
tPZL/tPLZ	6V
tPZH/tPHZ	GND

Load Circut for Outputs

Notes
1. Input pulse charateristics: 0V to 2.7V, tr = tf = 2.5 ns (10% to 90%), transition measured at 1.5V, pulse generator ZOUT = 50Ω.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Recommended operating conditions apply unless otherwise specified.

Symbol	Description[1]	3573, 32573 (Vcc = 3.3V ± 0.3V) Min	3573, 32573 (Vcc = 3.3V ± 0.3V) Max	3573A, 32573A (Vcc = 3.3V ± 0.3V) Min	3573A, 32573A (Vcc = 3.3V ± 0.3V) Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Oi, FCT3573	1.5	8	1.5	5.2	ns
t_{PLH} t_{PHL}	Propagation Delay Data to Oi, FCT32573	1.5	8	1.5	5.2	ns
t_{PLH} t_{PHL}	Propagation Delay Data LE to Oi, FCT3573	2	13	2	8.5	ns
t_{PLH} t_{PHL}	Propagation Delay Data LE to Oi, FCT32573	2	13	2	8.5	ns
t_{PZH} t_{PZL}	Output Enable $\overline{OE}$, to Yi, FCT3573	1.5	11	1.5	6.5	ns
t_{PZH} t_{PZL}	Output Enable $\overline{OE}$, to Yi, FCT32573	1.5	11	1.5	6.5	ns
t_{PLZ} t_{PHZ}	Disable Time[2]	1.5	7	1.5	5.5	ns
t_S	Data Setup Time	2	—	2	—	ns
t_H	Data Hold Time Di to LE HIGH-to-LOW	1.5	—	1.5	—	ns
t_W	LE Pulse Width[2] HIGH or LOW	6	—	5	—	ns

Notes:

1. Minimums guaranteed but not tested for all parameters except t_S and t_H.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.