



Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVERS (3-STATE)

IDT54/74FCT623T/AT/CT

FEATURES:

- Std., A and C speed grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- High drive outputs (-15mA IOH, 64mA IOL)
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

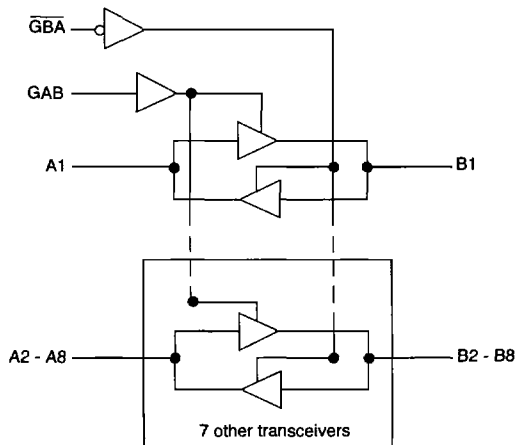
DESCRIPTION

The FCT623T/AT/CT is a non-inverting octal transceiver with 3-state bus-driving outputs in both the send and receive directions. The B bus outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

One important feature of the FCT623T/AT/CT is the Power Down Disable capability. When the GAB and $\bar{G}BA$ inputs are conditioned to put the device in high-Z state, the I/O ports will maintain high impedance during power supply ramps and when $V_{CC} = 0\text{V}$. This is a desirable feature in back-plane applications where it may be necessary to perform "live" insertion and removal of cards for on-line maintenance. It is also a benefit in systems with multiple redundancy where one or more redundant cards may be powered-off.

FUNCTIONAL BLOCK DIAGRAM



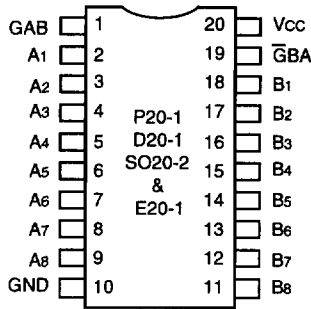
2563 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

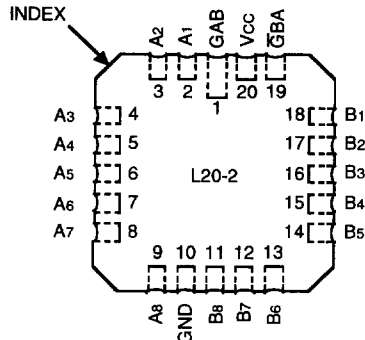
JUNE 1996

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2563 drw 02



LCC
TOP VIEW

2563 drw 03

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{\text{GBA}}$, GAB	Enable Inputs
A1 - A8	A Bus Inputs or 3-State Outputs
B1 - B8	B Bus Inputs or 3-State Outputs

2563 tbl 01

FUNCTION TABLE⁽¹⁾

Enable Inputs		Outputs
$\overline{\text{GBA}}$	GAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Z
L	H	B data to A bus A data to B bus

NOTES:

1. H = HIGH Voltage Level
2. L = LOW Voltage Level
3. Z = High-Impedance (OFF) state

2563 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc +0.5	-0.5 to Vcc +0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
Pr	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

2563 lmk 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COU	Output Capacitance	VOU = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

2563 lmk 04



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I_{IH}	Input HIGH Current ⁽⁵⁾	$V_{CC} = \text{Max.}, V_I = 2.7\text{V}$	—	—	± 1	μA	
I_{IL}	Input LOW Current ⁽⁵⁾	$V_{CC} = \text{Max.}, V_I = 0.5\text{V}$	—	—	± 1	μA	
I_I	Input HIGH Current ⁽⁵⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$	—	—	± 1	μA	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18\text{mA}$	—	-0.7	-1.2	V	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$	-60	-120	-225	mA	
V_{OH}	Output HIGH Voltage (A and B Bus)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage (A Bus)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}			0.3	0.5	V
			$I_{OL} = 32\text{mA MIL.}^{(4)}$ $I_{OL} = 48\text{mA COM'L.}$				
V_{OL}	Output LOW Voltage (B Bus)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}			0.3	0.55	V
			$I_{OL} = 48\text{mA MIL.}^{(4)}$ $I_{OL} = 64\text{mA COM'L.}$				
I_{OFF}	Input/Output Power Off Leakage ⁽⁶⁾	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$	—	—	± 1	μA	
V_H	Input Hysteresis	—	—	200	—	mV	
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}	—	0.01	1	μA	

NOTES:

2563 104 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
Δ ICC	Quiescent Power Supply Current TTL Inputs HIGH	VCC = Max. VIN = 3.4V ⁽³⁾		—	0.5	2.0	mA
ICCD	Dynamic Power Supply Current ⁽⁴⁾	VCC = Max. Outputs Open \bar{G} BA = GAB = GND One Input Toggling 50% Duty Cycle	VIN = VCC VIN = GND	—	0.15	0.25	mA/ MHz
IC	Total Power Supply Current ⁽⁶⁾	VCC = Max. Outputs Open fi = 10MHz 50% Duty Cycle \bar{G} BA = GAB = GND One Bit Toggling	VIN = VCC VIN = GND	—	1.5	3.5	mA
		VCC = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle \bar{G} BA = GAB = GND Eight Bits Toggling	VIN = VCC VIN = GND	—	3.0	6.0 ⁽⁵⁾	
		VCC = Max. Outputs Open fi = 10MHz 50% Duty Cycle \bar{G} BA = GAB = GND One Bit Toggling	VIN = 3.4V VIN = GND	—	1.8	4.5	
		VCC = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle \bar{G} BA = GAB = GND Eight Bits Toggling	VIN = 3.4V VIN = GND	—	5.0	14.0 ⁽⁵⁾	

NOTES:

2563 tbl 07

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Per TTL driven input (VIN = 3.4V). All other inputs at VCC or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
- IC = IQUIESCENT + IINPUTS + IDYNAMIC
 IC = ICC + Δ ICC DH/NT + ICCD (fCP/2 + fiNi)
 ICC = Quiescent Current
 Δ ICC = Power Supply Current for a TTL High Input (VIN = 3.4V)
 DH = Duty Cycle for TTL Inputs High
 NT = Number of TTL Inputs at DH
 ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 fCP = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 fi = Input Frequency
 Ni = Number of Inputs at fi
 All currents are in milliamps and all frequencies are in megahertz.



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	54/74FCT623T		54/74FCT623AT				54/74FCT623CT				Unit		
			Com'l.		Mil.		Com'l.		Mil.		Com'l.			Mil.	
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		Min. ⁽²⁾	Max.
tPLH	Propagation Delay An to Bn	CL = 50pF RL = 500Ω	1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPHL	Propagation Delay Bn to An		1.5	7.5	1.5	9.5	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPZH	Output Enable Time \bar{G} BA to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ	Output Disable Time \bar{G} BA to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

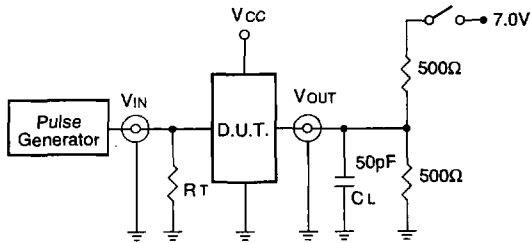
NOTES:

2563 tbl 07

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2563 drw 05

SWITCH POSITION

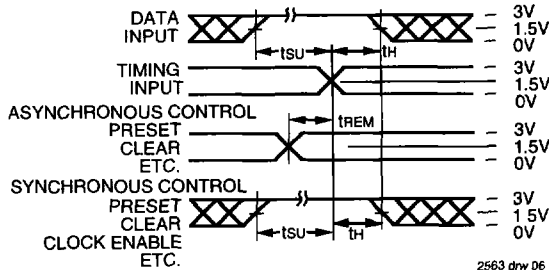
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2563 trw 09

DEFINITIONS:

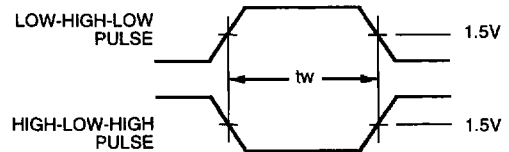
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Zout of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



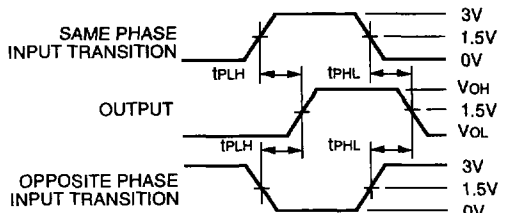
2563 drw 06

PULSE WIDTH



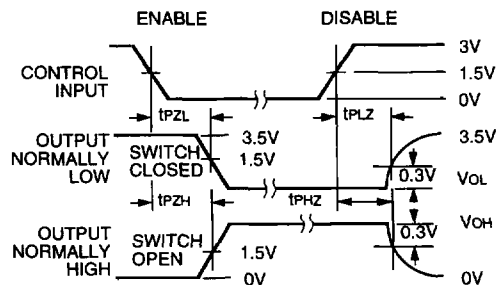
2563 drw 07

PROPAGATION DELAY



2563 drw 08

ENABLE AND DISABLE TIMES



2563 drw 09

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

ORDERING INFORMATION

