

December 1996

## Fast CMOS Bus Interface Registers

### Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (CD74FCT2821T, CD74FCT2823T Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

### Description

The CD74FCT821T and CD74FCT2821T are 10-bit wide registers designed with ten D-type flip-flops with a buffered common clock and buffered three-state outputs. The CD74FCT823T and CD74FCT2823T are 9-bit wide registers designed with Clock Enable and Clear. The CD74FCT825T is an 8-bit wide register with all CD74FCT823T controls plus multiple enables. When output enable ( $\overline{OE}$ ) is LOW, the outputs are enabled. When  $\overline{OE}$  is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The CD74FCT2821T and CD74FCT2823T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT821ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT821BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT821CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2821ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2821ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2821BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2821BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823CTQM	-40 to 85	24 Ld QSOP	M24.15-P

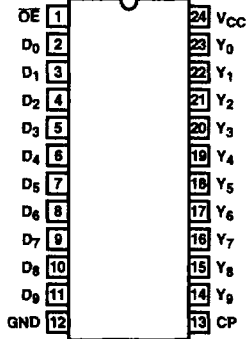
NOTE: QSOP is commonly known as SSCP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

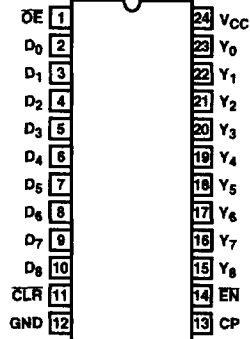
CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T

Pinouts

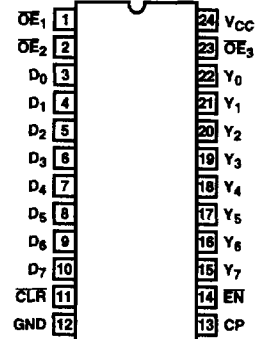
CD74FCT821T, CD74FCT2821T  
(QSOP, SOIC)  
TOP VIEW



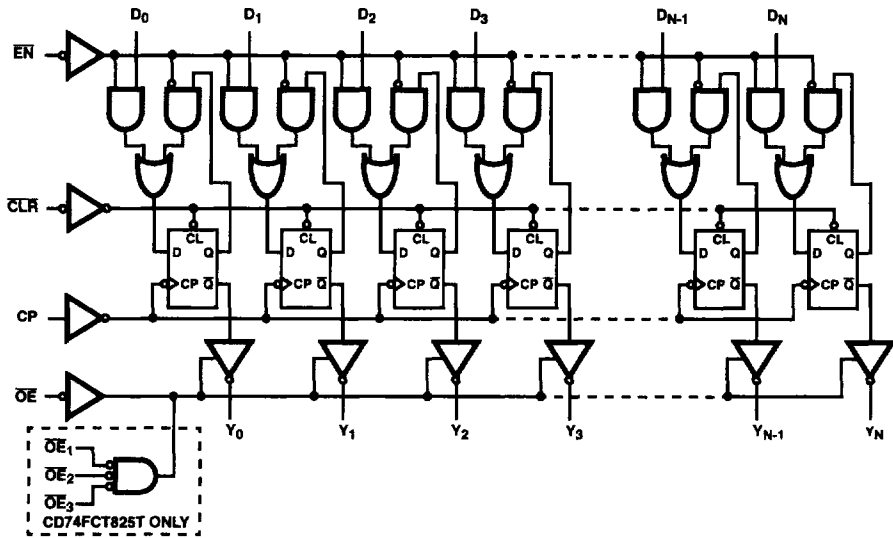
CD74FCT823, CD74FCT2823T  
(QSOP, SOIC)  
TOP VIEW



CD74FCT825T  
(QSOP, SOIC)  
TOP VIEW



Functional Block Diagram



4  
OCTAL 5V FCT  
5V FCT 25Ω

**CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T**

TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS	INTERNAL
	$\overline{\text{CLR}}$	$\overline{\text{EN}}$	$\overline{\text{OE}}$	CP	$\text{D}_N$	$\text{Y}_N$	$\text{Q}_N$
High-Z	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
Clear	L	X	H	X	X	Z	L
	L	X	L	X	X	L	L
Hold	H	H	H	X	X	Z	NC
	H	H	L	X	X	NC	NC
Load	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
	H	L	L	↑	L	L	L
	H	L	L	↑	H	H	H

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance
- NC = No Change
- ↑ = LOW-to-HIGH Transition

**Pin Descriptions**

PIN NAME	DESCRIPTION
$\overline{\text{OE}}$	Output Enable Input (Active LOW)
CP	Clock Pulse for the Register, Enters Data on LOW-to-HIGH Transition
$\text{D}_N$	Data Inputs
$\text{Y}_N$	Three-State Outputs
$\overline{\text{CLR}}$	Clear Input (Active LOW) (823/825/2823 Only)
$\overline{\text{EN}}$	Clock Enable Input (Active LOW)
GND	Ground
VCC	Power

**CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T**

**Absolute Maximum Ratings**

DC Input Voltage	.....-0.5V to 7.0V
DC Output Current	.....120mA

**Thermal Information**

Thermal Resistance (Typical, Note 2)	$\theta_{JA}$ (°C/W)
SOIC Package	75
QSOP Package	100
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (Lead Tips Only)

**Operating Conditions**

Operating Temperature Range	.....-40°C to 85°C
Supply Voltage to Ground Potential	
Inputs and $V_{CC}$ Only	.....-0.5V to 7.0V
Supply Voltage to Ground Potential	
Outputs and D/O Only	.....-0.5V to 7.0V

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

- 2.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS
<b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$						
Output HIGH Voltage	$V_{OH}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -15.0\text{mA}$	2.4	3.0	- V
Output LOW Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 48\text{mA}$	-	0.3	0.50 V
Output LOW Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 12\text{mA}$ (25 $\Omega$ series)	-	0.3	0.50 V
Input HIGH Voltage	$V_{IH}$	Guaranteed Logic HIGH Level		2.0	-	- V
Input LOW Voltage	$V_{IL}$	Guaranteed Logic LOW Level		-	-	0.8 V
Input HIGH Current	$I_{IH}$	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC}$	-	-	1 $\mu\text{A}$
Input LOW Current	$I_{IL}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$	-	-	-1 $\mu\text{A}$
High Impedance Output Current	$I_{OZH}$ , $I_{OZL}$	$V_{CC} = \text{Max}$	$V_{OUT} = 2.7\text{V}$			1 $\mu\text{A}$
			$V_{OUT} = 0.5\text{V}$			-1 $\mu\text{A}$
Clamp Diode Voltage	$V_{IK}$	$V_{CC} = \text{Min}$ , $I_{IN} = -18\text{mA}$		-	-0.7	-1.2 V
Short Circuit Current	$I_{OS}$	$V_{CC} = \text{Max}$ (Note 5), $V_{OUT} = \text{GND}$		-60	-120	- mA
Power Down Disable	$I_{OFF}$	$V_{CC} = \text{GND}$ , $V_{OUT} = 4.5\text{V}$		-	-	100 $\mu\text{A}$
Input Hysteresis	$V_H$			-	200	- mV
<b>CAPACITANCE</b> $T_A = 25^{\circ}\text{C}$ , $f = 1\text{MHz}$						
Input Capacitance (Note 6)	$C_{IN}$	$V_{IN} = 0\text{V}$		-	6	10 pF
Output Capacitance (Note 6)	$C_{OUT}$	$V_{OUT} = 0\text{V}$		-	8	12 pF
<b>POWER SUPPLY SPECIFICATIONS</b>						
Quiescent Power Supply Current	$I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or $V_{CC}$	-	0.1	500 $\mu\text{A}$
Supply Current per Input at TTL HIGH	$\Delta I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = 3.4\text{V}$ (Note 7)	-	0.5	2.0 mA
Supply Current per Input per MHz (Note 8)	$I_{CCD}$	$V_{CC} = \text{Max}$ , Outputs Open $\text{OE} = \text{EN} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.15	0.25 mA/MHz

**4**

OCTAL 5V FCT  
5V FCT 25 $\Omega$

**CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T**

**Electrical Specifications (Continued)**

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP		MAX	UNITS
Total Power Supply Current (Note 10)	I <sub>C</sub>	V <sub>CC</sub> = Max, Outputs Open f <sub>CP</sub> = 10MHz, 50% Duty Cycle OE = EN = GND f <sub>i</sub> = 5MHz One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	-	1.5	3.5 (Note 9)	mA	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	-	2.0	5.5 (Note 9)	mA	
		V <sub>CC</sub> = Max, Outputs Open f <sub>CP</sub> = 10MHz, 50% Duty Cycle OE = EN = GND Eight Bits Toggling f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	-	3.5	7.3 (Note 9)	mA	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	-	6.0	16.3 (Note 9)	mA	

**Switching Specifications Over Operating Range**

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		CT (NOTE 14)		UNIT
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
<b>CD74FCT821T, CD74FCT2821T</b>									
Propagation Delay CP to Y <sub>N</sub> (OE = LOW)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C <sub>L</sub> = 300pF (Note 13) R <sub>L</sub> = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
Setup Time HIGH or LOW, D <sub>N</sub> to CP	t <sub>SU</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, D <sub>N</sub> to CP	t <sub>H</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	2.0	-	1.5	-	1.5	-	ns
Setup Time HIGH or LOW, EN to CP	t <sub>SU</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, EN to CP	t <sub>H</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	2.0	-	0	-	0	-	ns
Propagation Delay CLR to Y <sub>N</sub>	t <sub>PHL</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	ns
Recovery Time, CLR to CP (Note 13)	t <sub>REM</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	6.0	-	6.0	-	6.0	-	ns
Clock Pulse Width HIGH or LOW (Note 13)	t <sub>w</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	7.0	-	5.0	-	6.0	-	ns
CLR Pulse Width LOW (Note 13)	t <sub>w</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	6.0	-	6.0	-	6.0	-	ns
Output Enable Time OE to Y <sub>N</sub>	t <sub>PZH</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
	t <sub>PZL</sub>	C <sub>L</sub> = 300pF (Note 13) R <sub>L</sub> = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
Output Disable Time OE to Y <sub>N</sub>	t <sub>PHZ</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
	t <sub>PLZ</sub>	C <sub>L</sub> = 300pF (Note 13) R <sub>L</sub> = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns
<b>CD74FCT823T, CD74FCT2823T, CD74FCT825T</b>									
Propagation Delay CP to Y <sub>N</sub> (OE = LOW)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C <sub>L</sub> = 300pF (Note 13) R <sub>L</sub> = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns

Switching Specifications Over Operating Range

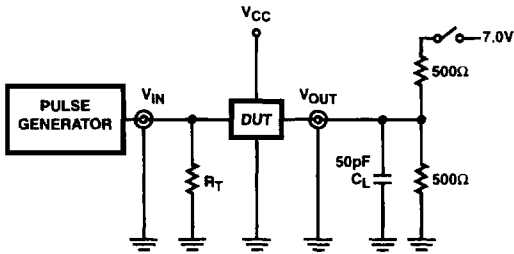
PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		CT (NOTE 14)		UNIT
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
Setup Time HIGH or LOW, D <sub>N</sub> to CP	t <sub>SU</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, D <sub>N</sub> to CP	t <sub>H</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	2.0	-	1.5	-	1.5	-	ns
Setup Time HIGH or LOW, E <sub>N</sub> to CP	t <sub>SU</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, E <sub>N</sub> to CP	t <sub>H</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	2.0	-	0	-	0	-	ns
Propagation Delay CLR to Y <sub>N</sub>	t <sub>PHL</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	13.0	1.5	9.0	1.5	8.0	ns
Recovery Time, CLR to CP (Note 13)	t <sub>REM</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	6.0	-	6.0	-	6.0	-	ns
Clock Pulse Width HIGH or LOW (Note 13)	t <sub>W</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	7.0	-	5.0	-	6.0	-	ns
CLR Pulse Width LOW (Note 13)	t <sub>W</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	6.0	-	6.0	-	6.0	-	ns
Output Enable Time OE to Y <sub>N</sub>	t <sub>PZH</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
	t <sub>PZL</sub>	C <sub>L</sub> = 300pF (Note 13) R <sub>L</sub> = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
Output Disable Time OE to Y <sub>N</sub>	t <sub>PHZ</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
	t <sub>PLZ</sub>	C <sub>L</sub> = 300pF (Note 13) R <sub>L</sub> = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_{CC} = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>in</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- The CD74FCT2821CT type is not available.

4  
OCTAL 5V FCT  
5V FCT 25Ω

Test Circuits and Waveforms



NOTE:

15. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_f, t_r \leq 2.5\text{ns}$ .

FIGURE 1. TEST CIRCUIT

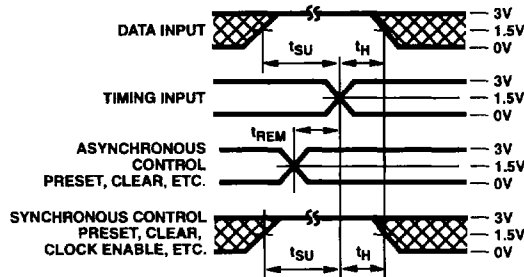


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}, t_{PZL}$	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

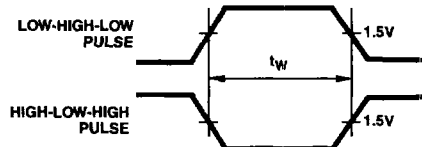


FIGURE 3. PULSE WIDTH

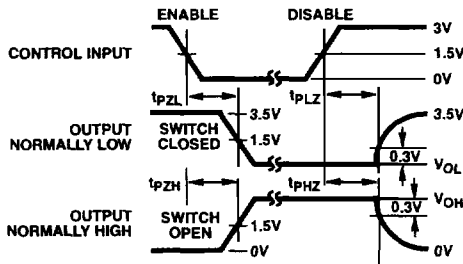


FIGURE 4. ENABLE AND DISABLE TIMING

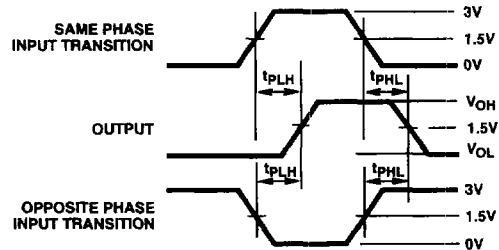


FIGURE 5. PROPAGATION DELAY