

74ACQ534•74ACTQ534

Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The 'ACQ/'ACTQ534 is the same as the 'ACQ/'ACTQ374 except that the outputs are inverted.

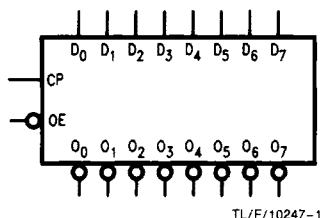
The 'ACQ/'ACTQ534 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

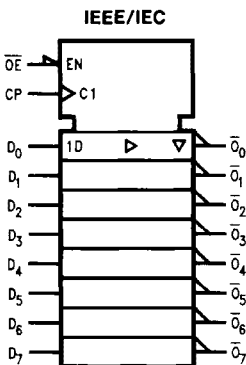
- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Inverted output version of the 'ACQ/'ACTQ374
- Faster prop delays than the standard 'ACT534
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols

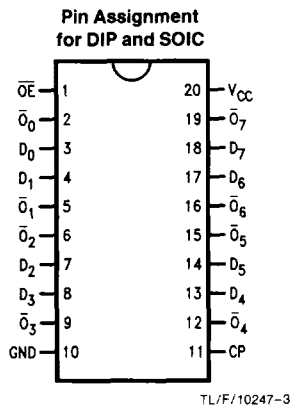


TL/F/10247-1



TL/F/10247-2

Connection Diagram



TL/F/10247-3

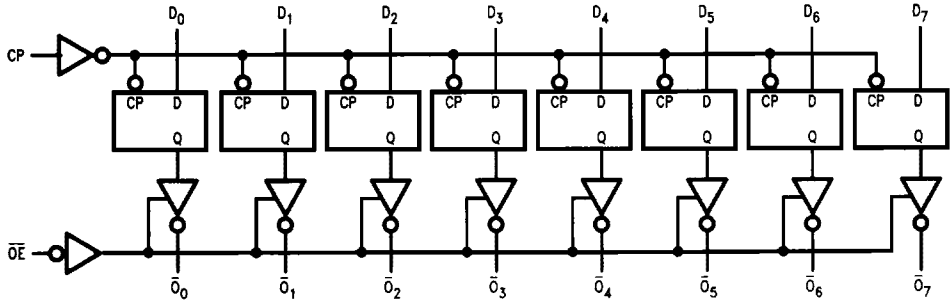
Pin Names	Description
D ₀ -D ₇	Data Inputs
CP	Clock Pulse Input
\overline{OE}	TRI-STATE Output Enable Input
\overline{O}_0 - \overline{O}_7	Complementary TRI-STATE Outputs

Functional Description

The 'ACQ/'ACTQ534 consists of eight D-type flip-flops with individual inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times

requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Logic Diagram



TL/F/10247-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Output
CP	OE	D	\overline{O}
⎓	L	H	L
⎓	L	L	H
L	L	X	\overline{O}_0
X	H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

⎓ = LOW-to-HIGH Clock Transition

Z = High Impedance

\overline{O}_0 = Value stored from previous clock cycle

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V	
DC Input Diode Current (I_{IK})		
$V_I = -0.5V$	-20 mA	
$V_I = V_{CC} + 0.5V$	+20 mA	
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$	
DC Output Diode Current (I_{OK})		
$V_O = -0.5V$	-20 mA	
$V_O = V_{CC} + 0.5V$	+20 mA	
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$	
DC Output Source or Sink Current (I_O)	± 50 mA	
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA	
Storage Temperature (T_{STG})	-65°C to +150°C	
DC Latch-Up Source or Sink Current	± 300 mA	
Junction Temperature (T_J)		
PDIP	140°C	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V	
'ACQ	4.5V to 5.5V	
'ACTQ		
Input Voltage (V_I)	0V to V_{CC}	
Output Voltage (V_O)	0V to V_{CC}	
Operating Temperature (T_A)	-40°C to +85°C	
74ACQ/ACTQ		
Minimum Input Edge Rate $\Delta V/\Delta t$		
'ACQ Devices	V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns	
Minimum Input Edge Rate $\Delta V/\Delta t$		
'ACTQ Devices	V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns	

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ		74ACQ		Units	Conditions
			$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	$I_{OUT} = -50 \mu\text{A}$
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		V	* $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	$I_{OUT} = 50 \mu\text{A}$
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		V	* $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0		μA	$V_I = V_{CC}, \text{GND}$ (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74ACQ		74ACQ		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V _{IN} = V _{CC} or GND (Note 1)	
I _{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.25	±2.5	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.1	1.5		V	Figures 2-12, 13 (Note 2, 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.6	-1.2		V	Figures 2-12, 13 (Notes 2, 3)	
V _{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Notes 2, 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Notes 2, 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V _{CC} (V)	74ACTQ		74ACTQ		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} = -24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} = 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.25	±2.5	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND	
I _{CC} T	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1V	

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74ACTQ		74ACTQ		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			-75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0		μA	V _{IN} = V _{CC} or GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.1	1.5			V	Figures 2-12, 13 (Notes 1, 2)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.6	-1.2			V	Figures 2-12, 13 (Notes 1, 2)
V _{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 1, 3)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 1, 3)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Plastic DIP package.

Note 2: Max number of Data Inputs defined as (n). n-1 Data Inputs are driven 0V to 3V. One Data Input @ V_{IN} = GND.

Note 3: Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74ACQ			74ACQ		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	75 90			70 85		MHz	
t _{PHL} , t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5	3.0 2.0	13.5 9.0	ns	2-3, 4
t _{PZL} , t _{PZH}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5	3.0 2.0	13.5 9.0	ns	2-5, 6
t _{PHZ} , t _{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	9.5 8.0	14.5 9.5	1.0 1.0	15.0 10.0	ns	2-5, 6
t _{OSSL} , t _{OSLH}	Output to Output Skew** CP to Q _n	3.3 5.0		1.0 0.5	1.5 1.0		1.5 1.0	ns	

*Voltage Range 5.0 is 5.0V ± 0.5V, Voltage Range 3.3 is 3.3V ± 0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSSL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74ACQ		74ACQ		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0	1.0 1.0	3.0 3.0	3.0 3.0	ns	2-7	
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0	0 0	1.5 1.5	1.5 1.5	ns	2-7	
t _w	CP Pulse Width HIGH or LOW	3.3 3.3	2 2	4.0 4.0	4.0 4.0	ns	2-4	

*Voltage Range 5.0 is 5.0V ± 0.5V, Voltage Range 3.3 is 3.3V ± 0.3V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74ACTQ			74ACTQ		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	85			80	MHz		
t _{PHL} , t _{PLH}	Propagation Delay CP to Q _n	5.0	2.0	7.0	9.0	2.0	9.5	ns	2-3, 4
t _{PZL} , t _{PZH}	Output Enable Time	5.0	2.0	7.0	9.0	2.0	9.5	ns	2-5, 6
t _{PHZ} , t _{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	10.5	ns	2-5, 6
t _{OSSL} , t _{OSLH}	Output to Output Skew** CP to Q _n	5.0		0.5	1.0		1.0	ns	

*Voltage Range 5.0 is 5.0V ± 0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSSL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74ACTQ		74ACTQ		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	1.0	3.0	3.0	ns	2-7	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	0	1.5	1.5	ns	2-7	
t _w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.0	ns	2-4	

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	40.0	pF	V _{CC} = 5.0V