

40097B • 40098B

3-STATE HEX NON-INVERTING AND INVERTING BUFFERS

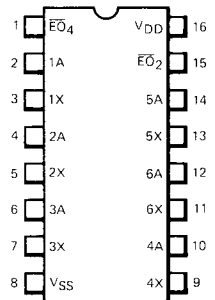
DESCRIPTION – These two CMOS buffers provide high current output capability suitable for driving high capacitance loads. The 40097B is a Non-Inverting CMOS Buffer with 3-state outputs and the 40098B is an Inverting CMOS Buffer with 3-state outputs. The 3-state outputs of each device are controlled by two Enable Inputs (\overline{EO}_4 , \overline{EO}_2). A HIGH on Enable Input \overline{EO}_4 causes the Outputs of four of the six buffer elements to assume a high impedance or OFF state, regardless of other input conditions and a HIGH on Enable Input \overline{EO}_2 causes the Outputs of the remaining two buffer elements to assume a high impedance or OFF state, regardless of other input conditions.

- 3STATE OUTPUTS
- TTL COMPATIBLE – FAN OUT OF ONE TTL LOAD
- ACTIVE LOW ENABLE INPUTS

PIN NAMES

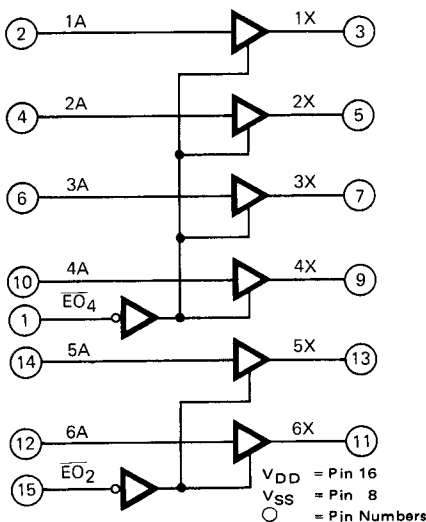
1A–6A	Buffer Inputs
\overline{EO}_4 , \overline{EO}_2	Enable Inputs (Active LOW)
1X–6X	Buffer Outputs (Active HIGH for the 40097B and Active LOW for the 40098B)

CONNECTION DIAGRAM DIP (TOP VIEW)

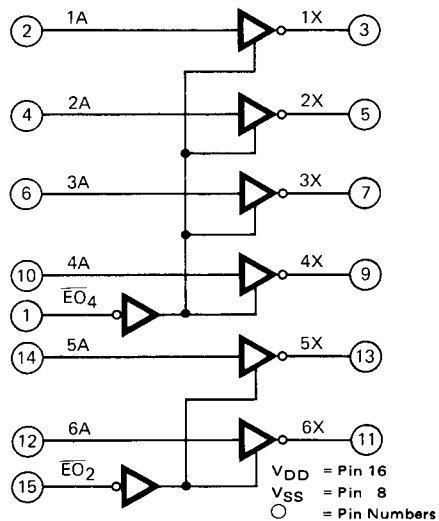


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

40097B LOGIC DIAGRAM



40098B LOGIC DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

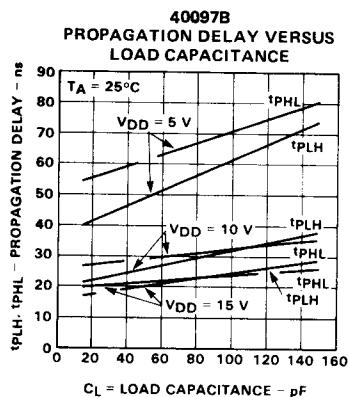
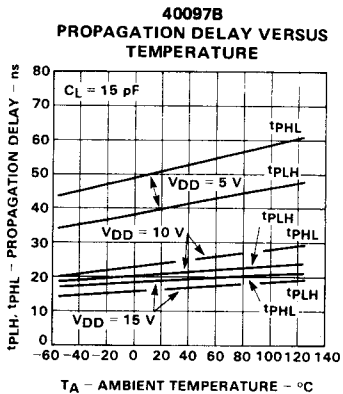
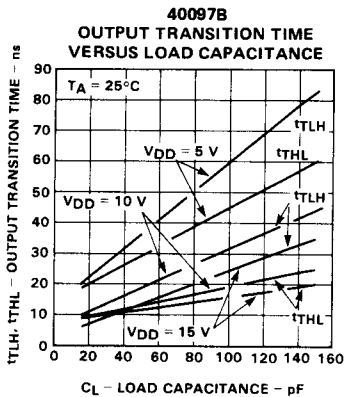
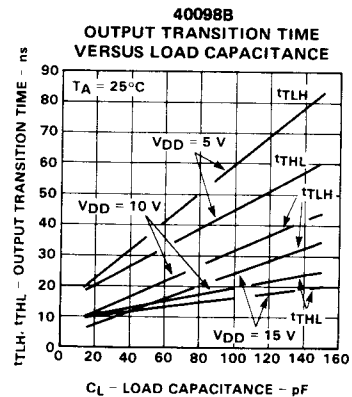
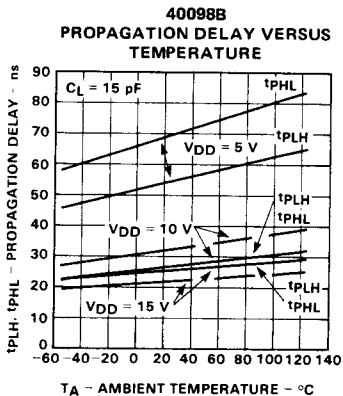
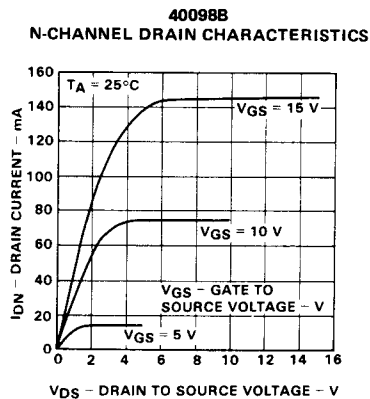
SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current	-1.0			-2.0			-3.2			mA	MIN, 25°C	$V_{OUT} = 4.5$ V for $V_{DD} = 5$ V $V_{OUT} = 9.5$ V for $V_{DD} = 10$ V $V_{OUT} = 14.5$ V for $V_{DD} = 15$ V Inputs at V_{SS} or V_{DD} Per Logic Function
		-0.7			-1.4			-2.2				MAX	
I_{OL}	Output LOW Current	2.5			6.25			11.25			mA	MIN, 25°C	$V_{OUT} = 0.4$ V for $V_{DD} = 5$ V $V_{OUT} = 0.5$ V for $V_{DD} = 10$ V $V_{OUT} = 0.5$ V for $V_{DD} = 15$ V Inputs at V_{SS} or V_{DD} Per Logic Function
		1.8			4.5			8.25				MAX	
I_{OZH}	Output OFF Current HIGH	XC								1.6	μ A	MIN, 25°C	Output Returned to V_{DD} , $\bar{E}O_n = V_{DD}$
		XM								0.4		MAX	
I_{OZL}	Output OFF Current LOW	XC								-1.6	μ A	MIN, 25°C	Output Returned to V_{SS} , $\bar{E}O_n = V_{DD}$
		XM								-12		MAX	
I_{DD}	Quiescent Power Supply Current	XC		4		8				16	μ A	MIN, 25°C	All Inputs at 0 V or V_{DD}
		XM		30		60				120		MAX	
				30		60				4		MIN, 25°C	
				30		60				120		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^\circ$ C, 40097B only (See Note 2)

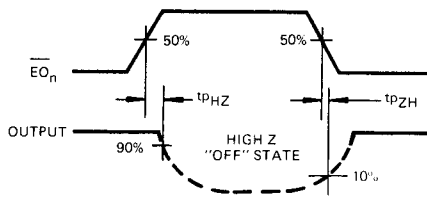
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, Data to Output		65	100		25	40		20	32	ns	$C_L = 50$ pF, $R_L = 200$ k Ω
t_{PHL}			80	100		28	40		20	32		
t_{PZH}	Output Enable Time		70	110		35	55		29	44	ns	$(R_L = 1$ k Ω to V_{SS}) $(R_L = 1$ k Ω to V_{DD})
t_{PZL}			95	150		40	65		30	52		
t_{PHZ}	Output Disable Time		40	65		31	55		29	44	ns	$(R_L = 1$ k Ω to V_{SS}) $(R_L = 1$ k Ω to V_{DD})
t_{PLZ}			60	95		35	55		30	44		
t_{TLH}	Output Transition Time		40	65		25	40		15	30	ns	Input Transition Times ≤ 20 ns
t_{THL}			30	60		15	30		15	30		

Notes on following page.

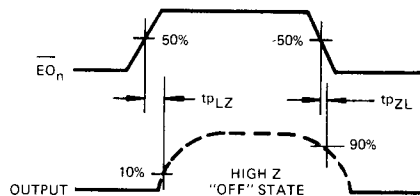
TYPICAL ELECTRICAL CHARACTERISTICS (Cont'd)



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PHZ}) AND OUTPUT DISABLE TIME (t_{PZH})



OUTPUT ENABLE TIME (t_{PLZ}) AND OUTPUT DISABLE TIME (t_{PZL})