# CY74FCT16646T
# CY74FCT162646T

# 16-Bit Registered Transceiver

## Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-E speed at 3.8 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40°C to +85°C**
- **$V_{CC}$ = 5V ± 10%**

*CY74FCT16646T Features:*

- **64 mA sink current, 32 mA source current**
- **Typical $V_{OLP}$ (ground bounce) <1.0V at $V_{CC}$ = 5V, $T_A$ = 25°C**

*CY74FCT162646T Features:*

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
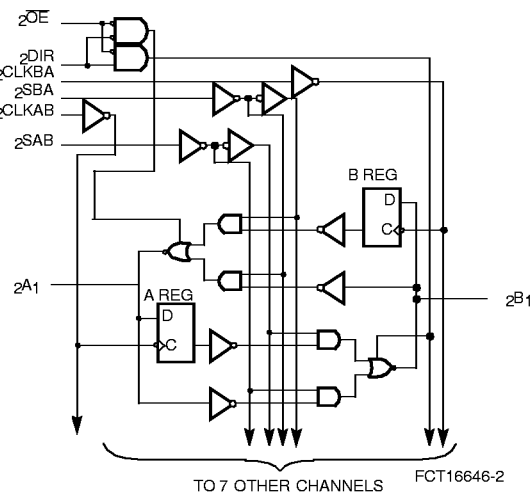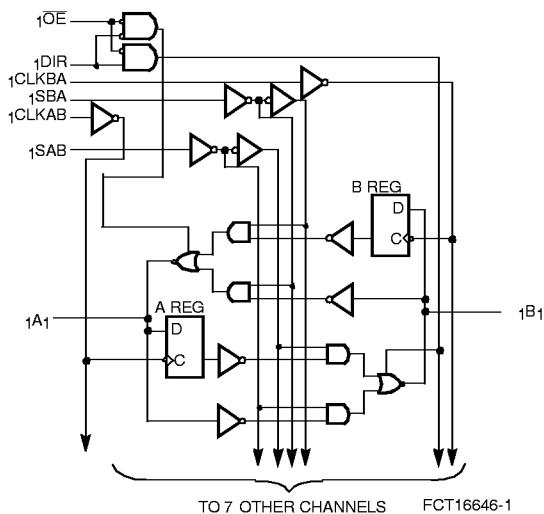- **Typical $V_{OLP}$ (ground bounce) <0.6V at $V_{CC}$ = 5V, $T_A$= 25°C**

## Functional Description

The CY74FCT16646T and CY74FCT162646T 16-bit transceivers are three-state, D-type registers, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Output Enable ($\overline{OE}$) and direction pins (DIR) are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the Output Enable ($\overline{OE}$) is Active LOW. In the isolation mode (Output Enable ($\overline{OE}$) HIGH), A data may be stored in the B register and/or B data may be stored in the A register. The output buffers are designed with a power-off disable feature that allows live insertion of boards.

The CY74FCT16646T is ideally suited for driving high-capacitance loads and low-impedance backplanes.
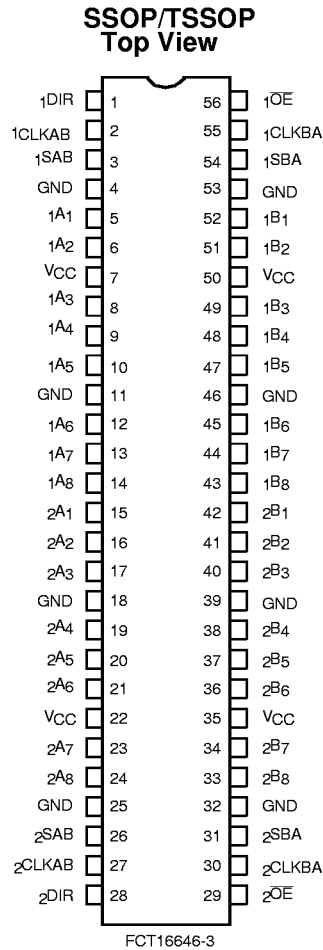
The CY74FCT162646T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162646T is ideal for driving transmission lines.
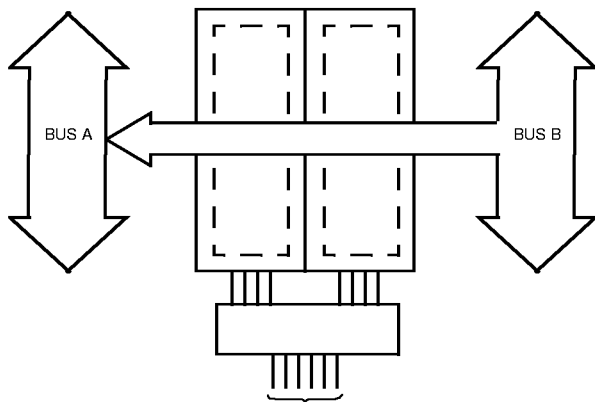
## Logic Block Diagrams



TO 7 OTHER CHANNELS    FCT16646-1

TO 7 OTHER CHANNELS    FCT16646-2

## Pin Configuration

**SSOP/TSSOP**
**Top View**

| | | |
|---|---|---|
| 1DIR | 1 | 56 | 1OE |
| 1CLKAB | 2 | 55 | 1CLKBA |
| 1SAB | 3 | 54 | 1SBA |
| GND | 4 | 53 | GND |
| 1A1 | 5 | 52 | 1B1 |
| 1A2 | 6 | 51 | 1B2 |
| VCC | 7 | 50 | VCC |
| 1A3 | 8 | 49 | 1B3 |
| 1A4 | 9 | 48 | 1B4 |
| 1A5 | 10 | 47 | 1B5 |
| GND | 11 | 46 | GND |
| 1A6 | 12 | 45 | 1B6 |
| 1A7 | 13 | 44 | 1B7 |
| 1A8 | 14 | 43 | 1B8 |
| 2A1 | 15 | 42 | 2B1 |
| 2A2 | 16 | 41 | 2B2 |
| 2A3 | 17 | 40 | 2B3 |
| GND | 18 | 39 | GND |
| 2A4 | 19 | 38 | 2B4 |
| 2A5 | 20 | 37 | 2B5 |
| 2A6 | 21 | 36 | 2B6 |
| VCC | 22 | 35 | VCC |
| 2A7 | 23 | 34 | 2B7 |
| 2A8 | 24 | 33 | 2B8 |
| GND | 25 | 32 | GND |
| 2SAB | 26 | 31 | 2SBA |
| 2CLKAB | 27 | 30 | 2CLKBA |
| 2DIR | 28 | 29 | 2OE |

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## Pin Description

| Pin Names | Description |
|---|---|
| A | Data Register A Inputs<br>Data Register B Outputs |
| B | Data Register B Inputs<br>Data Register A Outputs |
| CLKAB, CLKBA | Clock Pulse Inputs |
| SAB, SBA | Output Data Source Select Inputs |
| DIR | Direction |
| OE | Output Enable (Active LOW) |

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# CY74FCT16646T
# CY74FCT162646T

## Function Table[1]

| Inputs | | | | | | Data I/O[2] | | Function |
|---|---|---|---|---|---|---|---|---|
| OE | DIR | CLKAB | CLKBA | SAB | SBA | A | B | |
| H | X | H or L | H or L | X | X | Input | Input | Isolation |
| H | X | ↑ | ↑ | X | X | | | Store A and B Data |
| L | L | X | X | X | L | Output | Input | Real Time B Data to A Bus |
| L | L | X | H or L | X | H | | | Stored B Data to A Bus |
| L | H | X | X | L | X | Input | Output | Real Time A Data to Bus |
| L | H | H or L | X | H | X | | | Stored A Data to B Bus |

| DIR | OE | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**Real-Time Transfer
Bus B to Bus A**
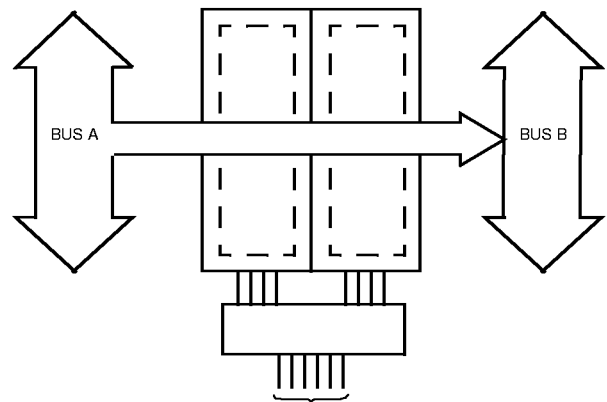
| DIR | OE | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | L | X | X | L | X |

**Real-Time Transfer
Bus A to Bus B**
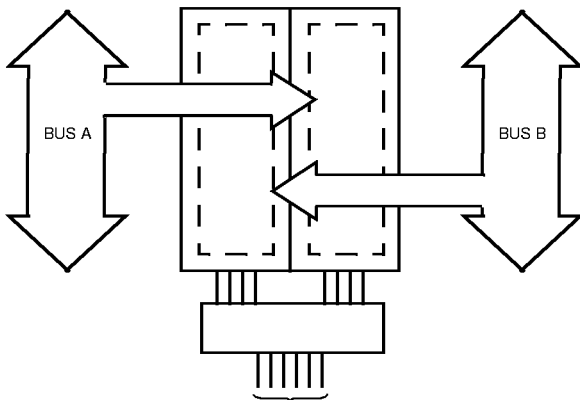
| DIR | OE | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | L | ↑ | X | X | X |
| L | L | X | ↑ | X | X |
| X | H | ↑ | ↑ | X | X |

**Storage from
A and/or B**
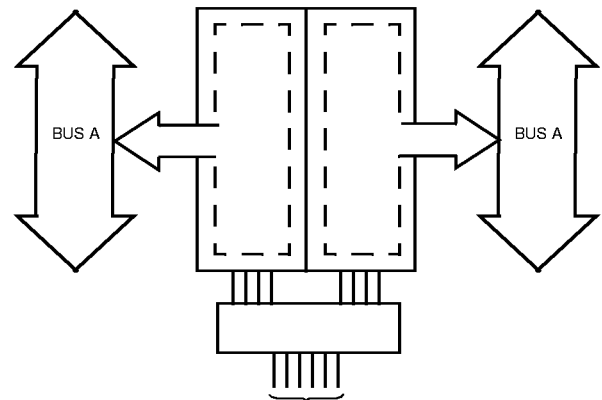
| DIR[3] | OE | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | H or L | X | H |
| H | L | H or L | X | H | X |

**Transfer Stored Data
to A and/or B**

**Notes:**
1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care ⌐ = LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the OE or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
3. Cannot transfer data to A-bus and B-bus simultaneously.

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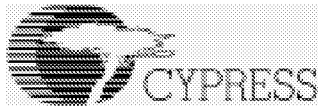
## Maximum Ratings[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....................Com'l −55°C to +125°C

Ambient Temperature with
Power Applied.................................Com'l −55°C to +125°C

DC Input Voltage ................................................−0.5V to +7.0V

DC Output Voltage .............................................−0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) ...........................−60 to +120 mA

Power Dissipation ..........................................................1.0W

Static Discharge Voltage ..........................................>2001V
(per MIL-STD-883, Method 3015)

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Industrial | −40°C to +85°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ.[5] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $V_H$ | Input Hysteresis[6] | | | 100 | | mV |
| $V_{IK}$ | Input Clamp Diode Voltage | $V_{CC}$=Min., $I_{IN}$=−18 mA | | −0.7 | −1.2 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$=Max., $V_I$=$V_{CC}$ | | | ±1 | μA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$=Max., $V_I$=GND | | | ±1 | μA |
| $I_{OZH}$ | High Impedance Output Current (Three-State Output pins) | $V_{CC}$=Max., $V_{OUT}$=2.7V | | | ±1 | μA |
| $I_{OZL}$ | High Impedance Output Current (Three-State Output pins) | $V_{CC}$=Max., $V_{OUT}$=0.5V | | | ±1 | μA |
| $I_{OS}$ | Short Circuit Current[7] | $V_{CC}$=Max., $V_{OUT}$=GND | −80 | −140 | −200 | mA |
| $I_O$ | Output Drive Current[7] | $V_{CC}$=Max., $V_{OUT}$=2.5V | −50 | | −180 | mA |
| $I_{OFF}$ | Power-Off Disable | $V_{CC}$=0V, $V_{OUT}$≤4.5V[9] | | | ±1 | μA |

## Output Drive Characteristics for CY74FCT16646T

| Parameter | Description | Test Conditions | Min. | Typ.[5] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$=Min., $I_{OH}$=−3 mA | 2.5 | 3.5 | | V |
| | | $V_{CC}$=Min., $I_{OH}$=−15 mA | 2.4 | 3.5 | | V |
| | | $V_{CC}$=Min., $I_{OH}$=−32 mA | 2.0 | 3.0 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$=Min., $I_{OL}$=64 mA | | 0.2 | 0.55 | V |

## Output Drive Characteristics for CY74FCT162646T

| Parameter | Description | Test Conditions | Min. | Typ.[5] | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{ODL}$ | Output LOW Current[7] | $V_{CC}$=5V, $V_{IN}$=$V_{IH}$ or $V_{IL}$, $V_{OUT}$=1.5V | 60 | 115 | 150 | mA |
| $I_{ODH}$ | Output HIGH Current[7] | $V_{CC}$=5V, $V_{IN}$=$V_{IH}$ or $V_{IL}$, $V_{OUT}$=1.5V | −60 | −115 | −150 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$=Min., $I_{OH}$=−24 mA | 2.4 | 3.3 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$=Min., $I_{OL}$=24 mA | | 0.3 | 0.55 | V |

**Notes:**
4. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Typical values are at $V_{CC}$= 5.0V, $T_A$= +25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.
8. This parameter is measured at characterization but not tested.
9. Tested at +25°C.

4
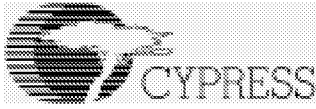
## Capacitance ($T_A$ = +25°C, f = 1.0 MHz)

| Symbol | Description[8] | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6.0 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ =0V | 5.5 | 8.0 | pF |

## Power Supply Characteristics

| Parameter | Description | Test Conditions[10] | | Min. | Typ.[5] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$=Max. | $V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC}-0.2V$ | — | 5 | 500 | μA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC}$ = Max. $V_{IN}$=3.4V[11] | | — | 0.5 | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[12] | $V_{CC}$=Max. Outputs Open DIR=OE=GND One-Bit Toggling 50% Duty Cycle | $V_{IN}$=$V_{CC}$ or $V_{IN}$=GND | — | 75 | 120 | μA/MHz |
| $I_C$ | Total Power Supply Current[13] | $V_{CC}$=Max. Outputs Open $f_o$=10 MHz (CLKBA) 50% Duty Cycle DIR=$\overline{OE}$=GND One-Bit Toggling $f_1$=5 MHz 50% Duty Cycle | $V_{IN}$=$V_{CC}$ or $V_{IN}$=GND | — | 0.8 | 1.7 | mA |
| | | | $V_{IN}$=3.4V or $V_{IN}$=GND | — | 1.3 | 3.2 | |
| | | $V_{CC}$=Max. Outputs Open $f_o$=10 MHz (CLKBA) 50% Duty Cycle DIR=$\overline{OE}$=GND Sixteen-Bits Toggling $f_1$=2.5 MHz 50% Duty Cycle | $V_{IN}$=$V_{CC}$ or $V_{IN}$=GND | — | 3.8 | 6.5[14] | |
| | | | $V_{IN}$=3.4V or $V_{IN}$=GND | — | 8.3 | 20.0[14] | |

**Notes:**
10. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
11. Per TTL driven input ($V_{IN}$=3.4V); all other inputs at $V_{CC}$ or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
13. $I_C$ = $I_{QUIESCENT}$ + $I_{INPUTS}$ + $I_{DYNAMIC}$
    $I_C$ = $I_{CC}$+$\Delta I_{CC}D_H N_T$+$I_{CCD}$($f_o$/2 + $f_1 N_1$)
    $I_{CC}$ = Quiescent Current with CMOS input levels
    $\Delta I_{CC}$ = Power Supply Current for a TTL HIGH input ($V_{IN}$=3.4V)
    $D_H$ = Duty Cycle for TTL inputs HIGH
    $N_T$ = Number of TTL inputs at $D_H$
    $I_{CCD}$ = Dynamic Current caused by an input transition pair (HLH or LHL)
    $f_o$ = Clock frequency for registered devices, otherwise zero
    $f_1$ = Input signal frequency
    $N_1$ = Number of inputs changing at $f_1$
    All currents are in milliamps and all frequencies are in megahertz.
14. Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.

## Switching Characteristics Over the Operating Range[15]

| Parameter | Description | CY74FCT16646T CY74FCT162646T Min. | Max. | CY74FCT16646AT CY74FCT162646AT Min. | Max. | Unit | Fig. No.[16] |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Bus to Bus | 1.5 | 9.0 | 1.5 | 6.3 | ns | 1, 2 |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time DIR or $\overline{OE}$ to Bus | 1.5 | 14.0 | 1.5 | 9.8 | ns | 1, 7, 8 |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time DIR or $\overline{OE}$ to Bus | 1.5 | 9.0 | 1.5 | 6.3 | ns | 1, 7, 8 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Clock to Bus | 1.5 | 9.0 | 1.5 | 6.3 | ns | 1, 5 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay SBA or SAB to Bus | 1.5 | 11.0 | 1.5 | 7.7 | ns | 1,5 |
| $t_{SU}$ | Set-Up Time HIGH or LOW Bus to Clock | 2.0 | — | 2.0 | — | ns | 4 |
| $t_{H}$ | Hold Time HIGH or LOW Bus to Clock | 1.5 | — | 1.5 | — | ns | 4 |
| $t_{W}$ | Clock Pulse Width HIGH or LOW | 5.0 | — | 5.0 | — | ns | 6 |
| $t_{SK(O)}$ | Output Skew[17] | — | 0.5 | — | 0.5 | ns | — |

| Parameter | Description | CY74FCT16646CT CY74FCT162646CT Min. | Max. | CY74FCT16646ET CY74FCT162646ET Min. | Max. | Unit | Fig. No.[16] |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Bus to Bus | 1.5 | 5.4 | 1.5 | 3.8 | ns | 1, 2 |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time DIR or $\overline{OE}$ to Bus | 1.5 | 7.8 | 1.5 | 4.8 | ns | 1, 7, 8 |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time DIR or $\overline{OE}$ to Bus | 1.5 | 6.3 | 1.5 | 4.0 | ns | 1, 7, 8 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Clock to Bus | 1.5 | 5.7 | 1.5 | 3.8 | ns | 1, 5 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay SBA or SAB to Bus | 1.5 | 6.2 | 1.5 | 4.2 | ns | 1,5 |
| $t_{SU}$ | Set-Up Time HIGH or LOW Bus to Clock | 2.0 | — | 2.0 | — | ns | 4 |
| $t_{H}$ | Hold Time HIGH or LOW Bus to Clock | 1.5 | — | 0.0 | — | ns | 4 |
| $t_{W}$ | Clock Pulse Width HIGH or LOW | 5.0 | — | 3.0 | — | ns | 6 |
| $t_{SK(O)}$ | Output Skew[17] | — | 0.5 | — | 0.5 | ns | — |

**Notes:**
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. See "Parameter Measurement Information" in the General Information section.
17. Skew any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

## Ordering Information CY74FCT16646

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 3.8 | CY74FCT16646ETPAC | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16646ETPVC | O56 | 56-Lead (300-Mil) SSOP | |
| 5.4 | CY74FCT16646CTPAC | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16646CTPVC | O56 | 56-Lead (300-Mil) SSOP | |
| 6.3 | CY74FCT16646ATPAC | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16646ATPVC | O56 | 56-Lead (300-Mil) SSOP | |
| 9.0 | CY74FCT16646TPAC | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16646TPVC | O56 | 56-Lead (300-Mil) SSOP | |

## Ordering Information CY74FCT162646

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 3.8 | CY74FCT162646ETPAC | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162646ETPVC | O56 | 56-Lead (300-Mil) SSOP | |
| 5.4 | CY74FCT162646CTPAC | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162646CTPVC | O56 | 56-Lead (300-Mil) SSOP | |
| 6.3 | CY74FCT162646ATPAC | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162646ATPVC | O56 | 56-Lead (300-Mil) SSOP | |
| 9.0 | CY74FCT162646TPAC | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162646TPVC | O56 | 56-Lead (300-Mil) SSOP | |

Document #: 38-00383-C

## Package Diagrams

### 56-Lead Shrunk Small Outline Package O56

.020

3  2  1

0.400
0.410

0.292
0.299

N

DIMENSIONS IN INCHES  MIN.
MAX.

0.720
0.730

0.088
0.092

0.095
0.110

.010

GAUGE PLANE

0.025
BSC

0.008
0.0135

0.008
0.016

SEATING PLANE

0.024
0.040

0°–8°

### 56-Lead Thin Shrunk Small Outline Package Z56

0.0098

3  2  1

0.313
0.325

0.236
0.244

N

DIMENSIONS IN INCHES  MIN.
MAX.

0.547
0.555

0.0433
MAX.

0.25
REF.

0.0335
0.0374

0.0197
BSC

0.0067
0.011

0.002
0.006

SEATING
PLANE

0.020
0.030

0°–8°