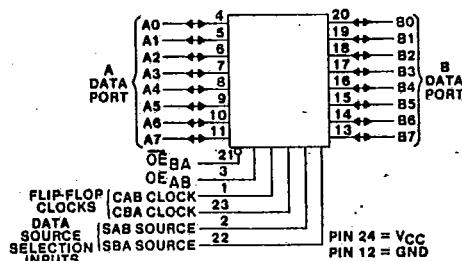


**CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654**

T-52-31

Advance Information



FUNCTIONAL DIAGRAM 92CS-42677

**Octal-Bus Transceivers/Registers,
Open-Drain (A Side), 3-State (B Side)**

CD54/74AC/ACT653 - Inverting
 CD54/74AC/ACT654 - Non-Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
5.3 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST[®]/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5 V to 5.5 V operation and balanced noise immunity at 30% of the supply
- ± 24 mA output drive current
 - Fanout to 15 FAST[®] ICs
 - Drives 50-ohm transmission lines

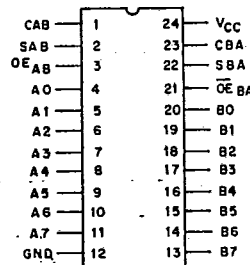
*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC653 and CD54/74AC654 and the CD54/74ACT653 and CD54/74ACT654 octal-bus transceivers/registers use the RCA ADVANCED CMOS technology. The CD54/74AC653 and CD54/74ACT653 are inverting types having open drains on the A outputs and 3-state outputs on the B side. The CD54/74AC654 and CD54/74ACT654 differ only in that these are non-inverting types. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE_{AB} and OE_{BA} are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and OE_{BA}. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD74AC/ACT653 and CD74AC/ACT654 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70° C); Industrial (-40 to +85° C); and Extended Industrial/Military (-55 to +125° C).

The CD54AC/ACT653 and CD54AC/ACT654, available in chip form (H suffix), are operable over the -55 to +125° C temperature range.



92CS-42670

TERMINAL ASSIGNMENT



File Number 1975

321

Technical Data

T-52-31

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

FUNCTION TABLE

INPUTS				DATA I/O				OPERATION OR FUNCTION	
OE _{AB}	OE _{BA}	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	653	654
L	H	H or L	H or L	X	X	Input	Input	Isolation*	Isolation*
L	H			X	X	Input	Input	Store A and B Data	Store A and B Data
X	H		H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H			X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L		X	X	Unspecified†	Input	Hold A, Store B	Hold, A Store B
L	L			X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

- * To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.
- † The data output functions may be enabled or disabled by various signals at the OE_{AB} or OE_{BA} inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- ‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V _{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I _{IK} (for V _I < -0.5 V or V _I > V _{CC} + 0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I _{OK} (for V _O < -0.5 V or V _O > V _{CC} + 0.5 V)	±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I _O (for V _O > -0.5 V or V _O < V _{CC} + 0.5 V)	±50 mA
DC V _{CC} or GROUND CURRENT (I _{CC} or I _{END})	±100 mA*
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -55 to +100°C (PACKAGE TYPE E)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +70°C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A)	-55 to +125°C
STORAGE TEMPERATURE (T _{STG})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C
Unit inserted into PC board mln. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	+300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V _{CC} †: (For T _A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V _I , V _O	0	V _{CC}	V
Operating Temperature, T _A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

†Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

T-52-31

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage V _{IH}			1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage V _{IL}			1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage (B Side) V _{OH}	V _{IH} or V _{IL}	#, *	-0.05	1.5	1.4	—	1.4	—	1.4	V	
			-0.05	3	2.9	—	2.9	—	2.9		
			-0.05	4.5	4.4	—	4.4	—	4.4		
			-4	3	2.58	—	2.48	—	2.4		
			-24	4.5	3.94	—	3.8	—	3.7		
			-75	5.5	—	—	3.85	—	—		
			-50	5.5	—	—	—	—	3.85		
Low-Level Output Voltage V _{OL}	V _{IH} or V _{IL}	#, *	0.05	1.5	—	0.1	—	0.1	—	V	
			0.05	3	—	0.1	—	0.1	—		
			0.05	4.5	—	0.1	—	0.1	—		
			12	3	—	0.36	—	0.44	—		0.5
			24	4.5	—	0.36	—	0.44	—		0.5
			75	5.5	—	—	—	1.65	—		—
			50	5.5	—	—	—	—	—		1.65
Input Leakage Current I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA	
3-State or Off-State Leakage Current I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA	

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#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
 *Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

T-52-31

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	V _{CC} (V)	AMBIENT TEMPERATURE (T _a) - °C						UNITS		
			+25		-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V _{IH}		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V _{IL}		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage (B Side)	V _{OH}	V _{IH} or V _{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _I	V _{CC} or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State or Off-State Leakage Current	I _{oz}	V _{IH} or V _{IL} V _O =V _{CC} or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin, TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

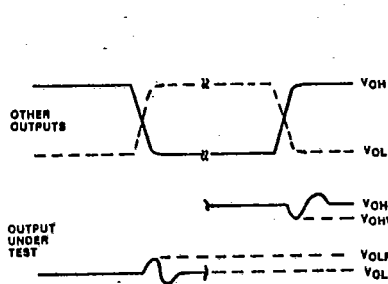
INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
OE _{AB}	0.67
OE _{BA}	1.17
A _n , B _n	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

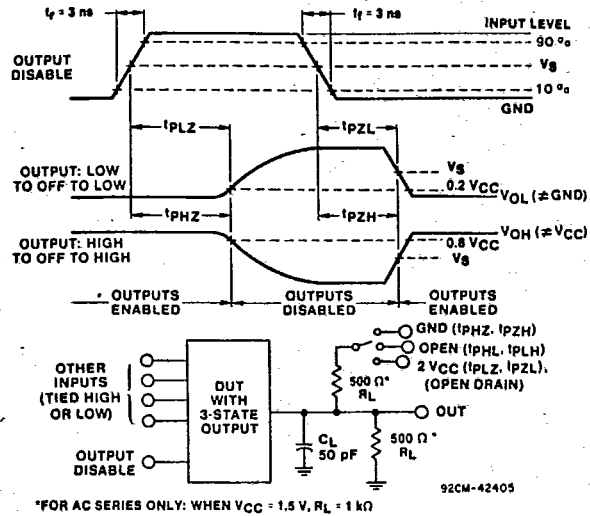
T-52-31

PARAMETER MEASUREMENT INFORMATION



- NOTES:
 1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
 2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
 PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
 3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.
 IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406



92CM-42405

*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit (B outputs).

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f _{max}	1.5	11	—	10	—	MHz
		3.3*	101	—	89	—	
		5†	143	—	125	—	
Setup Time Data to Clock	t _{su}	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time Data to Clock	t _h	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Clock Pulse Width Data to Clock	t _w	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	

* 3.3 V: min. is @ 3 V
 † 5 V: min. is @ 4.5 V

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Technical Data

T-52-31

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Stored A Data to B Bus (653) Stored A Data to B Bus (654)	t _{PLH}	1.5	—	153	—	169	ns
	t _{PHL}	3.3*	4.9	17.2	4.7	18.9	
	t _{PHL}	5†	3.5	12.3	3.4	13.5	
Stored B Data to A Bus (653) Stored B Data to A Bus (654)	t _{PZL}	1.5	—	153	—	169	ns
	t _{PZL}	3.3	5.2	18.4	5.1	20.2	
	t _{PZL}	5	3.5	12.3	3.4	13.5	
A Data to B Bus (653) A Data to B Bus (654)	t _{PLZ}	1.5	—	166	—	183	ns
	t _{PLZ}	3.3	4.7	16.6	4.6	18.3	
	t _{PLZ}	5	3.8	13.3	3.7	14.6	
B Data to A Bus (653) B Data to A Bus (654)	t _{PLH}	1.5	—	125	—	138	ns
	t _{PHL}	3.3	4	14	3.9	15.4	
	t _{PHL}	5	2.8	10	2.8	11	
B Data to A Bus (653) B Data to A Bus (654)	t _{PZL}	1.5	—	125	—	138	ns
	t _{PZL}	3.3	4.2	15	4.1	16.5	
	t _{PZL}	5	2.8	10	2.8	11	
Select to Data (B Bus) (653/654)	t _{PLZ}	1.5	—	137	—	151	ns
	t _{PLZ}	3.3	3.9	13.7	3.8	15.1	
	t _{PLZ}	5	3.1	11	3	12.1	
Select to Data (A Bus) (653/654)	t _{PLH}	1.5	—	136	—	150	ns
	t _{PHL}	3.3	4.3	15.3	4.2	16.8	
	t _{PHL}	5	3.1	10.9	3	12	
3-State Enabling/ Disabling Time (B Bus) Bus to Output or Register to Output (653/654)	t _{PZL}	1.5	—	136	—	150	ns
	t _{PZH}	3.3	4.6	16.4	4.5	18	
	t _{PZH}	5	3.1	10.9	3	12	
Off-State Enabling/ Disabling Time (A Bus) Bus to Output or Register to Output (653/654)	t _{PLZ}	1.5	—	149	—	164	ns
	t _{PLZ}	3.3	4.2	14.9	4.1	16.4	
	t _{PLZ}	5	3.4	11.9	3.3	13.1	
Power Dissipation Capacitance	C _{PD} §	—	150 Typ.		150 Typ.		pF
Min. (Valley) V _{OH} (B Side) During Switching of Other Outputs (Output Under Test No Switching)	V _{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C _I	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	C _O	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	C _O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = V_{CC}^2 C_{PD} f_i + \sum (V_{CC}^2 C_L f_o)$$

where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

T-52-3/

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f _{max}	5*	125	—	110	—	MHz
Setup Time Data to Clock	t _{SU}	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t _H	5	2	—	2	—	ns
Clock Pulse Width	t _w	5	3.9	—	4.5	—	ns

*5 V:min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Stored A Data to B Bus (653) Stored A Data to B Bus (654)	t _{PLH} t _{PHL}	5*	4	14.1	3.9	15.5	ns
Stored B̄ Data to A Bus (653) Stored B Data to A Bus (654)	t _{PZL} t _{PLZ}	5	4	14.1	3.9	15.5	ns
A Data to B̄ Bus (653) A Data to B Bus (654)	t _{PLH} t _{PHL}	5	3.2	11.4	3.1	12.5	ns
B̄ Data to A Bus (653) B Data to A Bus (654)	t _{PZL} t _{PLZ}	5	3.2	11.4	3.1	12.5	ns
Select to Data (B Bus) (653) (654)	t _{PLH} t _{PHL}	5	4 3.7	14.1 13.2	3.9 3.6	15.5 14.5	ns
Select to Data (A Bus) (653/654)	t _{PZL} t _{PLZ}	5	4 4.3	14.1 15.1	3.9 4.2	15.5 16.6	ns
3-State Enabling/ Disabling Time (B Bus) Bus to Output or Register to Output (653/654)	t _{PZL} t _{PZH} t _{PLZ} t _{PHZ}	5	4	14.1	3.9	15.5	ns
Off-State Enabling/ Disabling Time (A Bus) Bus to Output or Register to Output (653/654)	t _{PZL} t _{PLZ}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C _{PD§}	—	150 Typ.		150 Typ.		pF
Min. (Valley) V _{OH} (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V _{OHV} See Fig. 1.	5	4 Typ. @ 25°C				V
Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Fig. 1	5	1 Typ @ 25°C				V
Input Capacitance	C _I	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	C _O	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	C _O	—	—	15	—	15	pF

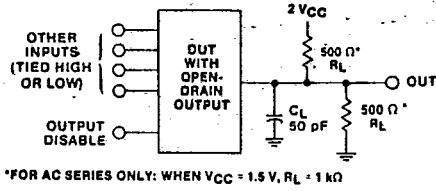
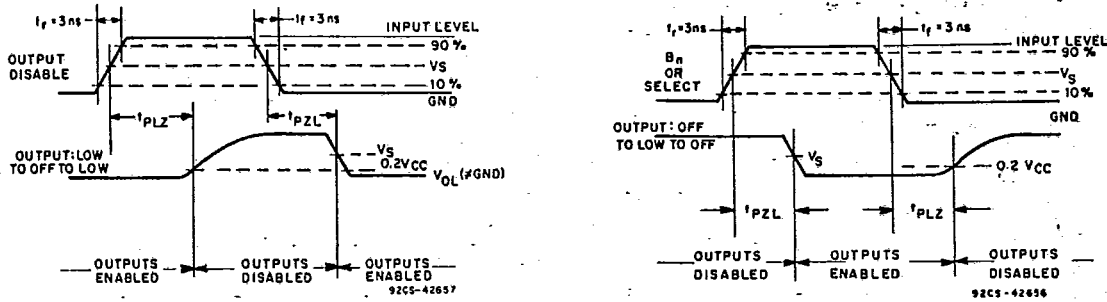
* Min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
 $P_o = V_{cc}^2 C_{PD} f_i + \sum V_{cc}^2 C_L f_o + V_{cc} \Delta I_{cc}$ where
 f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{cc} = supply voltage.

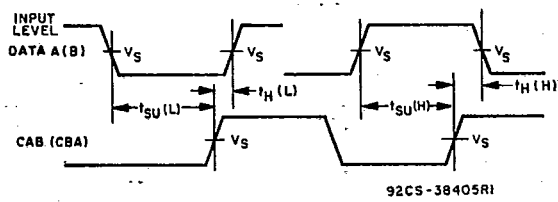
Technical Data

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

T-52-31



92CS-42610
Fig. 3 - Open-drain propagation delay times and test circuit (A outputs).

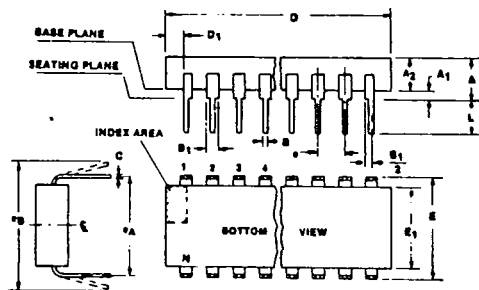


92CS-38405R1
Fig. 4 - Data setup and hold times.

	CD54/74AC	CD54/74ACT
Input Level	V _{CC}	3 V
Input Switching Voltage, V _S	0.5 V _{CC}	1.5 V
Output Switching Voltage, V _S	0.5 V _{CC}	0.5 V _{CC}

Dual-In-Line Plastic Packages

T-90-20



(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
 $1, N, \frac{N}{2}, \frac{N}{2} + 1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E₁ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D₁ at the left end of the package must equal dimension D₁ at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

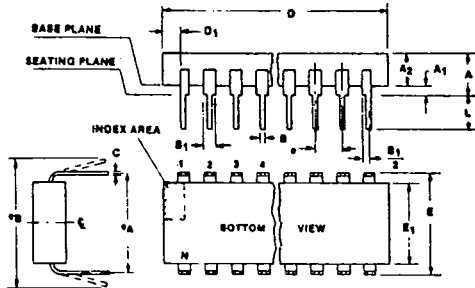
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

Dual-In-Line Plastic Packages

T-90-20

(E) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E₁ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around

center line shown in end view.

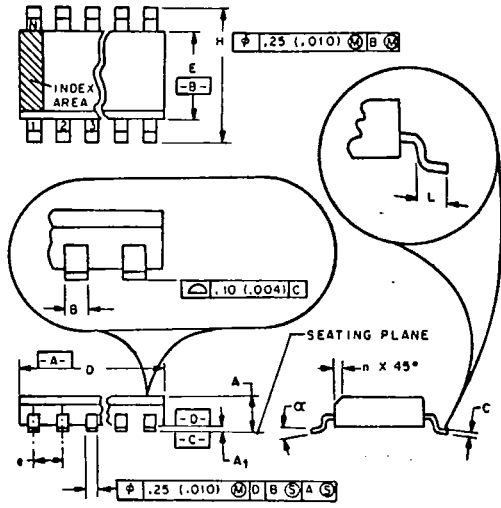
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D₁ at the left end of the package must equal dimension D₁ at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.



Dimensional Outlines

Dual-In-Line Small-Outline Plastic Packages

T-90-20



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

M Suffix (JEDEC MS-012AB)
14-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A ₁	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0° 8°		0° 8°		

Notes: 1, 2, 3, 8, 9

92CS-38924R2

M Suffix (JEDEC MS-012AC)
16-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A ₁	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0° 8°		0° 8°		

Notes: 1, 2, 3, 8, 9

92CS-38925R2

M Suffix (JEDEC MS-013AC)
20-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A ₁	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4861	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0° 8°		0° 8°		

Notes: 1, 2, 3, 8, 9

92CS-38926R2

M Suffix (JEDEC MS-013AD)
24-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A ₁	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0° 8°		0° 8°		

Notes: 1, 2, 3, 8, 9

92CS-39037R2