Data Sheet

ADBT1001

4-Channel AFE, Digital Controller, and PWM for Battery Formation and Testing

FEATURES

- Precise measurement of the voltage and current
- 4 PWM control channels up to 16 bits (effective) resolution
  - Selectable synchronous and asynchronous rectifier operation
  - Programmable dead time compensation
  - Programmable switching frequency from 62.5 kHz to 500 kHz in powers of 2 steps
- Multiphase operation
  - Interchip digital current sharing
  - Interchip frequency synchronization
- Digital control loop
  - Programmable PID loop filters
  - Fast dc bus voltage feedforward
- Integrated spectrum analysis per channel
  - Measure load impedance
- SPI port control and status interface
  - Host interrupt on programmable status changes
- CC, CV, CP, and CR operating modes
  - 15-bit setpoint resolution
  - Input and output inrush current protection
- External NTC thermistor temperature sensing
  - Internal die temperature measurement
- User calibration of input voltages and currents
- 0°C to 85°C operation

APPLICATIONS

- Battery formation and testing
- High efficiency battery test systems with recycle capability
- Battery conditioning (charging and discharging) systems

GENERAL DESCRIPTION

The ADBT1001 is a flexible, feature rich digital controller that targets high volume battery testing and formation manufacturing and precision battery test instrumentation applications. The ADBT1001 is optimized for minimal component count, maximum flexibility, and minimum design time. Features include differential remote voltage sense, current sense, pulse-width modulation (PWM) generation, frequency synchronization, overvoltage protection (OVP), and current sharing. Programmable protection features include overcurrent protection (OCP), OVP limiting, and external overtemperature protection (OTP).

Parameters can be programmed over the serial peripheral interface (SPI), providing extensive programming of the integrated loop filter, PWM signal timing, and soft start timing. The SPI provides access to the many monitoring and system test functions. Reliability is improved through a built-in checksum and programmable protection circuits.

A comprehensive graphical user interface (GUI) is provided for simple system and channel configuration and programming of the safety features. The ADBT1001 is available in a 100-lead LQFP_EP.

TYPICAL APPLICATION DIAGRAM

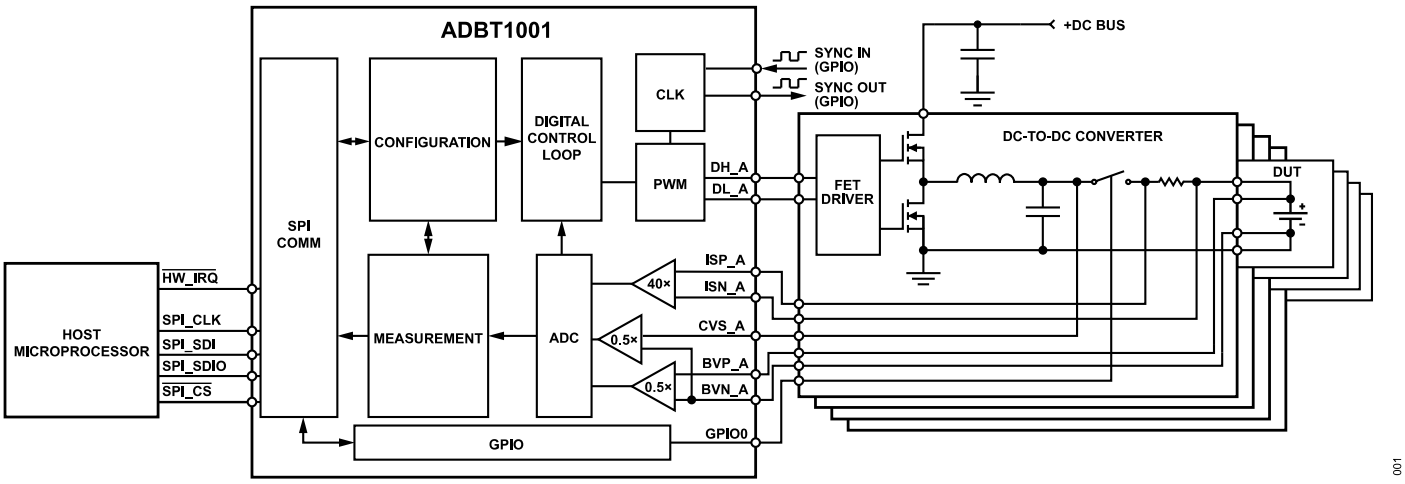

Figure 1.

Rev. 0

DOCUMENT FEEDBACK

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REVISION HISTORY

6/2021—Revision 0: Initial Version

SPECIFICATIONS

AHVDD = 15 V, AHVSS = −15 V, VDDIO = AVDD = DVDD = 3.3 V, and T_A = 0°C to 85°C, unless otherwise noted.

ANALOG FRONT END AND CONTROLLER SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SENSE CHANNEL					
Gain			40		V/V
Gain Error	Output voltage (V_{OUT}) =±2 V			0.2	%
Gain Drift				7	ppm/°C
System Input Offset Voltage[1]		−10		+10	LSB
System Input Offset Voltage Drift	RTI			0.235	LSB/°C
Input Bias Current	V_{ICM} = reference voltage (V_{REF})/2		30	500	nA
Input Differential Voltage Range		−62.5		+62.5	mV
Input Common-Mode Voltage Range		AHVSS + 5		AHVDD − 5	V
Differential Input Impedance	By design		24		kΩ
Common-Mode Input Impedance	By design		246		kΩ
Input Resistance	Both input pins		492		kΩ
Common-Mode Rejection Ratio (CMRR)		100	110		dB
CMRR Drift				0.05	ppm/°C
Small Signal −3 dB Bandwidth (Gain = 40)[2]	T_A = 25°C, V_{OUT} = 100 mV p-p		600		kHz
Power Supply Rejection Ratio (PSRR)	Supply voltage (Vs) = ±5 V to ±18 V	120			dB
Slew Rate	V_{OUT} = ±2 V		0.6		V/µs
Readout Data Signal-to-Noise Ratio (SNR)	MAF[3] = 16, FIR[4] on				
Update Rate[5]					
31.25 kHz (OSR = 32)			78		dB
15.625 kHz (OSR = 64)			81		dB
7.8125 kHz (OSR = 128)			84		dB
3.90625 kHz (OSR = 256)			87		dB
Full-Scale Input Range		−60		+60	mV
VOLTAGE SENSE AND CAPACITOR VOLTAGE SENSE CHANNEL					
Gain			0.5		V/V
Gain Error	V_{OUT} = ±2 V			0.2	%
Gain Drift				10	ppm/°C
System Input Offset Voltage[1]		−10		+10	LSB
Offset Voltage Drift				0.235	LSB/°C
Input Common-Mode Voltage Range		AHVSS + 5		AHVDD − 5	V
Differential Input Impedance	By design	0.85	1		MΩ
Common-Mode Input Impedance	By design		375		kΩ
Input Resistance	Noninverting pin		750		kΩ
	Inverting pin		375		kΩ
Small Signal −3 dB Bandwidth (G = 0.5)[6]	T_A = 25°C, V_{OUT} = 100 mV p-p		200		kHz
CMRR					
BVx_x		80	90		dB
CVS_x		78	90		dB

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMRR Drift					
BVx_x				0.235	ppm/°C
CVS_x				3	ppm/°C
PSRR		100	120		dB
Slew Rate			0.15		V/µs
Power Dissipation			30		mW
Readout Data SNR	MAF = 16, FIR on				
Update Rate					
31.25 kHz (OSR = 32)			91		dB
15.625 kHz (OSR = 64)			92		dB
7.8125 kHz (OSR = 128)			93		dB
3.90625 kHz (OSR = 256)			93		dB
Full-Scale Input Range		−4.8		+4.8	V
BATTERY CURRENT AND VOLTAGE ADCS	V_{REF} = 2.5 V				
SNR	1 kHz sine wave at 80% full scale		82		dB
Signal-to-Noise-and-Distortion (SINAD) Ratio			82		dB
Resolution			16		Bits
Differential Nonlinearity (DNL)[7, 8]		−1		+1	LSB
Integral Nonlinearity (INL)	Internal voltage reference	−6		+6	LSB
Sampling Rate			1		MHz/Channel
VOLTAGE REFERENCE (INTERNAL)					
Voltage Range		2.495	2.500	2.505	V
Temperature Coefficient			7	11	ppm/°C
RMS Noise	REFCAP = 1 µF		7		µV rms
PULSE-WIDTH MODULATION (PWM)	External CLK = 16 MHz				
Resolution			16		Bits
Switching Frequency	f_{SW}	62.5		500	kHz
Programmable Dead Time	Minimum		0		ns
	Maximum		992.2		ns
Dead Time Resolution[9]			7.8125		ns
Delay from External SYNC (Programmable)	Minimum[10]		0		µs
	Maximum at f_{SW} = 62.5 kHz[11]		16		µs
Delay Resolution			7.8125		ns
Effective Phase Shift Resolution					
f_{SW} = 62.5 kHz			0.176		Degrees
f_{SW} = 125 kHz			0.352		Degrees
f_{SW} = 250 kHz			0.703		Degrees
f_{SW} = 500 kHz			1.406		Degrees
CHANNEL AC PERFORMANCE					
Loop Bandwidth (Cross over Frequency)			10	50	kHz
Constant Current (CC) to Constant Voltage (CV) Transition Time	f_{SW} = 500 kHz		2		µs
	f_{SW} = 62.5 kHz		16		µs
Channel to Channel Isolation			96		dB
Intrachannel Isolation			90		dB
Current and Voltage Readout Rate[12]	Minimum OSR[13]		31,250		Samples/sec
	Maximum OSR		15.26		Samples/sec
Output Data Resolution			18		Bits

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AUXILIARY ADC					
Resolution (Effective)			12		Bits
Sampling Rate	DC bus monitor disabled		100,000		Samples/sec
	DC bus monitor enabled		50,000		Samples/sec
Input Voltage Range[14]		0.1		2.4	V
Unity-Gain Offset		−1		+1	LSB
Unity-Gain Offset Drift				0.02	LSB/°C
Current Excitation (4-Bit Programmable)	Minimum		0		µA
	Maximum		750		µA
Resolution			50		µA
LOGIC INPUTS ($\overline{SPI\_CS}$, SPI_SCK, SPI_SDIO, SPI_SDO, $\overline{FAULT\_x}$, GPIOx, AND $\overline{HW\_IRQ}$)	Hysteresis = 600 mV				
Input Voltage High (V_{IH})		VDDIO × 0.8			V
Input Voltage Low (V_{IL})				VDDIO × 0.2	V
Input Current High (I_{IH})	V_{IN} = VDDIO	−1			µA
Input Current Low (I_{IL})	V_{IN} = DVSS			1	µA
Input Pull-Down Current ($\overline{HW\_IRQ}$ Only)			15	115	µA
Input Capacitance			4		pF
LOGIC OPEN-DRAIN OUTPUTS (SPI_SDIO, SPI_SDO, AND $\overline{HW\_IRQ}$)	1 mA load				
Output Low Voltage (V_{OL})				0.4	V
Output High Leakage Current (I_{OH})			±0.1	±1.0	µA
LOGIC OUTPUTS (GPIO)	1 mA load				
Output Low Voltage (V_{OL})				0.4	V
Output High Leakage Current (I_{OH})			±0.1	±1.0	µA
Output High Voltage (V_{OH})	VDDIO = 3.0 V		3		V
	VDDIO = 3.3 V		3.3		V
	VDDIO = 3.6 V		3.6		V
Slew Rate[15]	Default settings				
Falling Edge			5.2		ns
Rising Edge			4		ns
Internal Oscillator Frequency			16		MHz
External Oscillator Frequency			16		MHz
Power Supplies					
AHVDD		4.5		30.7	V
Quiescent Current	Active and standby		3	4.2	mA
AHVSS		−26		−4.5	V
	Active and standby		4	6	mA
High Voltage Supply Range (AHVDD to AHVSS)		10.6		36	V
AVDD		3	3.3	3.6	V
	Active		40	47	mA
	Standby		3.6	4.5	mA
AVSS			0		V
VDDIO			3.3		V
	Active and standby		2	6	µA
VDDDRV			3.3		V
	Active		4.6	4.8	mA
	Standby		26	30	µA

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DVDD			3.3		V
	Active		21	22	mA
	Standby		4.8	5.2	mA
Power Dissipation					
AHVDD	AHVDD = 12 V, active and standby		50.4		mW
AHVSS	AHVSS = −12 V, active and standby		63.6		mW
VDDIO	Active and standby		19.8		µW
AVDD	Active		155		mW
	Standby		14.9		mW
DVDD	Active		72.6		mW
	Standby		17.2		mW
VDDDRV	Active		15.8		mW
	Standby		99		µW
PWM DRIVE LOGIC					
DLx and DHx Drive Voltage[16]	PWM_DRV = 0				
V_{OH}	0 mA load	3	3.29	3.3	V
	15 mA load	2.6	2.8	2.9	V
V_{OL}	0 mA load		17	25	mV
	15 mA load	0.6	0.8	1	V
DL_x and DH_x Sink Resistance	PWM_DRV = 0	10	23	40	Ω
	PWM_DRV = 15	1.8	2.6	5	Ω
DL_x and DH_x Source Resistance	PWM_DRV = 0	30	41	55	Ω
	PWM_DRV = 15	2.2	3.2	5.1	Ω
Internal Pull-Down Resistance			1		MΩ
Drive Capacitive Load		10		100	pF

[1] Factory calibration after ADC.

[2] Bandwidth is analog only. The readout data bandwidth is limited by the selected over sampling rate (OSR).

[3] The moving average filter (MAF) is a 3-bit field in the MAF_CFG register (one per channel). The default value is 8.

[4] The finite impulse response (FIR) filter in the readout filter is not bypassed (default).

[5] The readout filter update rate is selected in a 5-bit field in the DSP_READOUT_FILT_CFG register.

[6] The bandwidth is analog only. The readout data bandwidth is limited by the selected OSR.

[7] Guaranteed by design.

[8] No missing codes.

[9] For sync mode only.

[10] CHANNEL_A_PHASE = 0x000 in the PMU_CHANNEL CFG1 register.

[11] The 11-bit CHANNEL_A_PHASE in the PMU_CHANNEL_CFG1 register = 0x07FF and is the same for other channels.

[12] The readout update rate is set in a 5-bit field in the DSP_READOUT_FILT_CFG register. There is one per channel.

[13] Minimum OSR is based on the maximum readout rate of the current and voltage data for all four channels.

[14] Based on 2.5 V nominal V_{REF}.

[15] The output pins (SPI_SDIO, SPI_SDO, GPIOx, EXTCLKIO, and $\overline{\text{HW\_IRQ}}$) have xxx_PAD_CFG registers with a 3-bit xxx_SLEW bitfield. The default is 0x7, which is the fastest slew rate.

[16] PWM_DRV is a 4-bit field in the PWM_CFG1 channel register.

SPECIFICATIONS

Table 2. SPI Bus Timing

Parameter	Symbol	Min	Typ	Max	Unit
TIMING REQUIREMENTS					
Set-Up $\overline{\text{SPI\_CS}}$ to SPI_CLK Edge	t_S		4		ns
Minimum SPI_CLK Low Pulse Width	t_{LO}		31.25		ns
Minimum SPI_CLK High Pulse Width	t_{HI}		31.25		ns
Minimum SPI_CLK Period	t_{CLK}		62.5		ns
Data Input Setup Time Before SPI_CLK Edge	t_{DS}		4		ns
Data Input Hold Time After SPI_CLK Edge	t_{DH}		4		ns
Hold SCLK to $\overline{\text{SPI\_CS}}$ Deactivate	t_H		4		ns
SWITCHING CHARACTERISTICS					
Data Output Valid After SPI_CLK Edge	t_{ACCESS}		4		ns
$\overline{\text{SPI\_CS}}$ to SPI_SDIO/SPI_SDO High-Z	t_Z		4		ns

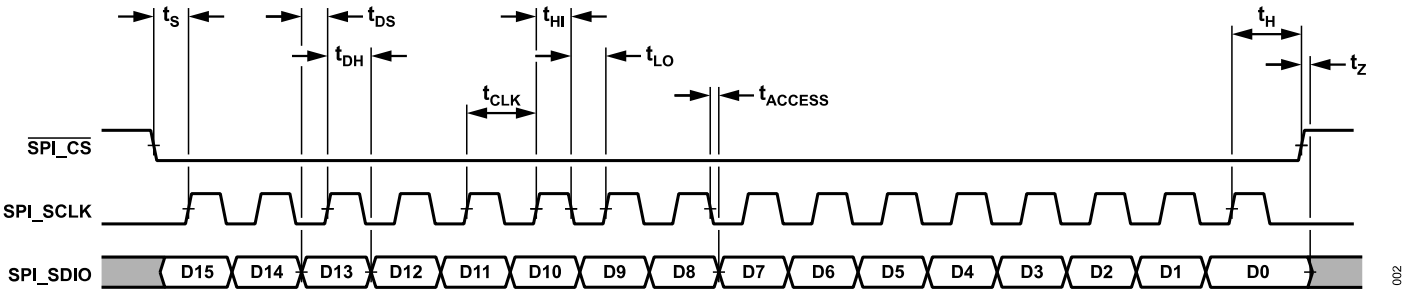


Figure 2. 3-Wire SPI Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog High Voltage Supply (Continuous), AHVDD − AHVSS	50 V
AHVDD − AVSS	50 V
AVSS − AHVSS	30 V
Input Pin Voltages (ISP_x, ISN_x, BVP_x, BVN_x, and CVS_x)	−0.3 V + AHVSS to AHVDD + 0.3 V
Digital Pins (Relative to DVSS)	−0.3 V to DVDD + 0.3 V
Analog Input Pins (AINx Relative to AIN_COM)	−0.3 V to AVDD + 0.3 V
DVSS and AVSS	−0.3 V to +0.3 V
DVDD, AVDD, and VDDDRV	−0.3 V to DVDD + 0.3 V
SPI_SCK, $\overline{\text{SPI\_CS}}$, SPI_SDIO, and SPI_SDO	−0.3 V to DVDD + 0.3 V
REFIO	−0.3 V to AVDD + 0.3 V
Temperature	
Operating Range	0°C to +85°C
Storage Range	−65°C to +150°C
Junction	125°C
Peak Solder Reflow	
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
SW-100-2	27.8	3.9	°C/W

SOLDERING

It is important to follow the correct guidelines when laying out the PCB footprint for the ADBT1001 and when soldering the device onto the PCB. For detailed information about these guidelines, see the EE-352 Engineer-to-Engineer Note.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADBT1001

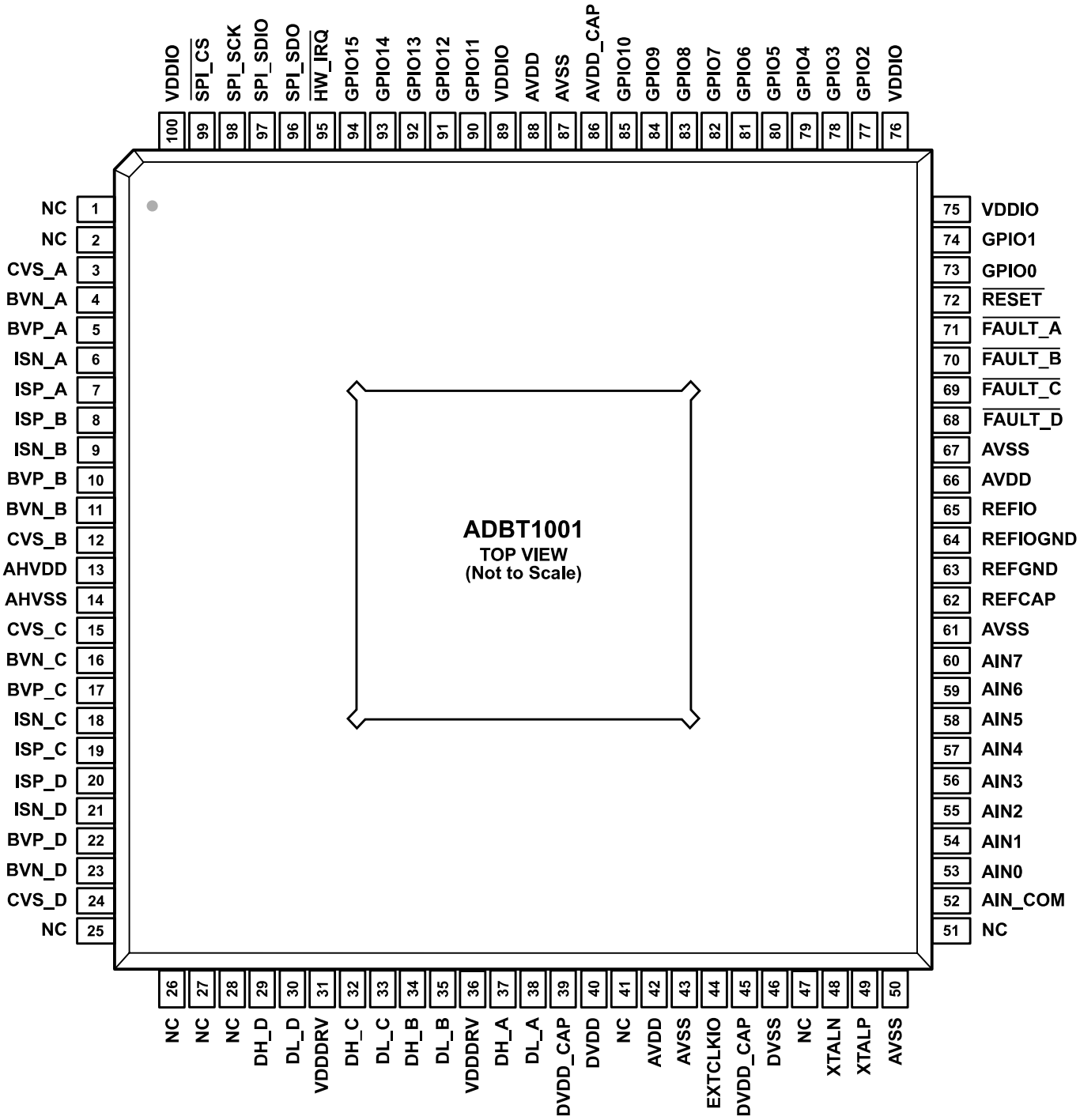
Table 5. ADBT1001, 100-Lead LQFP_EP

ESD Model	Withstand Threshold	Class
HBM	1.5 kV	1C
CDM	750 V	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC MEANS NO CONNECT.
2. EXPOSED PAD. DVSS FOR DVDD, VDDIO, AND VDDDRV.

003

Figure 3. Pin Configuration

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	NC	No Connect.
3	CVS_A	Channel A Capacitor Voltage Sense Input.
4	BVN_A	Channel A Voltage Sense Negative Input.
5	BVP_A	Channel A Voltage Sense Positive Input.
6	ISN_A	Channel A Current Sense Negative Input.
7	ISP_A	Channel A Current Sense Positive Input.
8	ISP_B	Channel B Current Sense Positive Input.
9	ISN_B	Channel B Current Sense Negative Input.
10	BVP_B	Channel B Voltage Sense Positive Input.
11	BVN_B	Channel B Voltage Sense Negative Input.
12	CVS_B	Channel B Capacitor Voltage Sense Input.
13	AHVDD	AFE Positive Supply.
14	AHVSS	AFE Negative Supply. Ensure AVDD is applied before applying AHVSS.
15	CVS_C	Channel C Capacitor Voltage Sense Input.
16	BVN_C	Channel C Voltage Sense Negative Input.
17	BVP_C	Channel C Voltage Sense Positive Input.
18	ISN_C	Channel C Current Sense Negative Input.
19	ISP_C	Channel C Current Sense Positive Input.
20	ISP_D	Channel D Current Sense Positive Input.
21	ISN_D	Channel D Current Sense Negative Input.
22	BVP_D	Channel D Voltage Sense Positive Input.
23	BVN_D	Channel D Voltage Sense Negative Input.
24	CVS_D	Channel D Capacitor Voltage Sense Input.
25	NC	No Connect.
26	NC	No Connect.
27	NC	No Connect.
28	NC	No Connect.
29	DH_D	PWM Drive High, Channel D.
30	DL_D	PWM Drive Low, Channel D.
31	VDDDRV	PWM Driver Supply.
32	DH_C	PWM Drive High, Channel C
33	DL_C	PWM Drive Low, Channel C.
34	DH_B	PWM Drive High, Channel B.
35	DL_B	PWM Drive Low, Channel B.
36	VDDDRV	PWM Driver Supply.
37	DH_A	PWM Drive High, Channel A.
38	DL_A	PWM Drive Low, Channel A.
39	DVDD_CAP	Digital Supply Source Capacitor. Connect a 10 µF decoupling capacitor from DVDD_CAP to DVSS.
40	DVDD	Digital Supply Source, 3.3 V Typical.
41	NC	No Connect.
42	AVDD	Analog Supply Source, 3.3 V Typical. Ensure AVDD is applied before applying AHVSS.
43	AVSS	Analog Supply Return.
44	EXTCLKIO	External Oscillator Input and Clock Output.
45	DVDD_CAP	Digital Supply Source Capacitor. Connect a 10 µF decoupling capacitor from DVDD_CAP to DVSS.
46	DVSS	Digital Supply Return.
47	NC	No Connect.
48	XTALP	External Crystal High-Side Excitation Pin.
49	XTALN	External Crystal Low-Side Excitation Pin.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
50	AVSS	Analog Supply Return.
51	NC	No Connect.
52	AIN_COM	Analog Input, ADC Common.
53	AIN0	Analog Input, ADC Channel 0.
54	AIN1	Analog Input, ADC Channel 1.
55	AIN2	Analog Input, ADC Channel 2.
56	AIN3	Analog Input, ADC Channel 3.
57	AIN4	Analog Input, ADC Channel 4.
58	AIN5	Analog Input, ADC Channel 5.
59	AIN6	Analog Input, ADC Channel 6.
60	AIN7	Analog Input, ADC Channel 7.
61	AVSS	Analog Power Return.
62	REFCAP	Internal Reference Capacitor.
63	REFGND	Internal Reference Ground.
64	REFIOGND	Ground for Reference Input and Output.
65	REFIO	Reference Input and Output. Connect a 10 µF from REFIO to AVSS.
66	AVDD	Analog Power Supply. Ensure AVDD is applied before applying AHVSS.
67	AVSS	Analog Power Return.
68	$\overline{\text{FAULT\_D}}$	Fault Detect Input, PWM Channel D Shutdown. Active low.
69	$\overline{\text{FAULT\_C}}$	Fault Detect Input, PWM Channel C Shutdown. Active low.
70	$\overline{\text{FAULT\_B}}$	Fault Detect Input, PWM Channel B Shutdown. Active low.
71	$\overline{\text{FAULT\_A}}$	Fault Detect Input, PWM Channel A Shutdown. Active low.
72	$\overline{\text{RESET}}$	Chip Reset. Active low.
73	GPIO0	General-Purpose Digital Input and Output 0.
74	GPIO1	General-Purpose Digital Input and Output 1.
75	VDDIO	Input and Output Supply.
76	VDDIO	Input and Output Supply.
77	GPIO2	General-Purpose Digital Input and Output 2.
78	GPIO3	General-Purpose Digital Input and Output 3.
79	GPIO4	General-Purpose Digital Input and Output 4.
80	GPIO5	General-Purpose Digital Input and Output 5.
81	GPIO6	General-Purpose Digital Input and Output 6.
82	GPIO7	General-Purpose Digital Input and Output 7.
83	GPIO8	General-Purpose Digital Input and Output 8.
84	GPIO9	General-Purpose Digital Input and Output 9.
85	GPIO10	General-Purpose Digital Input and Output 10.
86	AVDD_CAP	Analog Power Return Capacitor. Connect a 10 µF decoupling capacitor from AVDD_CAP to AVSS.
87	AVSS	Analog Power Return.
88	AVDD	Analog Power Supply. Ensure AVDD is applied before applying AHVSS.
89	VDDIO	Digital Input and Output Supply.
90	GPIO11	General-Purpose Digital Input and Output 11.
91	GPIO12	General-Purpose Digital Input and Output 12.
92	GPIO13	General-Purpose Digital Input and Output 13.
93	GPIO14	General-Purpose Digital Input and Output 14.
94	GPIO15	General-Purpose Digital Input and Output 15.
95	$\overline{\text{HW\_IRQ}}$	Host Interrupt Request. Active low.
96	SPI_SDO	Host SPI Master Input, Slave Output (MISO).
97	SPI_SDIO	Host SPI Master Output, Slave Input (MOSI) or Bidirectional.
98	SPI_SCK	Host SPI Clock.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
99	$\overline{\text{SPI\_CS}}$	Host SPI Select. Active low.
100	VDDIO	Input and Output Supply.
EPAD	DVSS	Exposed Pad. DVSS for DVDD, VDDIO, and VDDDRV.

TYPICAL PERFORMANCE CHARACTERISTICS

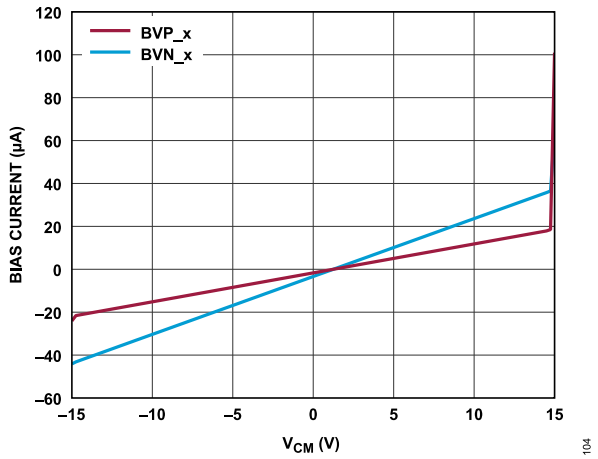


Figure 4. BVx_x Bias Current vs. Common-Mode Voltage (V_{CM})

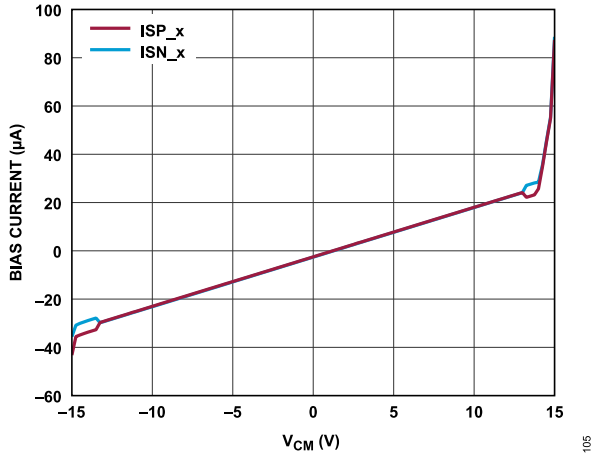


Figure 5. ISx_x Bias Current vs. V_{CM}

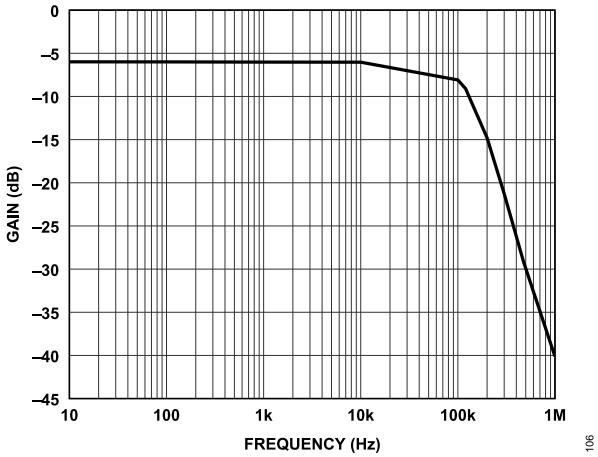


Figure 6. BVx_x Gain vs. Frequency

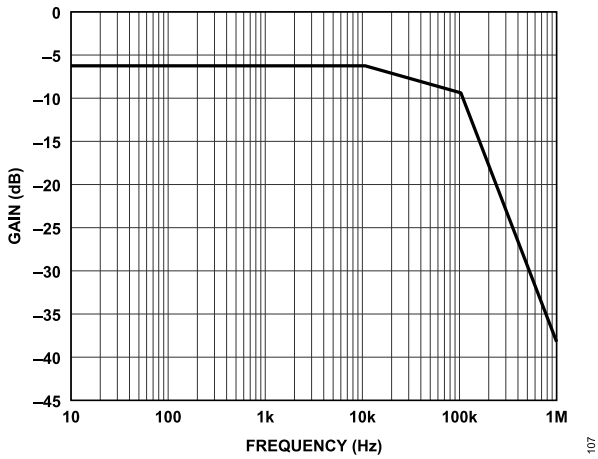


Figure 7. CVS_x Gain vs. Frequency

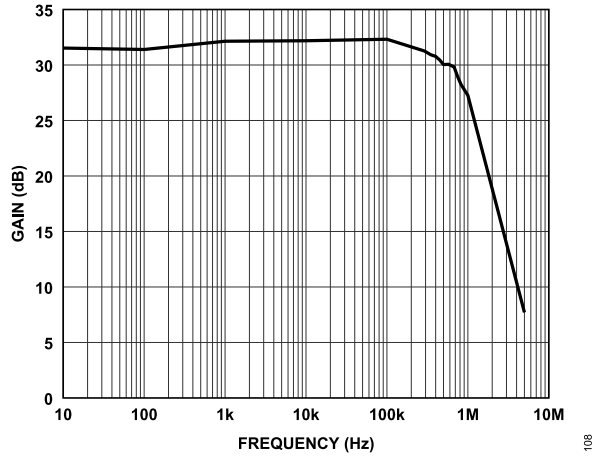


Figure 8. ISx_x Gain vs. Frequency

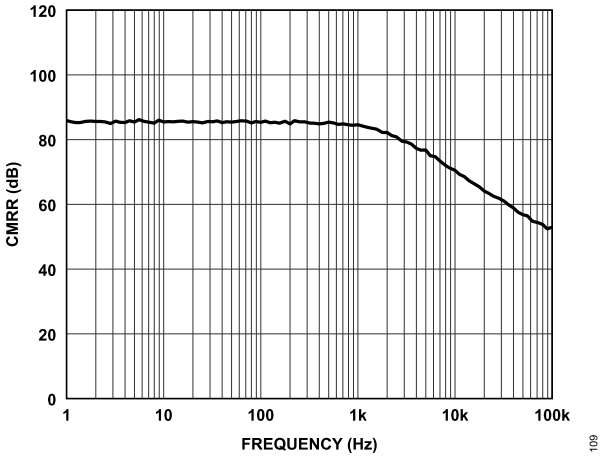


Figure 9. BVx_x CMRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

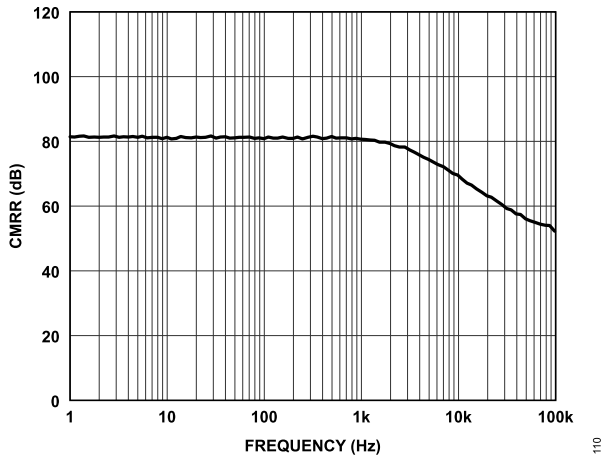


Figure 10. CVS_x CMRR vs. Frequency

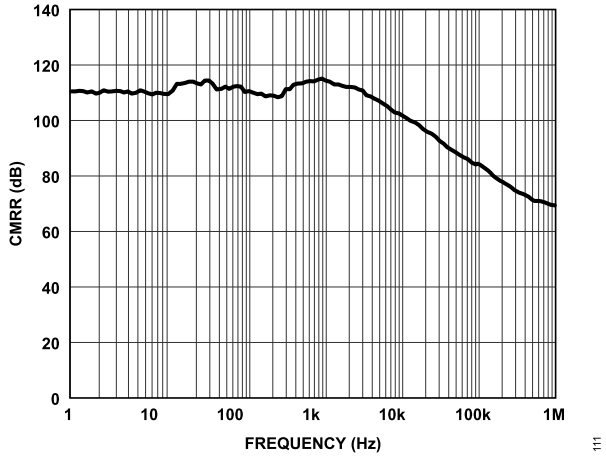


Figure 11. ISx_x CMRR vs. Frequency

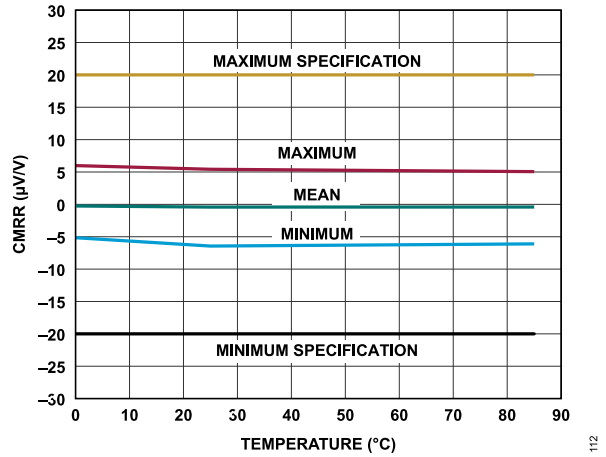


Figure 12. BVx_x CMRR vs. Temperature

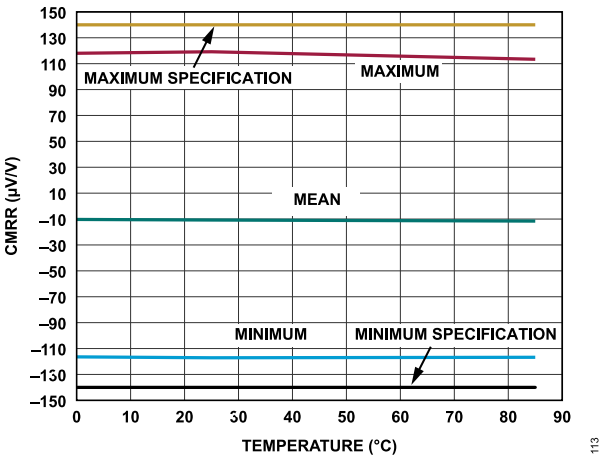


Figure 13. CVS_x CMRR vs. Temperature

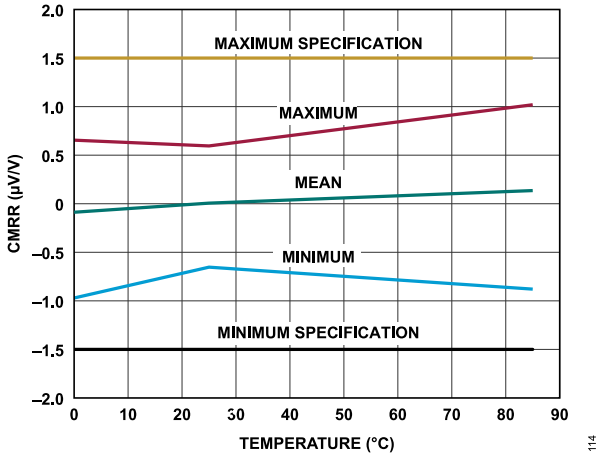


Figure 14. ISx_x CMRR vs. Temperature

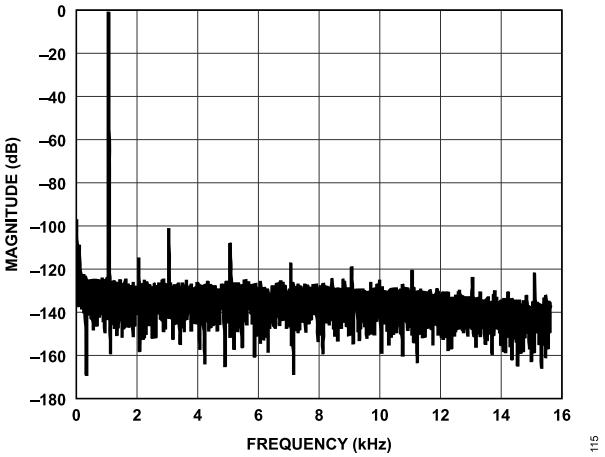


Figure 15. BVx_x Amplifier Fast Fourier Transform (FFT)

TYPICAL PERFORMANCE CHARACTERISTICS

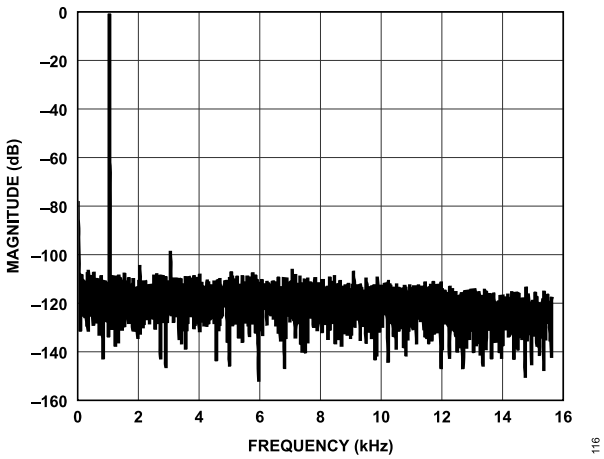


Figure 16. ISx_x Amplifier FFT

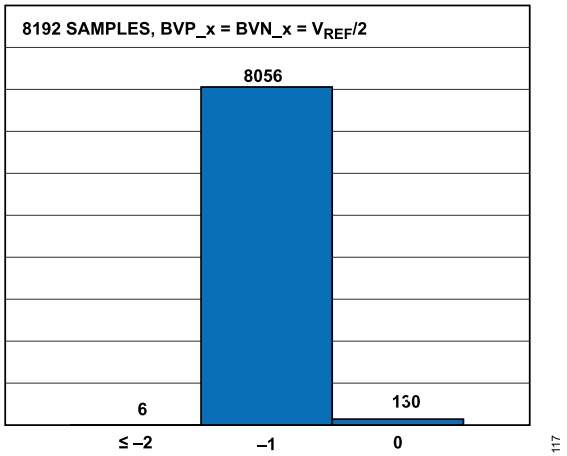


Figure 17. BVx_x Channel Histogram Codes at Code Center

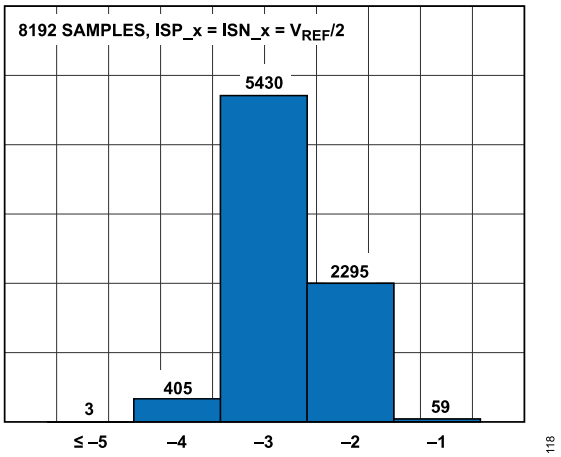


Figure 18. ISx_x Channel Histogram Codes at Code Center

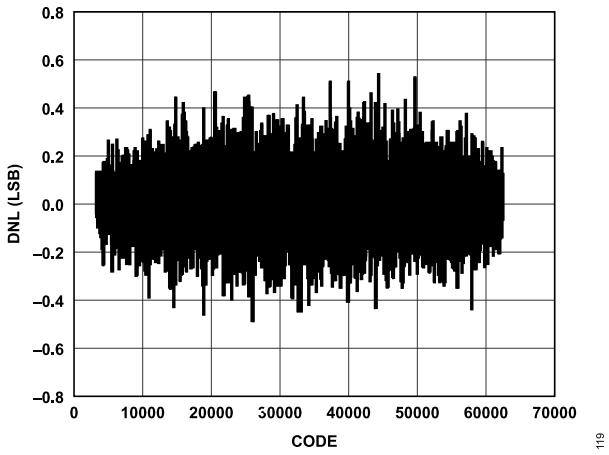


Figure 19. BVx_x Amplifier Full System DNL

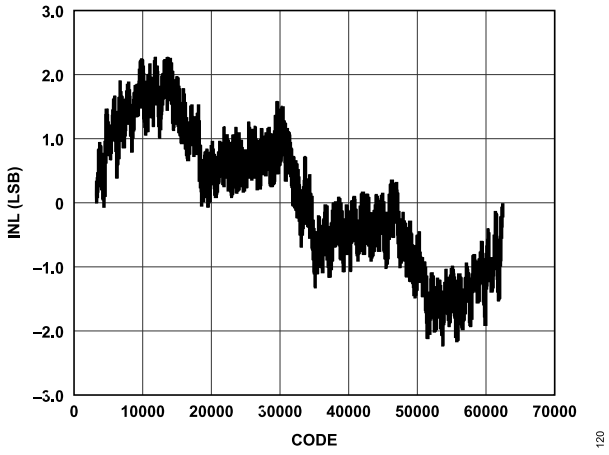


Figure 20. BVx_x Amplifier Full System INL

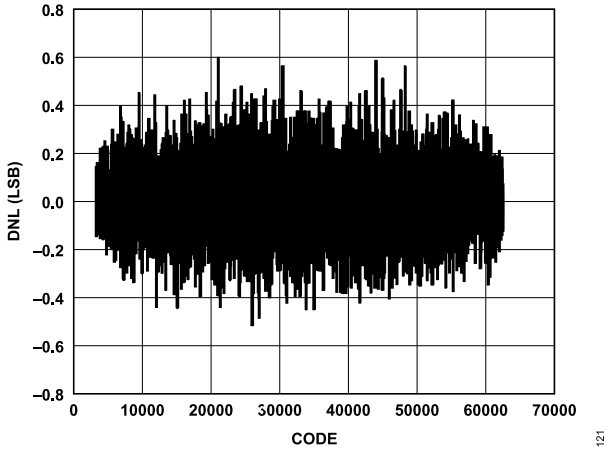


Figure 21. ISx_x Amplifier Full System DNL

TYPICAL PERFORMANCE CHARACTERISTICS

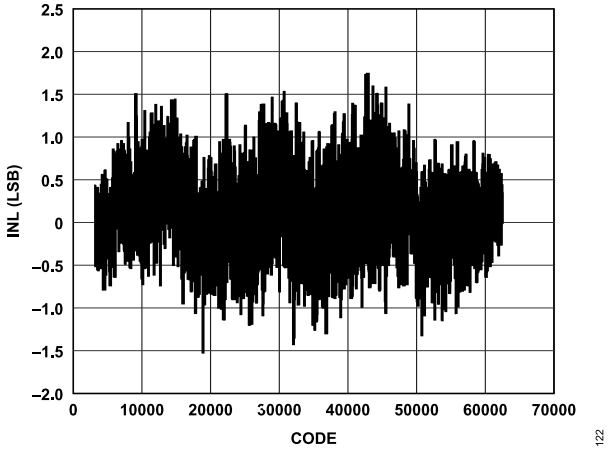


Figure 22. ISx_x Amplifier Full System INL

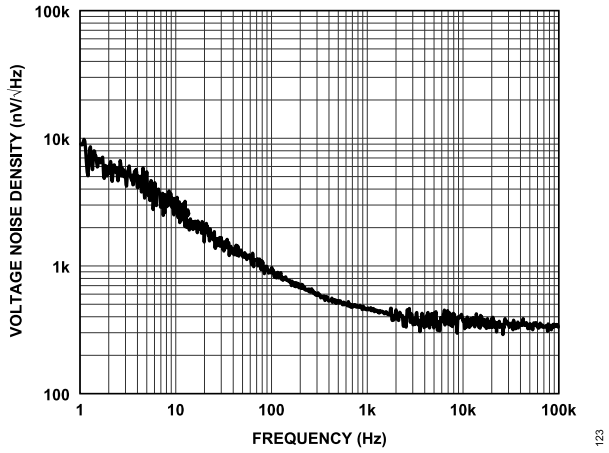


Figure 23. BVx_x Voltage Noise Density vs. Frequency, G = 0.5

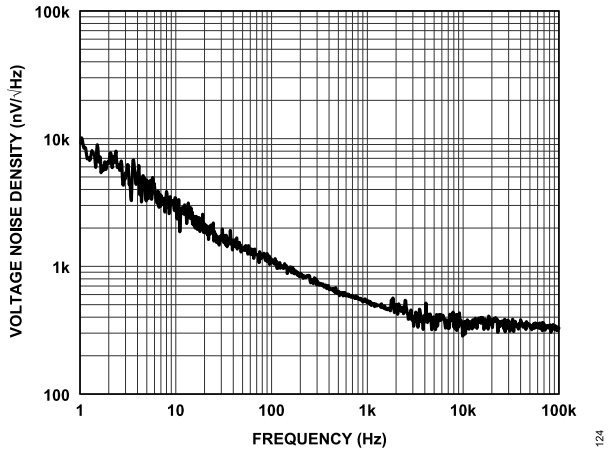


Figure 24. CVS_x Voltage Noise Density vs. Frequency, G = 0.5

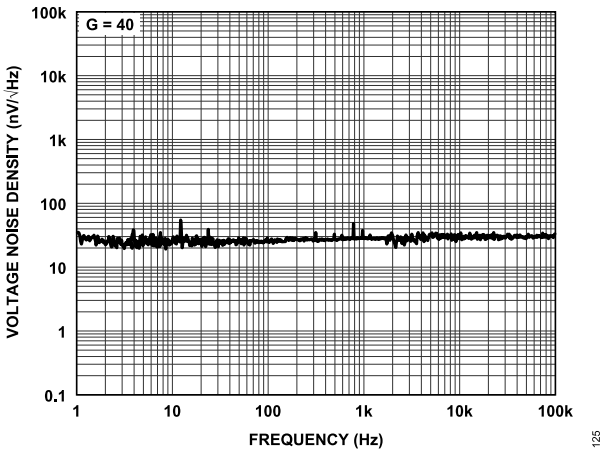


Figure 25. ISx_x Voltage Noise Density vs. Frequency, G = 40

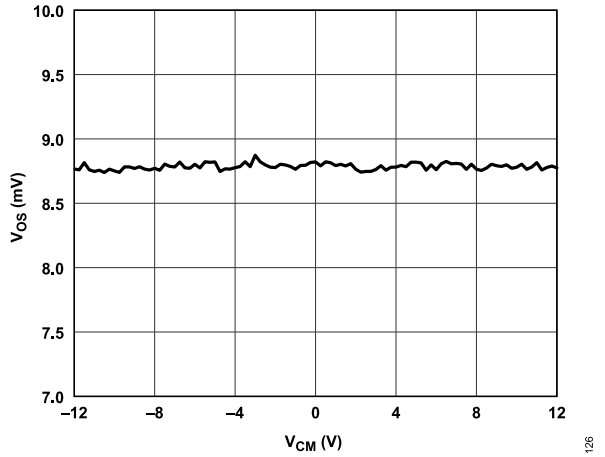


Figure 26. BVx_x Amplifier V_{OS} vs. V_{CM}

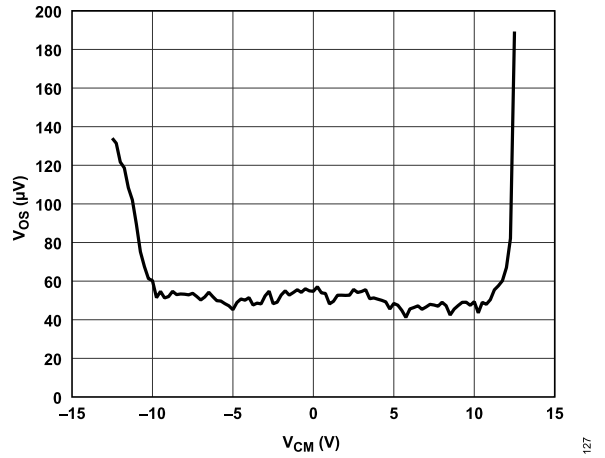


Figure 27. ISx_x Amplifier Offset Voltage (V_{OS}) vs. V_{CM}

TYPICAL PERFORMANCE CHARACTERISTICS

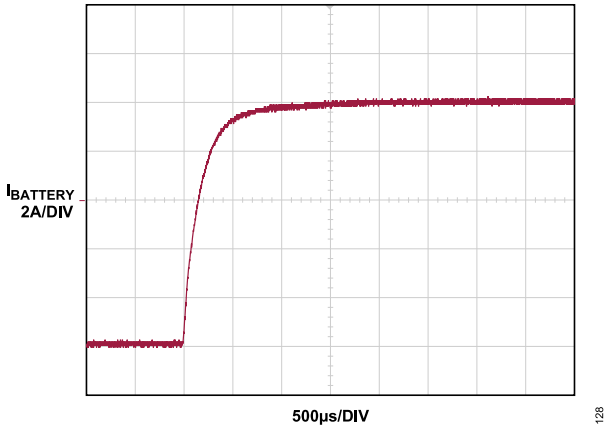


Figure 28. 10 A Step Charge Example in Synchronous Mode, 10 A System Demonstration with 10 AH LiFePO$_4$ ($I_{BATTERY}$ Is the Battery Current)

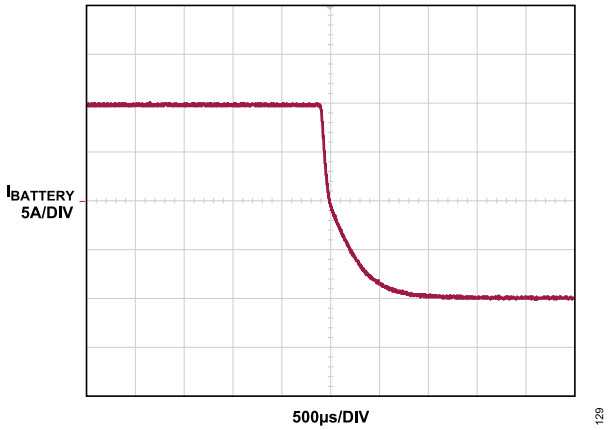


Figure 29. Charge to Discharge Transition Example in Synchronous Mode, 10 A System Demonstration with 10 AH LiFePO$_4$

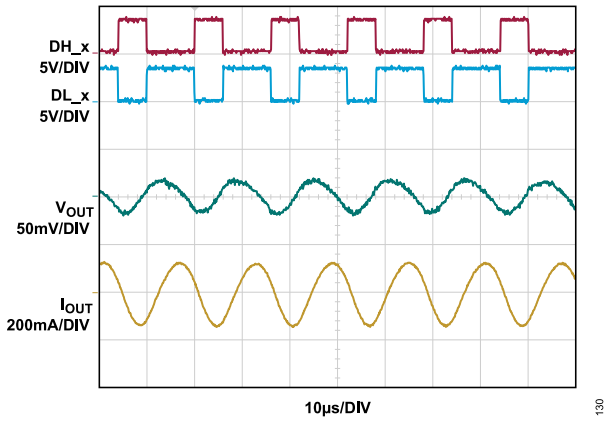


Figure 30. Typical 10 A CC Ripple at 62.5 kHz, 10 A System Demonstration with 10 AH LiFePO$_4$ (I_{OUT} Is the Output Current)

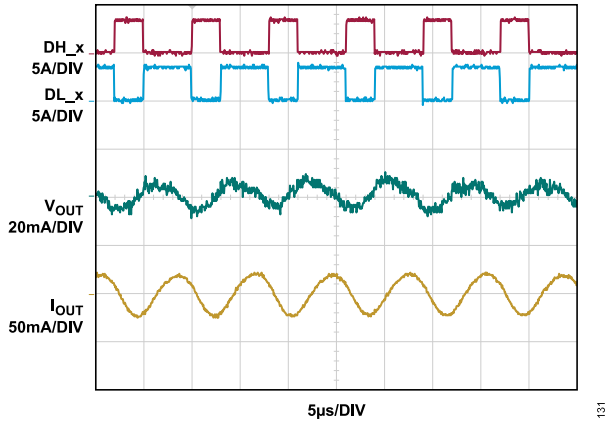


Figure 31. Typical 10 A CC Ripple at 125 kHz, 10 A System Demonstration with 10 AH LiFePO$_4$

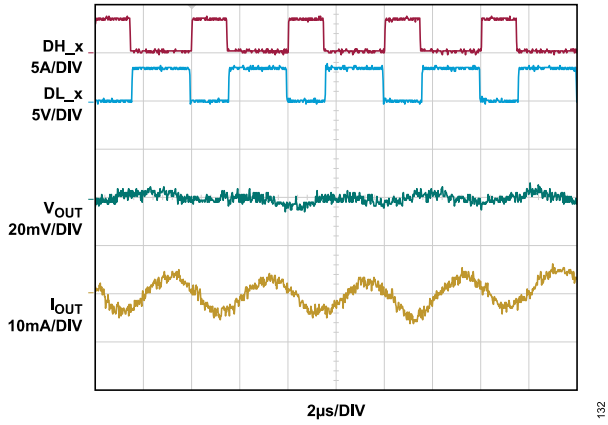


Figure 32. Typical 10 A CC Ripple at 250 kHz, 10 A System Demonstration with 10 AH LiFePO$_4$

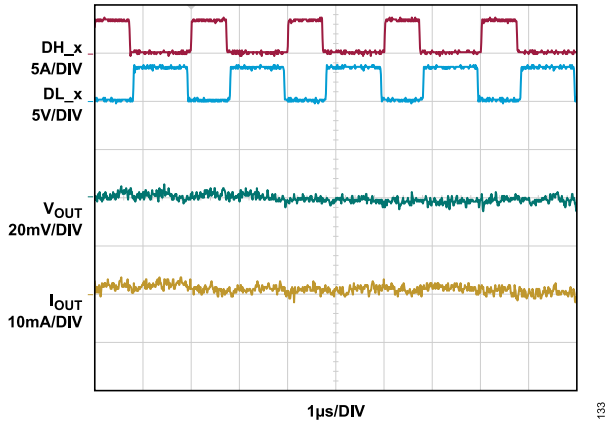


Figure 33. Typical 10 A CC Ripple at 500 kHz, 10 A System Demonstration with 10 AH LiFePO$_4$

THEORY OF OPERATION

OVERVIEW

The ADBT1001 is a highly integrated digital controller that provides four channels of charge and discharge control with a focus on battery formation and test applications. Each channel is composed of a precision analog front end (AFE), measuring both battery current and voltage using a high accuracy ADC, a user programmable digital compensator, and a precision PWM. Additionally, there are 8 auxiliary ADC channels and 16 GPIOx pins.

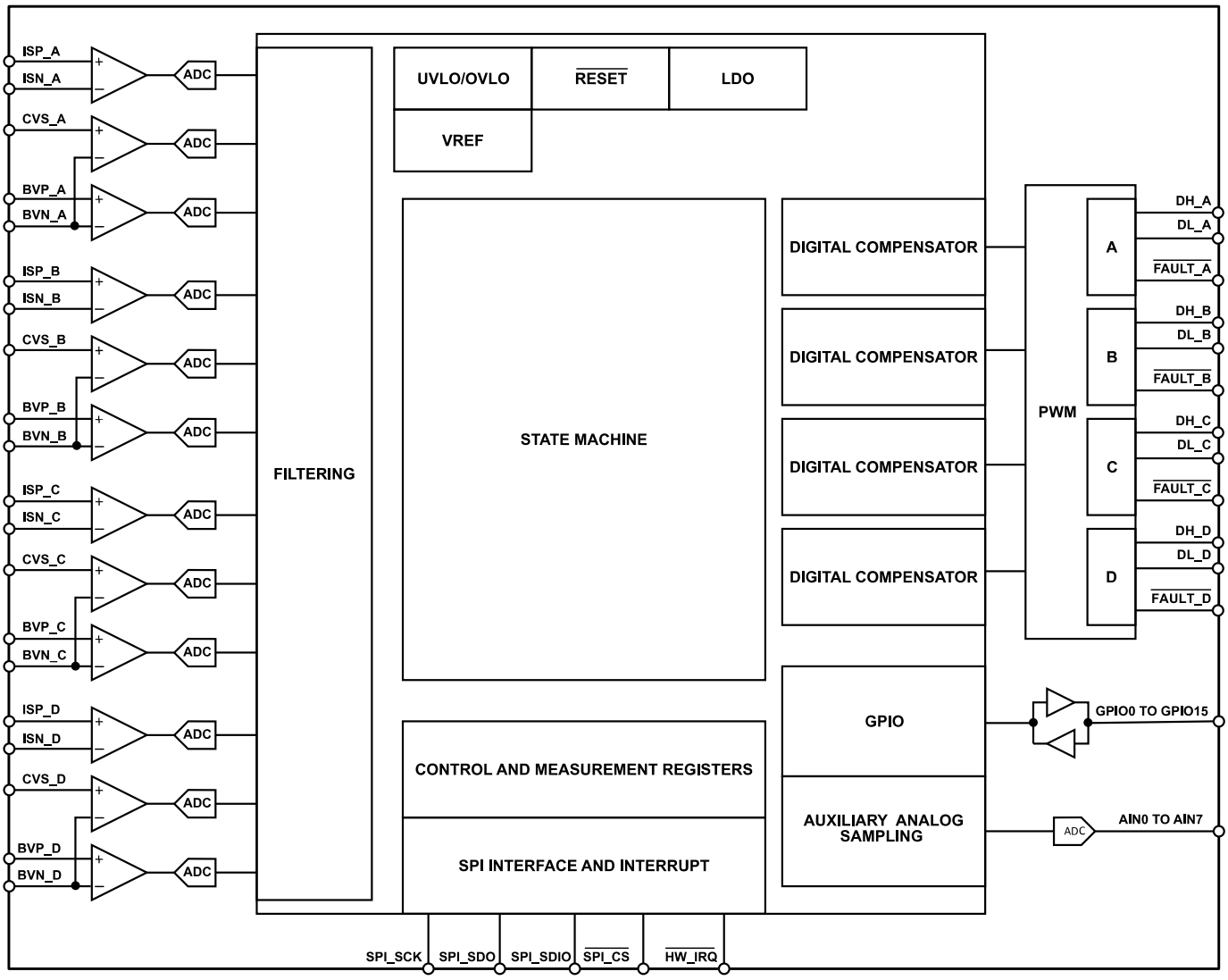


Figure 34. Functional Block Diagram

THEORY OF OPERATION

ANALOG FRONT END

Each channel has a precision current sense differential amplifier with a fixed gain of 40 and a precision voltage sense differential amplifier with a fixed gain of 0.5. A pair of simultaneous sampling ADCs converts the conditioned current and voltage signals to 12-bit digital representations before transferring the signals to the digital controller.

DIGITAL CONTROLLER

A finite state machine (FSM)-based proportional integral derivative (PID) controller provides digital loop control. The controller has user-programmable filter coefficients for control loop compensation. Current and voltage setpoints are register based and are configured by the user over a host SPI. Power and resistance setpoints are also available. Separate current and voltage control loops support CC and CV, as well as constant power (CP) and constant resistance (CR) operating modes. The controller output is used to command the duty cycle of an 16-bit digital PWM. Operation of the controller is discussed in the Sequencer Operation Example section.

HOST SPI

Control is provided by an external host through a 3-wire or a 4-wire SPI. Use the $\overline{\text{SPI\_CS}}$, SPI_SCK, and SPI_SDIO pins for the 3-wire SPI and use the $\overline{\text{SPI\_CS}}$, SPI_SCK, SPI_SDIO, and SPI_SDO pins for the 4-wire SPI. This interface is used to configure the controller through the memory mapped registers. These registers are introduced in Table 11.

HOST INTERRUPT REQUEST

Use the HW_IRQ signal, $\overline{\text{HW\_IRQ}}$, to provide interrupt requests to the host. Use the SPI port accessible set of registers to select which internal events generate host interrupt requests. Event options include system errors, channel data ready, channel voltage and current over limit detection, channel operation complete, and auxiliary ADC high and low threshold detection.

CLOCKING

The ADBT1001 derives all internal clocking from either an internal oscillator, an external 16 MHz crystal, or an external 16 MHz oscillator. Phase interleaving can be configured to help minimize input ripple as well as output ripple when channels are paralleled for greater current capacity. Additionally, multiple devices can be synchronized together, which enables parallel channel operation in multiples of four. The master device provides a 16 MHz clock on the EXTCLKIO pin, and this clock signal is an input at the EXTCLKIO pin on the slave device.

GPIOX PINS

There are 16 GPIOx pins on the ADBT1001. Typical GPIOx pin usage includes controlling the dc bus and battery isolation switches or getting the digital inputs from the digital sources. The GPIOx pins are user-programmable through the following set of memory mapped registers. The GPIOx pins used for the battery isolation switches can be assigned in the global registers for sequencer control. This assigning facilitates the precharge operation at start-up that prevents reverse current when connecting to the battery. Additionally, the GPIOx pins can be configured to provide interdevice digital current sharing communications when using multiple ADBT1001 devices in parallel.

The GPIO_PAD_CFG register is used to configure the GPIOx pin parameters including slew rate, hysteresis, and drive strength. The default bitfields, GPIO_SLEW, GPIO_HYST, and GPIO_DRV, have default settings of 5 ns, 600 mV, and 10 Ω, respectively. These default values are typically acceptable for most applications.

The GPIOx pins can be individually configured as inputs or outputs by using the 16-bit GPIO_IEN_CFG and GPIO_OEN_CFG registers, respectively. Bits[15:0] in each register corresponds to GPIO0 through GPIO15.

When configured as standard GPIOx pins, there are five 16-bit registers that can interact with these pins. In each case, Bit 0 corresponds to GPIO0, and Bit 15 corresponds to GPIO15. The GPIO_READ register can be read to see the state of each GPIOx pin, and the GPIO_WRITE register can be written to set the output pins as 1 or 0. The GPIO_SET, GPIO_CLEAR, and GPIO_TOGGLE registers set, clear, or toggle, respectively, the GPIOx pins that are set as standard GPIOx pin outputs.

In addition to basic user-controlled GPIO operations, the GPIOx pins can be configured for specific operation modes. This configuration is done through the GPIO_MODE_CFG0 (for GPIO0 through GPIO7 pins) and the GPIO_MODE_CFG1 (for GPIO8 through GPIO15 pins) registers. All GPIOx pins can be configured as either standard GPIO input and output functions or can be controlled by the sequencer. The latter is used to control a battery isolation switch that is used as part of the precharge operation. Additional options for GPIO0 through GPIO7 are unique functions used for interdevice communications when multiple devices are used in parallel.

When a GPIOx pin is controlled by the sequencer in a particular channel, there is also a channel GPIO_CFG register where the 4 LSBs are used to select which GPIOx pin is controlled by the sequencer of the channel.

AUXILIARY ADC

An 8-channel, 12-bit ADC is available for dedicated (for example, internal temperature) or general-purpose external measurements. Note that four of the channels have optional current sources for use with the external thermistors for temperature measurement. The dc bus voltage can also be sensed on an ADC channel and used in a feedforward control mechanism to reduce the effect of dc bus transients. All auxiliary ADC operations are user configurable.

THEORY OF OPERATION

SUPPORTS COULOMBIC EFFICIENCY MEASUREMENT

Coulombic efficiency is a ratio of the capacity during discharge to the capacity during charge. The device supports this efficiency through the integration of current over time. The integration results are accessible through a set of registers.

SUPPORTS PRECHARGE OPERATION

When connecting to a cell before a new formation or test cycle, there is a possibility of having a large inrush current from the battery to the discharged output stage. The device allows a user to precharge the output stage before connecting to the cell, which is described in additional detail in the Precharge Operation section.

SEQUENCER

INSTRUCTION DEFINITION

The ADBT1001 works by executing instructions on each of the four channels. Each instruction manages the control loop. The ADBT1001 can operate with CC, CV, CP, and CR modes of operation.

SEQUENCING MODES

Three possible sequencing modes exist to execute instructions from a user point of view: manual, semiautomatic, and automatic.

Manual Mode

In manual sequencing mode, the host central processing unit (CPU) is responsible for feeding instructions to the device. The user writes the full instruction into the next instruction area (that is, the registers prefixed with SEQ_NEXT_xxx) of the channel register map. The user writes to the self clearing start bit after, which initiates the execution of this instruction. The instruction provides a limit or a timeout that can generate a flag that goes into the interrupt controller. The user must service the interrupt, write the next instruction, and set the start bit. The device continues to execute the last instruction until the host CPU services the interrupt.

The register map inside the channel provides a fixed layout for the instruction. The repercussion of this layout is that all possible fields are available independently, whether the instruction uses that information or not. The host CPU is responsible for writing to all the required fields for the instruction to execute as expected.

A double buffer mechanism exists to write the instruction. Only when the start bit is written to the channel is a copy of the instruction forwarded to the state machine and executed. This technique allows the next instruction to be written in advance. Access to the registers regarding the instruction executing is available as a debug feature.

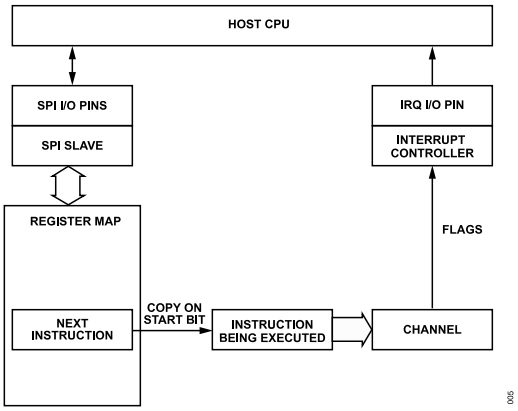


Figure 35. Manual Sequencing Mode

SEQUENCER

Semiautomatic Mode

In semiautomatic mode, the copy of the next instruction executes when the following conditions are met:

- The current instruction hits the limits (voltage, current, or time), which are the same reasons why an interrupt can be raised in manual mode.
- A new instruction has been completely written in the register map.

To avoid executing the same instruction sequentially, there is a bitfield that indicates when the next instruction is fully programmed as follows:

- A flag is set by the user through the self clearing NEXT_INSTR_READY bit in the register map.
- A flag is cleared whenever the instruction is copied from the register map.

The start bit copies the instruction regardless of what the status of the previous instruction is. Such an operation clears the internal register. A readback for the internal flag is then provided through the register map for debug purposes.

Automatic Mode

In automatic sequencing mode, all instructions must be programmed into the instruction memory before setting the start bit. The start bit resets the instruction pointer to the start of the channel memory. Each instruction provides a limit or a timeout that terminates the current instruction and advances the instruction pointer to the next instruction. The channel issues a flag to the interrupt controller when all instructions complete execution. The device inhibits any activity on the DH and DL signals once the instruction sequence terminates.

The instructions stored in the channel memory have variable length payloads using 16-bit words. A fixed header is a one word length. The payload depends on the instruction declared in the header. The instruction pointer advances according to the expected payload. A GUI is available to help users code instruction memory.

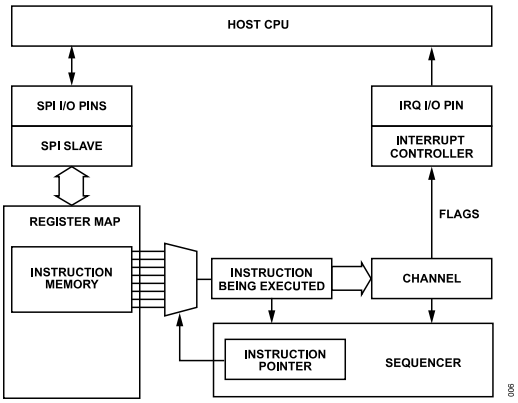


Figure 36. Automatic Sequencing Mode

SEQUENCER

CHARGE AND DISCHARGE INSTRUCTION MODES

The device provides two PID control loops per channel, the current loop and the voltage loop. Only one PID control loop is in control at any given time. The PID control loop in control is the one with the smallest error between the filtered ADC sample and the target setpoint. Note that, VMEAS is the measurement on the V channel.

There are four independent bits to configure how the control loop behaves:

- CC, where the I channel is in control, and the loop target is set to the current setpoint (ISET).
- CV, where the V channel is in control, and the loop target is set to the voltage setpoint (VSET).
- CP, where the I channel is in control, and the loop target is set to the power setpoint (PSET/VMEAS).
- CR, where the I channel is in control, and the loop target is set to the resistance setpoint (VMEAS × GSET).

There are 16 possible mode combinations or 32 including whether the loop is charging or discharging the battery.

The VSET bits (15 LSBs in Register SEQ_NEXT_VSET) can refer to either the absolute value or a delta value based on VMEAS, as determined by the VSET_DELTA bit (MSB in Register SEQ_NEXT_VSET). The main purpose of the delta is to allow the programming of a VSET value at some offset from the last VMEAS value. The start-up (that is, precharge) procedure uses the VSET_DELTA bit with zero offset to get to the current battery voltage value. The precharge operation is discussed in the Precharge Operation section.

CHARGE AND DISCHARGE INSTRUCTION LIMITS

There are three 16-bit programmable fields that represent instruction limits. VLIMIT is associated with the CC mode of operation and can be used to signal the end point of a CC charge or discharge. ILIMIT is associated with the CV mode of operation and is typically used to signal the end point for a CV charge or discharge operation. TLIMIT can be used to either set the duration of an instruction or to set an error overlimit when an instruction should have completed earlier.

VLIMIT

The following details the operation of the VLIMIT bits (Register SEQ_VLIMIT):

- The VLIMIT threshold flags the instruction end on a charge or discharge instruction with CC mode.
- In an instruction with both the CV and CC modes, VLIMIT avoids early instruction termination by not letting any crossing through ILIMIT (Bits[14:0], Register SEQ_ILIMIT) to end the instruction before VLIMIT is crossed. In addition, the V channel PID is not allowed to take control until this threshold is reached.
- If the VLIMIT_DELTA (MSB) bit is cleared, the VLIMIT bits, Bits[14:0], represent an absolute positive voltage.
- If the VLIMIT_DELTA bit is set, the limit is understood as an increment (charge) or a decrement (discharge) from the first VMEAS value read during the execution of an instruction. The main purpose of this bit is to set this limit dynamically without having to read the ADC value before programming this instruction. This bit is related to the VSET_DELTA bit (Register SEQ_VSET).
- The VLIMIT is reached when the measured voltage is higher or equal to the VLIMIT threshold with a charge instruction.
- The VLIMIT is reached when the measured voltage is lower or equal to the VLIMIT threshold with a discharge instruction.

ILIMIT

The following details the operation of the ILIMIT bits (Register SEQ_ILIMIT):

- The ILIMIT threshold flags the instruction end on a charge or discharge instruction with the CV mode active.
- The ILIMIT bits, Bits[14:0], always represent the absolute current magnitude.
- The ILIMIT is reached when the measured current is lower or equal to the ILIMIT threshold with a charge instruction. A reverse current while charging triggers the limit.
- The ILIMIT is reached when the measured current is higher or equal to the negative value of the ILIMIT threshold with a battery discharge instruction. A reverse current while discharging triggers the limit.

TLIMIT

The following details the usage of the NEXT_TLIMIT_SCALE and NEXT_TLIMIT_VAL bitfields (Register SEQ_NEXT_TLIMIT):

- TLIMIT is the target for a timeout trigger event. The trigger is asserted when the elapsed time is equal or greater than TLIMIT.
  - A timeout trigger event can be used for either an error, if an instruction must terminate through another limit, or for a timed execution of an instruction (no error).
- The SEQ_NEXT_TLIMIT, Bits[15:0], are encoded as the following:
  - NEXT_TLIMIT_SCALE, Bits[15:14] are the time units, 3 = minutes, 2 = minutes, 1 = milliseconds, and 0 = microseconds.
  - NEXT_TLIMIT_VAL, Bits[13:0] are the integer value.
- The time units set the resolution and the maximum time value. On a scale of minutes, the resolution is minutes, and the maximum time is 11.3 days. On a scale of microseconds, the resolution is microseconds, and the maximum time is approximately 16.5 ms.

SEQUENCER

Zero Value Limit Implications

The following limit values have special meaning:

- TLIMIT_VAL = 0 means that the timeout is disabled, and no flag is generated.
- ILIMIT = 0, or any low value, means that a CV operation can take a long time to complete.
- VLIMIT = 0 causes a CC operation to terminate immediately.

SLEW RATE

The device provides a slew rate function of the programmed targets that smooths out the transition between instructions. With this function disabled, a step waveform is seen at the error signal of the control loop. With this function enabled, the step waveform is transformed into a ramp waveform.

If the target value slewing function is enabled, the target value ramps from its measured value into the programmed target value as part of the instruction. The register map provides the slew rate for the ISET and VSET bits. The rate is described within two fields: code and time. The code units are in ADC codes, and the time is within the PID and PWM update rate.

The starting point for the ramp is the first value measured with the following limitations:

- In a charge instruction, ISET cannot be a negative value. If there is a back current, ISET starts from 0, ramping up to the setpoint target.
- In a discharge instruction, ISET cannot be a positive value. If there is a positive current, ISET starts from 0, ramping down to the setpoint target.
- VSET is always positive.

A charge and discharge instruction that uses CC ramps ISET. A charge and discharge instruction for CV ramps VSET.

PARALLEL OPERATION

Multiple channels can work in parallel to increase the working current. When multiple channels work in parallel, a channel is declared as the master and transmits the measurement for the I channel (IMEAS) to the other channels. The master channel works as described in the Two Parallel—Two Independent Channels Use Case section and the Four Channels in Parallel Use Case section. The other channels operate in CC mode and target the raw IMEAS from the master channel. Note that the IMEAS value compensates for gain and offset.

Groups of channels working in parallel can span multiple devices.

Transmitting of the IMEAS between channels on a single device happens inside a PID cycle. Transmitting of the IMEAS between channels of different devices is dependent on the interchip SPI communications rate of 8 MHz. Communications between the master and slave devices take 2 µs per 16-bit IMEAS transfer.

FLAGS

The flag block generates flags that end up in the interrupt controller block. The user then unmasks individual flags (in the INT_EN_CH_x registers), as required, to generate interrupts. Flags are cleared when the channel interrupt status register containing the flag is read.

The INSTR_DONE flag is set when an instruction hits the last limit, or if it was the REST instruction when the timeout is reached. Keep this flag separate from the SEQ_DONE flag for debug purposes. When a new instruction loads, the INSTR_DONE flag resets in automatic mode. The start bit can only reset the INSTR_DONE flag in manual mode.

If in automatic mode, the SEQ_DONE flag is set when the last instruction finishes. When in manual mode, this flag is never set, and the start bit resets the SEQ_DONE flag.

The INSTR_TIMEOUT flag results when the timeout is reached if the flag was not another limit termination or the HALT instruction.

The VMEAS_OVER_LMT and IMEAS_OVER_LMT flags result when the input data (ADC raw data for better latency) reaches user specified VMEAS and IMEAS low and high levels, specifically VMEAS_OVER_LIMITS_LOW_THLD and VMEAS_OVER_LIMITS_HIGH_THLD, as well as IMEAS_OVER_LIMITS_LOW_THLD and IMEAS_OVER_LIMITS_HIGH_THLD, respectively. User can also specify the number of consecutive overlimit samples for detection.

The INSTR_USER_IRQ flag is set when the sequencer reads the next instruction with the NEXT_USER_IRQ bit set in the channel SEQ_NEXT_INST register and finishes the execution of that instruction.

The INSTR_ERR flag is set during various events that are not part of the instruction. An instruction error writes a debug error code in the channel register map so that it can be read by the host. Codes include malformed instruction and division by zero.

The INSTR_MODE_TRANS flag is set upon detection of a mode transition, such as a CC to CV transition.

Table 7. Sequencer Flags

Flag	Description
Instruction Finished, INSTR_DONE	Instruction has ended. If in manual sequencing mode, the device expects a new instruction.
Sequence Finished, SEQ_DONE	Instruction halt was run or instruction pointer points outside of the instruction memory.
Timeout, INSTR_TIMEOUT	If instruction is set to flag timeouts, TLIMIT was met.
Measurement Current ($I_{MEASUREMENT}$) Overlimit, IMEAS_OVER_LMT	IMEAS is outside of the globally programmed thresholds.

SEQUENCER

Table 7. Sequencer Flags

Flag	Description
Measurement Voltage (VMEASUREMENTS) Overlimit, VMEAS_OVER_LMT	VMEAS is outside of the globally programmed thresholds.
User Interrupt, INSTR_USER_IRQ	The instruction with the NEXT_USER_IRQ bit was executed.
Instruction Error, INSTR_ERR	Various motives. This flag is a read instruction error code.
Instruction Mode Transition, INSTR_MODE_TRANS	The instruction transitioned from one mode to another, such as from CC to CV mode in a CC to CV operation.

GLOBAL REGISTER SETTINGS

The following global register settings list sits outside of the channel register map, and these settings affect all four channels:

- PWM and loop update rate, which is common for all changes, and the rates can be configured for 500 kHz, 250 kHz, 125 kHz, and 62.5 kHz.
- Configuration of channels for parallel operation.
- Interrupt controller settings.
- Auxiliary ADC configuration and readout.

CHANNEL STATIC SETTINGS

The channel static settings that follow are registers that reside in each of the channel register maps, but these settings are not controllable per instruction.

- Slew rate settings (the enable bit is in the instruction)
- Measurement overlimit thresholds (hard limits that automatically turn-off the channel)
- PWM automatic asynchronous mode transition thresholds
- Digital signal processor (DSP) datapath settings follow:
  - Readout filter decimation rate
  - Numerically controlled oscillator (NCO)
  - Frequency response analysis (FRA) demodulator

INSTRUCTION SET ARCHITECTURE

The instructions that can be programmed into the channel sequencer follow. The word size in memory is 16 bits wide. Each instruction has one word as the header and zero or more words as the payloads.

To simplify register diagrams, 16-bit words are drawn into two rows describing the lower 8 bits first and the higher 8 bits second.

Manual sequencing mode provides a limited set of instructions.

Bits marked with the X mean that the contents of those bits are do not care. It is recommended to write 0s in these bits.

Bits[1:0] of the header define the instruction, INST_TYPE. Instructions include rest, stop, charge, or discharge.

CC , CV, CP, and CR are bits in the header that represent a mode of operation for the charge or the discharge of the battery.

DISABLE_VI_LIMITS disables the use of VLIMIT or ILIMIT for determining instruction end conditions. This bit also disables flagging any voltage or current measurement overlimits.

PWM_AUTO_ASYNC_ENABLE enables or disables the automatic PWM asynchronous mode transition based on current measurements.

TLIMIT_MODE indicates whether the time limit is a normal end condition, or if this bit is a timeout error that, if reached, raises a flag.

SLEW_EN enables a procedure in the charge or the discharge where either ISET or VSET targets are ramped.

GPIO_VAL sets the value of the channel associated GPIOx. In a standard application, this associated GPIOx controls a switch that connects or disconnects the battery from the voltage regulator. A static register inside the channel register map determines which GPIOx that this GPIO_VAL bit controls.

LOOP_START, when set, represents the first instruction that is part of a loop. The hardware stores the address pointer. When set, the first word in the payload must be the number of iterations of the loop. The instruction sets the loop counter with this value if the internal loop counter is 0.

LOOP_END, when set, represents the last instruction that is part of the loop. The loop counter decrements. If the new loop counter value is not 0, the program jumps to the first instruction of the loop.

The V_SEL bit represents the two following options for feeding data into the V channel:

- Battery voltage measurement = 1'b0 means that the measurement is taken across the BVP_x and BVN_x pins.
- Capacitor voltage measurement = 1'b1 means that the measurement is taken across the CVS_x and BVN_x pins.

PID_COEF_SET represents the different options for the PID coefficients. It is desirable to reserve one set for the start-up procedure when the battery is not connected, and another set for the charge or discharge instructions.

USER_IRQ makes the instruction raise a user-defined interrupt at instruction completion.

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Table 8. Instruction Header

Header	7	6	5	4	3	2	1	0
Header LSB Bits	PWM_AUTO_ ASYNC_ ENABLE	DISABLE_VI_ LIMITS	CR	CP	CC	CV	INST_TYPE[1:0]	
Header MSB Bits	TLIMIT_MODE	USER_IRQ	PID_COEF_SET	V_SEL	LOOP_END	LOOP_START	GPIO_VAL	SLEW_EN

SEQUENCER

Halt

Halt is coded with INST_TYPE = 2'b00.

This instruction halts the program thus raising the channel SEQ_DONE flag in automatic mode. The program pointer is not advanced. The PWM (DH_x/DL_x) outputs are overridden with a logic low level.

There is no payload associated with the halt instruction.

Rest

Rest is coded with INST_TYPE = 2'b01.

During a rest instruction, the PID output is held for the duration of TLIMIT to have it ready for the following instruction. The PWM outputs are overridden with a logic low level. GPIO_VAL can be used to disconnect the battery. The channels can also be used as a data acquisition system for taking voltage and current measurements during this instruction.

The rest instruction payload is shown in Table 9. Note that TLIMIT is a required parameter. A LOOP_CNT value is needed if LOOP_START is set. In automatic mode only, LOOP_CNT (8-bit count) must be included if the LOOP_START bit is set in the instruction. A later instruction with the LOOP_END bit set determines the end of the list of instructions that get repeated in the loop.

Table 9. Rest Instruction Payload

Payload	7	6	5	4	3	2	1	0
Payload 0 LSB Bits	TLIMIT, Bits[7:0]							
Payload 0 MSB Bits	TLIMIT, Bits[15:8]							
Payload 1 LSB Bits	LOOP_CNT, Bits[7:0] (Only if LOOP_START is set)							
Payload 1 MSB Bits	X (Don't Care)							

SEQUENCER

Charge and Discharge Operation

These instructions are the main purpose of the ADBT1001 and controls the charge or discharge of the battery.

The payload depends on which bitfields are enabled in the header.

The DH_x and DL_x outputs are active and based on the control loop.

The VLIMIT_DELTA and VSET_DELTA bits tell whether VLIMIT or VSET are based on the last V channel measurement.

Table 10. Charge and Discharge Instruction Payload

Header or Payload	7	6	5	4	3	2	1	0
Header LSBs[1]								
Header MSBs[1]								
Payload 0 LSB Bits	ISET, Bits[7:0] (Only if CC is set)							
Payload 0 MSB Bits	X (Don't Care)	ISET, Bits[14:8] (Only if CC is set)						
Payload 1 LSB Bits	VSET, Bits[7:0] (Only if CV is set)							
Payload 1 MSB Bits	VSET_ DELTA	VSET[14:8] (Only if CV is set)						
Payload 2 LSB Bits	PSET[7:0] (Only if CP is set)							
Payload 2 MSB Bits	PSET[15:8] (Only if CP is set)							
Payload 3 LSB Bits	GSET[7:0] (Only if CR is set)							
Payload 3 MSB Bits	GSET[15:8] (Only if CR is set)							
Payload 4 LSB Bits	ILIMIT, Bits[7:0] (Only if CV is set)							
Payload 4 MSB Bits	X (Don't Care)	ILIMIT, Bits[14:8] (Only if CV is set)						
Payload 5 LSB Bits	VLIMIT, Bits[7:0] (Only if CC is set)							
Payload 5 MSB Bits	VLIMIT_ DELTA	VLIMIT, Bits[14:8] (Only if CC is set)						
Payload 6 LSB Bits	TLIMIT, Bits[7:0]							
Payload 6 MSB Bits	TLIMIT, Bits[15:8]							
Payload 7 LSB Bits	LOOP_CNT[2], Bits[7:0] (Only if LOOP_START is set)							
Payload 7 MSB Bits	X (Don't Care)							

[1] See the Instruction Set Architecture section and Table 8 for additional information on this row.

[2] In automatic mode only, LOOP_CNT (8-bit count) must be included if the LOOP_START bit is set in the instruction. A later instruction with the LOOP_END bit set determines the end of the list of instructions that get repeated in the loop.

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SEQUENCER OPERATION EXAMPLE

To highlight how limits and setpoints interact, a CC to CV charge example description follows.

CC to CV Charge Operation

Figure 37 demonstrates the ISET, VSET, ILIMIT, and VLIMIT usage in a CC to CV charge operation. ISET and VSET are the target CC and CV values, respectively. ILIMIT is the battery current level that signifies the end of the CV portion of the charge cycle. VLIMIT is the minimum battery voltage level before the CV loop can compete for control with the CC loop.

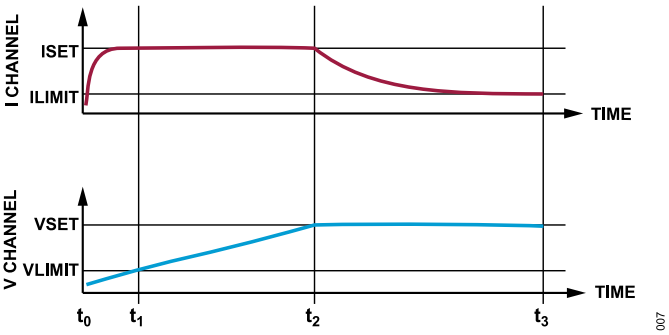

Figure 37. CC to CV Operation

The charge operation starts at t_0. The charge current is 0, and the battery voltage is an open-circuit voltage at the start. From t_0 to t_1, only the CC loop is in control. t_1 is where the battery voltage exceeds VLIMIT. Without VLIMIT, the charge can stop prematurely because the initial battery current at start is 0, which is less than ILIMIT. From t_1 to t_2, both the CC and the CV loops are competing for control. The loop with the lowest error is in control. At t_2, control transitions from CC to CV loop. Note that the error between the battery voltage and VSET is 0. From t_2 to t_3, the CV loop is in control, and the charge current decreases. At t_3, the charge current reaches ILIMIT. In manual sequencer mode, an INSTR_DONE flag generates that can in turn generate an interrupt request. The host must service the interrupt request and either stop the instruction or start a new one. Otherwise, in manual mode, the current instruction keeps executing. In semiautomatic mode, if another instruction is preloaded, it starts executing when the current instruction limit is reached. Otherwise, with no preloaded next instruction, the same operation continues execution as manual mode. In either case, an INSTR_DONE flag is set that can be used to generate a host interrupt. In automatic mode, the next instruction in the sequence executes.

MEMORY MAPPED REGISTERS

Table 11. Register Block Summary

Name	Block	Address
SPI_SLV_CTRL	SPI_SLV_CTRL	0x0000
SYSTEM_CTRL	MISC_CTRL_DIG	0x1000
ADC_CTRL	ADC_COMMON_SETTINGS	0x2800
CHANNEL_CTRLA	CHANNEL_REGMAP	0x3000
CHANNEL_CTRLB	CHANNEL_REGMAP	0x3200
CHANNEL_CTRLC	CHANNEL_REGMAP	0x3400
CHANNEL_CTRLD	CHANNEL_REGMAP	0x3600
CHANNEL_MEM0	SEQ_MEMORY	0x3800
CHANNEL_MEM1	SEQ_MEMORY	0x3A00
CHANNEL_MEM2	SEQ_MEMORY	0x3C00
CHANNEL_MEM3	SEQ_MEMORY	0x3E00

Table 11 shows the various ADBT1001 register blocks and their starting address. The SPI_SLV_CTRL block contains a set of registers used to configure the SPI port and communications protocol.

The SYSTEM_CTRL block contains a set of global registers. These include system configuration, auxiliary ADC configuration, auxiliary ADC data readback, multichannel configuration, and interrupt management.

The ADC_CTRL block contains a few registers used to enable the auxiliary ADC channels and to enable the current excitation for the external temperature measurement.

Each of the four CHANNEL_CTRLx blocks contain the same set of registers, whose addresses are offset by 0x0200 from channel to channel. These individual channel blocks configure channel sequencer operations, diagnostics configuration, and data readback.

The CHANNEL_MEMx blocks do not contain any registers. Instead, these blocks each include 128 16-bit locations to store sequencer configuration parameters when automatic mode operation is selected.

Table 12. SPI_SLV_CTRL (SPI_SLV_CTRL) Register Summary

Address	Name	Description	Reset	Access
0x0	INTERFACE_CONFIG	Interface Configuration	0x06	R/W
0x1	STREAM_MODE	Configure Loop Count	0x00	R/W
0x2	INTERFACE_STATUS	Interface Status	0x00	R/W

Table 13. SYSTEM_CTRL (MISC_CTRL_DIG) Register Summary

Address	Name	Description	Reset	Access
0x1000	RST_CTRL	Software Reset Control Register	0x0000	R/W
0x1001	PMU_CLOCK_SEL	Power Management Unit (PMU) Clock Selection Register	0x0001	R/W
0x1002	PMU_CHANNEL_CFG0	Channel Enable Selection Register	0x0010	R/W
0x1003	PMU_CHANNEL_CFG1	Phase Adjustment for Channel A PWM Signal Register	0x0000	R/W
0x1004	PMU_CHANNEL_CFG2	Phase Adjustment for Channel B PWM Signal Register	0x0200	R/W
0x1005	PMU_CHANNEL_CFG3	Phase Adjustment for Channel C PWM Signal Register	0x0400	R/W
0x1006	PMU_CHANNEL_CFG4	Phase Adjustment for Channel D PWM Signal Register	0x0600	R/W
0x1010	RST_STA	Reset Status Register	0x0000	R/W
0x1012	PMU_CLOCK_STATUS	PMU Clock Status Register	0x0000	R
0x1013	PMU_OTP_STATUS	PMU OTP Status Register	0x0000	R
0x1014	PMU_CHANNEL_STATUS	PWM Locking Status Register	0x0000	R
0x101F	REV_ID_INFO	Revision ID Register	0x00B2	R
0x1020	SPI_SLV_PAD_CFG	SPI Slave Pad Configuration Register	0x0E2A	R/W
0x1021	FAULT_PAD_CFG	Fault Pad Configuration Register	0x0002	R/W
0x1022	GPIO_PAD_CFG	GPIO0 to GPOI1 Pad Configuration Register	0x0035	R/W
0x1023	EXTCLKIO_PAD_CFG	External Input and Output Clock Pad Configuration Register	0x0035	R/W
0x1024	HW_IRQ_PAD_CFG	Hardware Interrupt Pad Configuration Register	0x003D	R/W

MEMORY MAPPED REGISTERS

Table 13. SYSTEM_CTRL (MISC_CTRL_DIG) Register Summary

Address	Name	Description	Reset	Access
0x1025	GPIO_IEN_CFG	GPIO Input Enable Configuration Register	0x0000	R/W
0x1026	GPIO_OEN_CFG	GPIO Output Enable Configuration Register	0x0000	R/W
0x1027	GPIO_MODE_CFG0	GPIO0 to GPIO7 Mode Configuration Register	0x0000	R/W
0x1028	GPIO_MODE_CFG1	GPIO8 to GPIO15 Mode Configuration Register	0x0000	R/W
0x1029	GPIO_READ	GPIO Data Read Register	0x0000	R
0x102A	GPIO_WRITE	GPIO Data Write Register	0x0000	R/W
0x102B	GPIO_SET	GPIO Data Set Register	0x0000	W
0x102C	GPIO_CLEAR	GPIO Data Clear Register	0x0000	W
0x102D	GPIO_TOGGLE	GPIO Data Toggle Register	0x0000	W
0x1040	AIN0_FILT_CFG0	Configuration Register for Filtering Applied to AIN0	0x0000	R/W
0x1041	AIN0_FILT_CFG1	Configuration Register for Filtering Applied to AIN0	0x0000	R/W
0x1042	AIN0_FILT_CFG2	Configuration Register for Filtering Applied to AIN0	0x0010	R/W
0x1043	AIN1_FILT_CFG0	Configuration Register for Filtering Applied to AIN1	0x0000	R/W
0x1044	AIN1_FILT_CFG1	Configuration Register for Filtering Applied to AIN1	0x0000	R/W
0x1045	AIN1_FILT_CFG2	Configuration Register for Filtering Applied to AIN1	0x0010	R/W
0x1046	AIN2_FILT_CFG0	Configuration Register for Filtering Applied to AIN2	0x0000	R/W
0x1047	AIN2_FILT_CFG1	Configuration Register for Filtering Applied to AIN2	0x0000	R/W
0x1048	AIN2_FILT_CFG2	Configuration Register for Filtering Applied to AIN2	0x0010	R/W
0x1049	AIN3_FILT_CFG0	Configuration Register for Filtering Applied to AIN3.	0x0000	R/W
0x104A	AIN3_FILT_CFG1	Configuration Register for Filtering Applied to AIN3	0x0000	R/W
0x104B	AIN3_FILT_CFG2	Configuration Register for Filtering Applied to AIN3	0x0010	R/W
0x104C	AIN4_FILT_CFG0	Configuration Register for Filtering Applied to AIN4	0x0000	R/W
0x104D	AIN4_FILT_CFG1	Configuration Register for Filtering Applied to AIN4	0x0000	R/W
0x104E	AIN4_FILT_CFG2	Configuration Register for Filtering Applied to AIN4	0x0010	R/W
0x104F	AIN5_FILT_CFG0	Configuration Register for Filtering Applied to AIN5	0x0000	R/W
0x1050	AIN5_FILT_CFG1	Configuration Register for Filtering Applied to AIN5	0x0000	R/W
0x1051	AIN5_FILT_CFG2	Configuration Register for Filtering Applied to AIN5	0x0010	R/W
0x1052	AIN6_FILT_CFG0	Configuration Register for Filtering Applied to AIN6	0x0000	R/W

MEMORY MAPPED REGISTERS

Table 13. SYSTEM_CTRL (MISC_CTRL_DIG) Register Summary

Address	Name	Description	Reset	Access
0x1053	AIN6_FILT_CFG1	Configuration Register for Filtering Applied to AIN6	0x0000	R/W
0x1054	AIN6_FILT_CFG2	Configuration Register for Filtering Applied to AIN6	0x0010	R/W
0x1055	AIN7_FILT_CFG0	Configuration Register for Filtering Applied to AIN7	0x0000	R/W
0x1056	AIN7_FILT_CFG1	Configuration Register for Filtering Applied to AIN7	0x0000	R/W
0x1057	AIN7_FILT_CFG2	Configuration Register for Filtering Applied to AIN7	0x0010	R/W
0x1058	TEMP_AFE_FILT_CFG0	Configuration Register for Filtering Applied to Temperature AFE	0x0000	R/W
0x1059	TEMP_AFE_FILT_CFG1	Configuration Register for Filtering Applied to Temperature AFE	0x0000	R/W
0x105A	TEMP_AFE_FILT_CFG2	Configuration Register for Filtering Applied to Temperature AFE	0x0010	R/W
0x105B	TEMP_DSP_FILT_CFG0	Configuration Register for Filtering Applied to Temperature DSP	0x0000	R/W
0x105C	TEMP_DSP_FILT_CFG1	Configuration Register for Filtering Applied to Temperature DSP	0x0000	R/W
0x105D	TEMP_DSP_FILT_CFG2	Configuration Register for Filtering Applied to Temperature DSP	0x0010	R/W
0x105E	DC_BUS_FILT_CFG0	Configuration Register for Filtering Applied to DC Bus	0x0000	R/W
0x105F	DC_BUS_FILT_CFG1	Configuration Register for Filtering Applied to DC Bus	0x0000	R/W
0x1060	DC_BUS_FILT_CFG2	Configuration Register for Filtering Applied to DC Bus	0x0001	R/W
0x1061	DC_BUS_FILT_CFG3	DC Bus Filter Initial Delay in Multiples of 32 µs Register	0x0000	R/W
0x1062	TEMP_INT_CAL_CFG	Configuration for Temperature Gain and Offset Internal Calibration Register	0x0000	R/W
0x1063	TEMP_CAL_0	Temperature Value for Calibration Point 0 Register	0x0000	R/W
0x1064	TEMP_CAL_1	Temperature Value for Calibration Point 1 Register	0x0000	R/W
0x1065	TEMP_CAL_2	Temperature Value for Calibration Point 2 Register	0x0000	R/W
0x1066	TEMP_CAL_3	Temperature Value for Calibration Point 3 Register	0x0000	R/W
0x106B	TEMP_CAL_INV_MSB_0	Slope Between Temperature 0 and Temperature 1 MSBs Register	0x0000	R/W
0x106C	TEMP_CAL_INV_LSB_0	Slope Between Temperature 0 and Temperature 1 LSBs Register	0x0000	R/W

MEMORY MAPPED REGISTERS

Table 13. SYSTEM_CTRL (MISC_CTRL_DIG) Register Summary

Address	Name	Description	Reset	Access
0x106D	TEMP_CAL_INV_MSB_1	Slope Between Temperature 1 and Temperature 2 MSBs Register	0x0000	R/W
0x106E	TEMP_CAL_INV_LSB_1	Slope Between Temperature 1 and Temperature 2 LSBs Register	0x0000	R/W
0x106F	TEMP_CAL_INV_MSB_2	Slope Between Temperature 2 and Temperature 3 MSBs Register	0x0000	R/W
0x1070	TEMP_CAL_INV_LSB_2	Slope Between Temperature 2 and Temperature 3 LSBs Register	0x0000	R/W
0x1071	TEMP_EXT_CAL_CFG0	Configuration for Temperature I Gain External Calibration Register	0x0000	R/W
0x1072	TEMP_EXT_CAL_CFG1	Configuration for Temperature I Gain External Calibration Register	0x0000	R/W
0x1080	AIN0_READOUT	Result of the Measure on the External Pin AIN0 Register	0x0000	R
0x1081	AIN1_READOUT	Result of the Measure on the External Pin AIN1 Register	0x0000	R
0x1082	AIN2_READOUT	Result of the Measure on the External Pin AIN2 Register	0x0000	R
0x1083	AIN3_READOUT	Result of the Measure on External Pin AIN3	0x0000	R
0x1084	AIN4_READOUT	Result of the Measure on the External Pin AIN4 Register	0x0000	R
0x1085	AIN5_READOUT	Result of the Measure on the External Pin AIN5 Register	0x0000	R
0x1086	AIN6_READOUT	Result of the Measure on the External Pin AIN6 Register	0x0000	R
0x1087	AIN7_READOUT	Result of the Measure on the External Pin AIN7 Register	0x0000	R
0x1088	TEMP_AFE_READOUT	Result of the Temperature Measure of the AFE Domain Register	0x0000	R
0x1089	TEMP_DSP_READOUT	Result of the Temperature Measure of the DSP Domain Register	0x0000	R
0x1090	DC_BUS_READOUT	Result of the DC Bus Filter Used for Correction in All PIDs Register	0x0000	R
0x1091	DC_BUS_CORR_FACTOR_READOUT	DC Bus Correction Factor for All Channels Register	0x8000	R
0x10A0	MC_CTRL	Multichannel Global Control Register	0x0000	R/W
0x10A1	MC_CFG0	Multichannel Mode, Slave Channels Configuration Register	0x0000	R/W
0x10A2	MC_CFG1	Multichannel Mode, External Communications Configuration Register	0x0020	R/W

MEMORY MAPPED REGISTERS

Table 13. SYSTEM_CTRL (MISC_CTRL_DIG) Register Summary

Address	Name	Description	Reset	Access
0x10A3	MC_PAD_CFG0	Multichannel Mode, Pad Configuration Register for Slave SPI	0x002A	R/W
0x10A4	MC_PAD_CFG1	Multichannel Mode, Pad Configuration Register for Master SPI	0x0DDD	R/W
0x10C0	SYSTEM_INT_EN	System Interrupt Enable Register	0x0000	R/W
0x10C1	INT_EN_CH_A	Channel A Interrupt Enable Register	0x0000	R/W
0x10C2	INT_EN_CH_B	Channel B Interrupt Enable Register	0x0000	R/W
0x10C3	INT_EN_CH_C	Channel C Interrupt Enable Register	0x0000	R/W
0x10C4	INT_EN_CH_D	Channel D Interrupt Enable Register	0x0000	R/W
0x10C5	INT_EN_AUX_ADC0	Auxiliary Measurements Interrupt Enable Register	0x0000	R/W
0x10C6	INT_EN_AUX_ADC1	Auxiliary Measurements Interrupt Enable Register	0x0000	R/W
0x10D0	SYSTEM_INT_ST	System Interrupt Status Register	0x0000	R/W
0x10D1	INT_ST_CH_A	Channel A Interrupt Status Register	0x0000	R/W
0x10D2	INT_ST_CH_B	Channel B Interrupt Status Register	0x0000	R/W
0x10D3	INT_ST_CH_C	Channel C Interrupt Status Register	0x0000	R/W
0x10D4	INT_ST_CH_D	Channel D Interrupt Status Register	0x0000	R/W
0x10D5	INT_ST_AUX_ADC0	Auxiliary Measurements Interrupt Status Register	0x0000	R/W
0x10D6	INT_ST_AUX_ADC1	Auxiliary Measurements Interrupt Status Register	0x0000	R/W

Table 14. ADC_CTRL (ADC_COMMON_SETTINGS) Register Summary

Address	Name	Description	Reset	Access
0x2800	AUX_ADC_CFG0	Current Values for External Thermistor Applied in AIN0 to AIN3 Pins Register	0x0000	R/W
0x2801	AUX_ADC_CFG1	Control for Auxiliary Inputs and Temperature Sensor Being Measured Register	0x4000	R/W
0x2803	ADC_COMMON_REG	AFE Chopping and Internal Reference Amplifier Settings Register	0x00DA	R/W

MEMORY MAPPED REGISTERS

Table 15. CHANNEL_CTRLA (CHANNEL_REGMAP) Register Summary

Address	Name	Description	Reset	Access
0x3000	SEQ_CTRL	Channel Sequencer Control Register	0x0000	R/W
0x3001	SEQ_STATUS	Channel Sequencer Status Register	0x0000	R
0x3002	SEQ_MEM_PTR	Channel Sequencer Memory Address Pointer Register	0x0000	R
0x3003	SEQ_INST	Channel Sequencer Instruction Register	0x0000	R/W
0x3004	SEQ_ISET	Channel Sequencer Current Setpoint Register	0x0000	R/W
0x3005	SEQ_VSET	Channel Sequencer Voltage Setpoint Register	0x0000	R/W
0x3006	SEQ_PSET	Channel Sequencer Power Set Point Register	0x0000	R/W
0x3007	SEQ_GSET	Channel Sequencer Conductance Set Point Register	0x0000	R/W
0x3008	SEQ_ILIMIT	Channel Sequencer Current Limit Register	0x0000	R/W
0x3009	SEQ_VLIMIT	Channel Sequencer Voltage Limit Register	0x0000	R/W
0x300A	SEQ_TLIMIT	Channel Sequencer Time Limit Register	0x0000	R/W
0x300B	SEQ_NEXT_INST	Channel Sequencer Next Instruction Register	0x0000	R/W
0x300C	SEQ_NEXT_ISET	Channel Sequencer Next Current Set Point Register	0x0000	R/W
0x300D	SEQ_NEXT_VSET	Channel Sequencer Next Voltage Set Point Register	0x0000	R/W
0x300E	SEQ_NEXT_PSET	Channel Sequencer Next Power Set Point Register	0x0000	R/W
0x300F	SEQ_NEXT_GSET	Channel Sequencer Next Conductance Set Point Register	0x0000	R/W
0x3010	SEQ_NEXT_ILIMIT	Channel Sequencer Current-Limit Register	0x0000	R/W
0x3011	SEQ_NEXT_VLIMIT	Channel Sequencer Voltage Limit Register	0x0000	R/W
0x3012	SEQ_NEXT_TLIMIT	Channel Sequencer Next Time Limit Register	0x0000	R/W
0x3013	SLEW_RATE_CFG	Slew Rate Configuration for the Setpoints Register	0x0000	R/W
0x3014	GPIO_CFG	GPIO Configuration Associated to the Channel Register	0x0000	R/W
0x3015	OPEN_LOOP_CFG	Open-Loop Configuration Register	0x0000	R/W
0x3016	OPEN_LOOP_DC_VAL_MSB	Open-Loop DC Value (MSB) Register	0x0000	R/W
0x3017	OPEN_LOOP_DC_VAL_LSB	Open-Loop DC Value (LSB) Register	0x0000	R/W
0x3018	SLAVE_CFG	Slave Configuration Register	0x0008	R/W
0x3040	I_PID_KP_SET1_LSB	Current PID Proportional Coefficient (LSB) Register, Set to 1	0x0000	R/W

MEMORY MAPPED REGISTERS

Table 15. CHANNEL_CTRLA (CHANNEL_REGMAP) Register Summary

Address	Name	Description	Reset	Access
0x3041	I_PID_KP_SET1_MSB	Current PID Proportional Coefficient (MSB) Register, Set to 1	0x0010	R/W
0x3042	I_PID_KI_SET1_LSB	Current PID Integral Coefficient (LSB) Register, Set to 1	0x0000	R/W
0x3043	I_PID_KI_SET1_MSB	Current PID Integral Coefficient (MSB) Register, Set to 1	0x0000	R/W
0x3044	I_PID_KD_SET1_LSB	Current PID Derivative Coefficient (LSB) Register, Set to 1	0x0000	R/W
0x3045	I_PID_KD_SET1_MSB	Current PID Derivative Coefficient (MSB) Register, Set to 1	0x0000	R/W
0x3046	V_PID_KP_SET1_LSB	Voltage PID Proportional Coefficient (LSB) Register, Set to 1	0x0000	R/W
0x3047	V_PID_KP_SET1_MSB	Voltage PID Proportional Coefficient (MSB) Register, Set to 1	0x0010	R/W
0x3048	V_PID_KI_SET1_LSB	Voltage PID Integral Coefficient (LSB) Register, Set to 1	0x0000	R/W
0x3049	V_PID_KI_SET1_MSB	Voltage PID Integral Coefficient (MSB) Register, Set to 1	0x0000	R/W
0x304A	V_PID_KD_SET1_LSB	Voltage PID Derivative Coefficient (LSB) Register, Set to 1	0x0000	R/W
0x304B	V_PID_KD_SET1_MSB	Voltage PID Derivative Coefficient (MSB) Register, Set to 1	0x0000	R/W
0x304C	I_PID_KP_SET2_LSB	Current PID Proportional Coefficient (LSB) Register, Set to 2	0x0000	R/W
0x304D	I_PID_KP_SET2_MSB	Current PID Proportional Coefficient (MSB) Register, Set to 2	0x0010	R/W
0x304E	I_PID_KI_SET2_LSB	Current PID Integral Coefficient (LSB) Register, Set to 2	0x0000	R/W
0x304F	I_PID_KI_SET2_MSB	Current PID Integral Coefficient (MSB) Register, Set to 2	0x0000	R/W
0x3050	I_PID_KD_SET2_LSB	Current PID Derivative Coefficient (LSB) Register, Set to 2	0x0000	R/W
0x3051	I_PID_KD_SET2_MSB	Current PID Derivative Coefficient (MSB) Register, Set to 2	0x0000	R/W
0x3052	V_PID_KP_SET2_LSB	Voltage PID Proportional Coefficient (LSB) Register, Set to 2	0x0000	R/W
0x3053	V_PID_KP_SET2_MSB	Voltage PID Proportional Coefficient (MSB) Register, Set to 2	0x0010	R/W
0x3054	V_PID_KI_SET2_LSB	Voltage PID Integral Coefficient (LSB) Register, Set to 2	0x0000	R/W

MEMORY MAPPED REGISTERS

Table 15. CHANNEL_CTRLA (CHANNEL_REGMAP) Register Summary

Address	Name	Description	Reset	Access
0x3055	V_PID_KI_SET2_MSB	Voltage PID Integral Coefficient (MSB) Register, Set to 2	0x0000	R/W
0x3056	V_PID_KD_SET2_LSB	Voltage PID Derivative Coefficient (LSB) Register, Set to 2	0x0000	R/W
0x3057	V_PID_KD_SET2_MSB	Voltage PID Derivative Coefficient (MSB) Register, Set to 2	0x0000	R/W
0x3058	PID_CCCV_KTRANS_SET1	PID CC to CV Transition Coefficient, Set to 1	0x0000	R/W
0x3059	PID_CCCV_KTRANS_SET2	PID CC to CV Transition Coefficient, Set to 2	0x0000	R/W
0x305A	TEMP_EXT_CAL_0	Temperature Value for the External Calibration Point 0 Register	0x0000	R/W
0x305B	TEMP_EXT_CAL_1	Temperature Value for the External Calibration Point 1 Register	0x0000	R/W
0x305C	TEMP_EXT_CAL_2	Temperature Value for the External Calibration Point 2 Register	0x0000	R/W
0x305D	TEMP_EXT_CAL_3	Temperature Value for the External Calibration Point 3 Register	0x0000	R/W
0x305E	TEMP_EXT_CAL_4	Temperature Value for the External Calibration Point 4 Register	0x0000	R/W
0x305F	TEMP_EXT_CAL_5	Temperature Value for the External Calibration Point 5 Register	0x0000	R/W
0x3060	TEMP_EXT_CAL_INV_MSB_0	Slope Between the External Temperature 0 and Temperature 1 MSBs Register	0x0000	R/W
0x3061	TEMP_EXT_CAL_INV_LSB_0	Slope Between the External Temperature 0 and Temperature 1 LSBs Register	0x0000	R/W
0x3062	TEMP_EXT_CAL_INV_MSB_1	Slope Between the External Temperature 1 and Temperature 2 MSBs Register	0x0000	R/W
0x3063	TEMP_EXT_CAL_INV_LSB_1	Slope Between the External Temperature 1 and Temperature 2 LSBs Register	0x0000	R/W
0x3064	TEMP_EXT_CAL_INV_MSB_2	Slope Between the External Temperature 2 and Temperature 3 MSBs Register	0x0000	R/W
0x3065	TEMP_EXT_CAL_INV_LSB_2	Slope Between the External Temperature 2 and Temperature 3 LSBs Register	0x0000	R/W
0x3066	TEMP_EXT_CAL_INV_MSB_3	Slope Between the External Temperature 3 and Temperature 4 MSBs Register	0x0000	R/W
0x3067	TEMP_EXT_CAL_INV_LSB_3	Slope Between the External Temperature 3 and Temperature 4 LSBs Register	0x0000	R/W

MEMORY MAPPED REGISTERS

Table 15. CHANNEL_CTRLA (CHANNEL_REGMAP) Register Summary

Address	Name	Description	Reset	Access
0x3068	TEMP_EXT_CAL_INV_MSB_4	Slope Between the External Temperature 4 and Temperature 5 MSBs Register	0x0000	R/W
0x3069	TEMP_EXT_CAL_INV_LSB_4	Slope Between the External Temperature 4 and Temperature 5 LSBs Register	0x0000	R/W
0x306A	I_GAIN_EXT_CAL_T0	Current Gain External Calibration for Temperature 0, Signed 2.14 Register	0x4000	R/W
0x306B	I_GAIN_EXT_CAL_T1	Current Gain External Calibration for Temperature 1, Signed 2.14 Register	0x4000	R/W
0x306C	I_GAIN_EXT_CAL_T2	Current Gain External Calibration for Temperature 2, Signed 2.14 Register	0x4000	R/W
0x306D	I_GAIN_EXT_CAL_T3	Current Gain External Calibration for Temperature 3, Signed 2.14 Register	0x4000	R/W
0x306E	I_GAIN_EXT_CAL_T4	Current Gain External Calibration for Temperature 4, Signed 2.14 Register	0x4000	R/W
0x306F	I_GAIN_EXT_CAL_T5	Current Gain External Calibration for Temperature 5, Signed 2.14 Register	0x4000	R/W
0x3070	V_GAIN_INT_CAL_T0	Voltage Gain Internal Calibration for Temperature 0, Signed 2.14 Register	0x4000	R/W
0x3071	V_GAIN_INT_CAL_T1	Voltage Gain Internal Calibration for Temperature 1, Signed 2.14 Register	0x4000	R/W
0x3072	V_GAIN_INT_CAL_T2	Voltage Gain Internal Calibration for Temperature 2, Signed 2.14 Register	0x4000	R/W
0x3073	V_GAIN_INT_CAL_T3	Voltage Gain Internal Calibration for Temperature 3, Signed 2.14 Register	0x4000	R/W
0x3074	I_GAIN_INT_CAL_T0	Current Gain Internal Calibration for Temperature 0, Signed 2.14 Register	0x4000	R/W
0x3075	I_GAIN_INT_CAL_T1	Current Gain Internal Calibration for Temperature 1, Signed 2.14 Register	0x4000	R/W
0x3076	I_GAIN_INT_CAL_T2	Current Gain Internal Calibration for Temperature 2, Signed 2.14 Register	0x4000	R/W
0x3077	I_GAIN_INT_CAL_T3	Current Gain Internal Calibration for Temperature 3, Signed 2.14 Register	0x4000	R/W
0x3078	V_OFFSET_INT_CAL_T0	Voltage Offset Internal Calibration for Temperature 0, Signed 1.15 Register	0x0000	R/W
0x3079	V_OFFSET_INT_CAL_T1	Voltage Offset Internal Calibration for Temperature 1, Signed 1.15 Register	0x0000	R/W

MEMORY MAPPED REGISTERS

Table 15. CHANNEL_CTRLA (CHANNEL_REGMAP) Register Summary

Address	Name	Description	Reset	Access
0x307A	V_OFFSET_INT_CAL_T2	Voltage Offset Internal Calibration for Temperature 2, Signed 1.15 Register	0x0000	R/W
0x307B	V_OFFSET_INT_CAL_T3	Voltage Offset Internal Calibration for Temperature 3, Signed 1.15 Register	0x0000	R/W
0x307C	I_OFFSET_INT_CAL_T0	Current Offset Internal Calibration for Temperature 0, Signed 1.15 Register	0x0000	R/W
0x307D	I_OFFSET_INT_CAL_T1	Current Offset Internal Calibration for Temperature 1, Signed 1.15 Register	0x0000	R/W
0x307E	I_OFFSET_INT_CAL_T2	Current Offset Internal Calibration for Temperature 2, Signed 1.15 Register	0x0000	R/W
0x307F	I_OFFSET_INT_CAL_T3	Current Offset Internal Calibration for Temperature 3, Signed 1.15 Register	0x0000	R/W
0x3080	DSP_READOUT_FILT_CFG	Configuration for the Readout Filters Register	0x0003	R/W
0x3081	MAF_CFG	Configuration for the Moving Average Filter Register	0x0003	R/W
0x3082	SDM_CFG	Configuration for the SDM Register	0x0002	R/W
0x3083	DC_BUS_CORRECTION_CFG	DC Bus Correction Configuration Register	0x0000	R/W
0x3084	PWM_CFG0	Configuration for the PWM 0 Register	0x050A	R/W
0x3085	PWM_CFG1	Configuration for the PWM 1 Register	0x0000	R/W
0x3086	PWM_CFG2	Configuration for the PWM 2 Register	0x0000	R/W
0x3087	PWM_CFG3	Configuration for the PWM 3 Register	0x0000	R/W
0x3088	NCO_CFG0	Configuration for the NCO 0 Register	0x0002	R/W
0x3089	NCO_CFG1	Configuration for the NCO 1 Register	0x8000	R/W
0x308A	NCO_PHASE_INCR_LSB	NCO Phase Increment LSBs Register	0x0000	R/W
0x308B	NCO_PHASE_INCR_MSB	NCO Phase Increment MSBs Register	0x0000	R/W
0x308C	NCO_PHASE_INIT_LSB	NCO Initial Phase LSBs Register	0x0000	R/W
0x308D	NCO_PHASE_INIT_MSB	NCO Initial Phase MSBs Register	0x0000	R/W
0x308E	DEMOD_CFG	Configuration for the FRA Demodulator Register	0x0000	R/W
0x308F	DEMOD_ACCUM_COUNT_LSB	Demodulator Integration Count LSBs Register	0x0000	R/W
0x3090	DEMOD_ACCUM_COUNT_MSB	Demodulator Integration Count MSBs Register	0x0000	R/W
0x3091	FAULT_CFG	Fault Configuration Register	0x0001	R/W

MEMORY MAPPED REGISTERS

Table 15. CHANNEL_CTRLA (CHANNEL_REGMAP) Register Summary

Address	Name	Description	Reset	Access
0x3092	MEAS_OVER_LIMITS_CFG	Overlimits Detection for the Voltage and Current Measurement ADC Raw Data Configuration Register	0x0000	R/W
0x3093	VMEAS_OVER_LIMITS_HIGH_THLD	High Overlimit Threshold for the Voltage Measurement ADC Raw Data Register	0x0000	R/W
0x3094	VMEAS_OVER_LIMITS_LOW_THLD	Low Overlimit Threshold for the Voltage Measurement ADC Raw Data Register	0x0000	R/W
0x3095	IMEAS_OVER_LIMITS_HIGH_THLD	High Overlimit Threshold for the Current Measurement ADC Raw Data Register	0x0000	R/W
0x3096	IMEAS_OVER_LIMITS_LOW_THLD	Low Overlimit Threshold for the Current Measurement ADC Raw Data Register	0x0000	R/W
0x3100	DSP_READOUT_DATA_0	Readout Data, MSBs of Voltage Data Register (Whenever there is a read on this register, the rest of the readout data registers are sampled.)	0x0000	R
0x3101	DSP_READOUT_DATA_1	Readout Data, MSBs of Current Data Register	0x0000	R
0x3102	DSP_READOUT_DATA_2	Readout Data, LSBs of the Voltage and Current Data and Tag Number Register	0x0000	R
0x3104	COULOMB_COUNT_0	Coulomb Integration Result for the Ongoing Instruction 0 Register (Whenever there is a read on this register, the rest of the COULOMB_COUNT_1 to COULOMB_COUNT_3 registers are sampled.)	0x0000	R
0x3105	COULOMB_COUNT_1	Coulomb Integration Result for the Ongoing Instruction 1 Register	0x0000	R
0x3106	COULOMB_COUNT_2	Coulomb Integration Result for the Ongoing Instruction 2 Register	0x0000	R
0x3107	COULOMB_COUNT_3	Coulomb Integration Result for the Ongoing Instruction 3 Register	0x0000	R
0x3108	COULOMB_COUNT_PREV_0	Coulomb Integration Result for the Previous Instruction 0 Register	0x0000	R
0x3109	COULOMB_COUNT_PREV_1	Coulomb Integration Result for the Previous Instruction 1 Register	0x0000	R
0x310A	COULOMB_COUNT_PREV_2	Coulomb Integration Result for the Previous Instruction.	0x0000	R
0x310B	COULOMB_COUNT_PREV_3	Coulomb Integration Result for the previous Instruction 3 Register	0x0000	R

MEMORY MAPPED REGISTERS

Table 15. CHANNEL_CTRLA (CHANNEL_REGMAP) Register Summary

Address	Name	Description	Reset	Access
0x310C	DEMOD_XV_I_RESULT_0	FRA PID Output + NCO Demodulator Current Result 0 Register	0x0000	R
0x310D	DEMOD_XV_I_RESULT_1	FRA PID Output + NCO Demodulator Current Result 1 Register	0x0000	R
0x310E	DEMOD_XV_I_RESULT_2	FRA PID Output + NCO Demodulator Current Result 2 Register	0x0000	R
0x310F	DEMOD_XV_I_RESULT_3	FRA PID Output + NCO Demodulator Current Result 3 Register	0x0000	R
0x3110	DEMOD_XV_Q_RESULT_0	FRA PID Output + NCO Demodulator Quadrature Result 0 Register	0x0000	R
0x3111	DEMOD_XV_Q_RESULT_1	FRA PID Output + NCO Demodulator Quadrature Result 1 Register	0x0000	R
0x3112	DEMOD_XV_Q_RESULT_2	FRA PID Output + NCO Demodulator Quadrature Result 2 Register	0x0000	R
0x3113	DEMOD_XV_Q_RESULT_3	FRA PID Output + NCO Demodulator Quadrature Result 3 Register	0x0000	R
0x3114	DEMOD_YI_I_RESULT_0	FRA PID Output Demodulator Current Result 0 Register	0x0000	R
0x3115	DEMOD_YI_I_RESULT_1	FRA PID Output Demodulator Current Result 1 Register	0x0000	R
0x3116	DEMOD_YI_I_RESULT_2	FRA PID Output Demodulator Current Result 2 Register	0x0000	R
0x3117	DEMOD_YI_I_RESULT_3	FRA PID Output Demodulator Current Result 3 Register	0x0000	R
0x3118	DEMOD_YI_Q_RESULT_0	FRA PID Output Demodulator Quadrature Result 0 Register	0x0000	R
0x3119	DEMOD_YI_Q_RESULT_1	FRA PID Output Demodulator Quadrature Result 1 Register	0x0000	R
0x311A	DEMOD_YI_Q_RESULT_2	FRA PID Output Demodulator Quadrature Result 2 Register	0x0000	R
0x311B	DEMOD_YI_Q_RESULT_3	FRA PID Output Demodulator Quadrature Result 3 Register	0x0000	R

HOST SPI INTERFACE DETAILS

SPI OVERVIEW

The host communicates with the device through a SPI port. The SPI port supports both 3-wire (with a single bidirectional data signal) and traditional 4-wire interfaces (default). These interfaces are selectable through configuration of the INTERFACE_CONFIG register.

SPI_SCK functions as a serial shift clock and is generated by the host. The default clock polarity (CPOL) and clock phase (CPHA) are both 0. The rising edge of SPI_SCK is used to latch data from the host while the falling edge latches data to the host. The maximum clock rate is 16 MHz.

SPI_SDIO is a data input pin in 4-wire mode and a bidirectional data pin in 3-wire mode.

SPI_SDO is the data output only pin used in 4-wire-mode. Note that MSB first is the default mode, but LSB first can also be configured.

$\overline{\text{SPI\_CS}}$ is an active low SPI chip select signal. A low going assertion starts a read or write operation. Data streaming can also be accommodated with automatic register address increment (default) or decrement.

Additional SPI port features include cyclic redundancy check (CRC) and address looping. The latter allows streaming over a limited range of consecutive register addresses.

COMMUNICATIONS PROTOCOLS

All transfers are done with 16-bit words. The first 16-bit word of each transaction (instruction phase) consists of a 15-bit register address and a R/W bit. The MSB R/W bit is 0 for a write and a 1 for a read.

Basic Read Operation

The instruction phase is performed in the first 16-bit word transfer. The R/W bit, which is the MSB during the instruction phase shown in Figure 38, is set to 1 for a read operation. The other 15 bits specify the register address. The next 16-bit transfer from the host specifies the number of consecutive 16-bit reads to perform. For a single 16-bit register read, this field is set to 0 or 1. Starting on the 33rd SPI_SCLK, data is read out. If the number of reads is 2 or more, $\overline{\text{SPI\_CS}}$ must be asserted beyond the three basic single word 16-bit transfers through the total number requested.

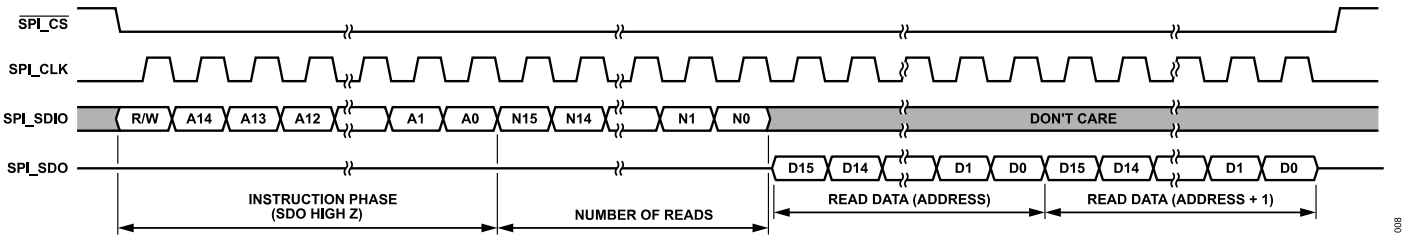

Figure 38. Basic 4-Wire Read Operation

HOST SPI INTERFACE DETAILS

Basic Write Operation

Timing for basic write operation is shown in Figure 39. The R/W bit in the instruction phase is 0 for a write operation. The 16-bit data to be written to immediately follows the 16-bit instruction phase. Additional data can be written by keeping $\overline{\text{SPI\_CS}}$ asserted while clocking in additional 16-bit words. The data is transferred to sequential register addresses.

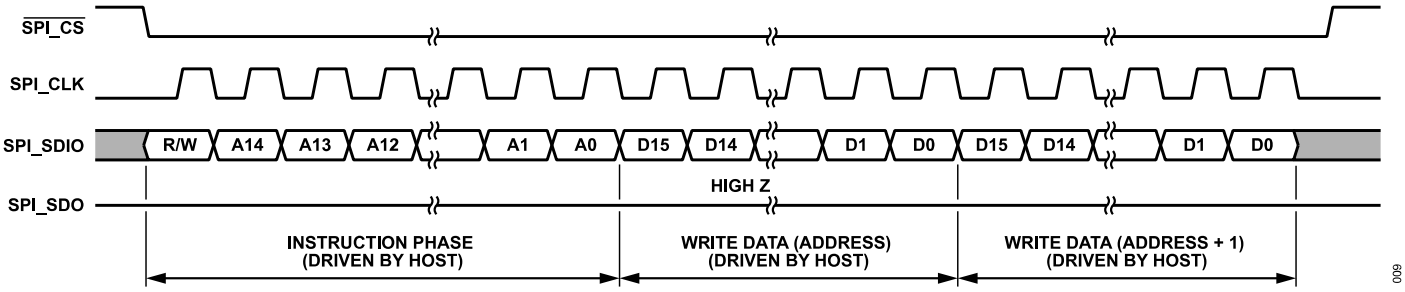

Figure 39. Basic 4-Wire Write Operation

APPLICATIONS INFORMATION

CALIBRATION

Facilitate System Calibration

The device supports a means to facilitate a system calibration, which includes registers for each ADC channel to include offset and gain scaling calibration data. The user can provide external stimulus, measure the results, and calculate the requisite offset and gain scaling values over several temperature points. These values can then be user programmed into the ADC calibration registers. These values can then be used to compensate for system errors over a specific temperature range.

DIAGNOSTICS

Support DC Internal Resistance (DCIR) Measurement

DCIR measurement is supported indirectly via accurate measurement of the battery voltage. The external controller must store data samples, monitor current step changes, determine when the RC time constant is complete, and estimate the voltage difference.

$$DCIR = \Delta V / \Delta I \quad (1)$$

During this measurement, the output data rate can be increased to capture the transient response.

OPERATING USE CASES

4-Channel Independent Use Case

For the 4-channel independent use case, each channel conducts a separate and independent measurement of the battery voltage and current, and has independent control of the same. In addition, each channel has independently programmable voltage and current setpoints.

APPLICATIONS INFORMATION

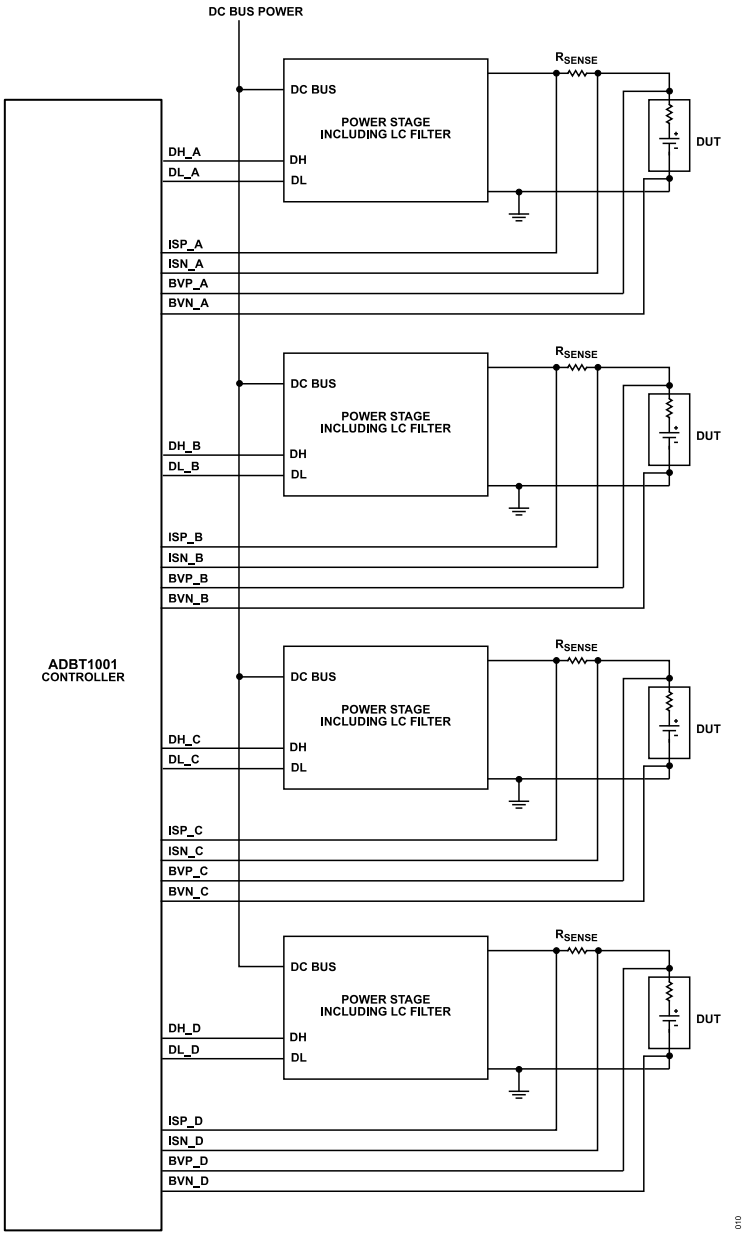

Figure 40. 4-Channel Independent Use Case

APPLICATIONS INFORMATION

Two Parallel—Two Independent Channels Use Case

This use case has two of the four channels operating in parallel for increased current capacity, and the other two channels are configured as independent channels. Each channel conducts separate and independent measurement of the battery voltage and current, and has independent control of the same. Each of the two independent channels have independently programmable voltage and current setpoints. However, with the two parallel channels, the master channel (Channel A) uses both the voltage and current setpoints, while the slave parallel channel uses only the current setpoint. The current setpoint is provided automatically from the master channel current measurement so that it tracks properly. The host must program the master channel current setpoint with half of the total desired current.

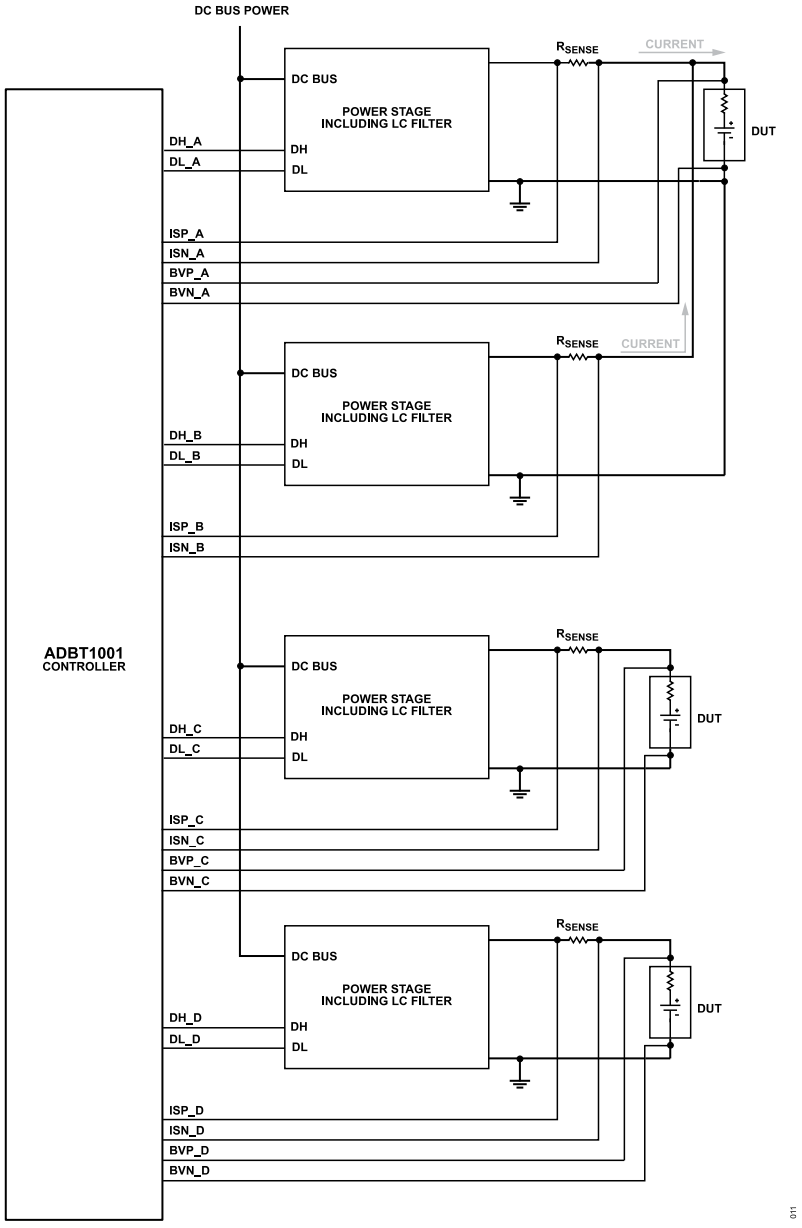

Figure 41. Two Parallel—Two Independent Channels Use Case

APPLICATIONS INFORMATION

Four Channels in Parallel Use Case

This use case has all four channels operating in parallel for increased current capacity. Each channel conducts separate and independent measurement of the battery voltage and current, and has independent control of the same. The master channel (Channel A) uses both the voltage and current setpoints, while the slave parallel channels use only the current setpoint. The current setpoint is provided automatically from the master channel current measurement so that it tracks properly. The host must program the master channel current setpoint with ¼ of the total desired current.

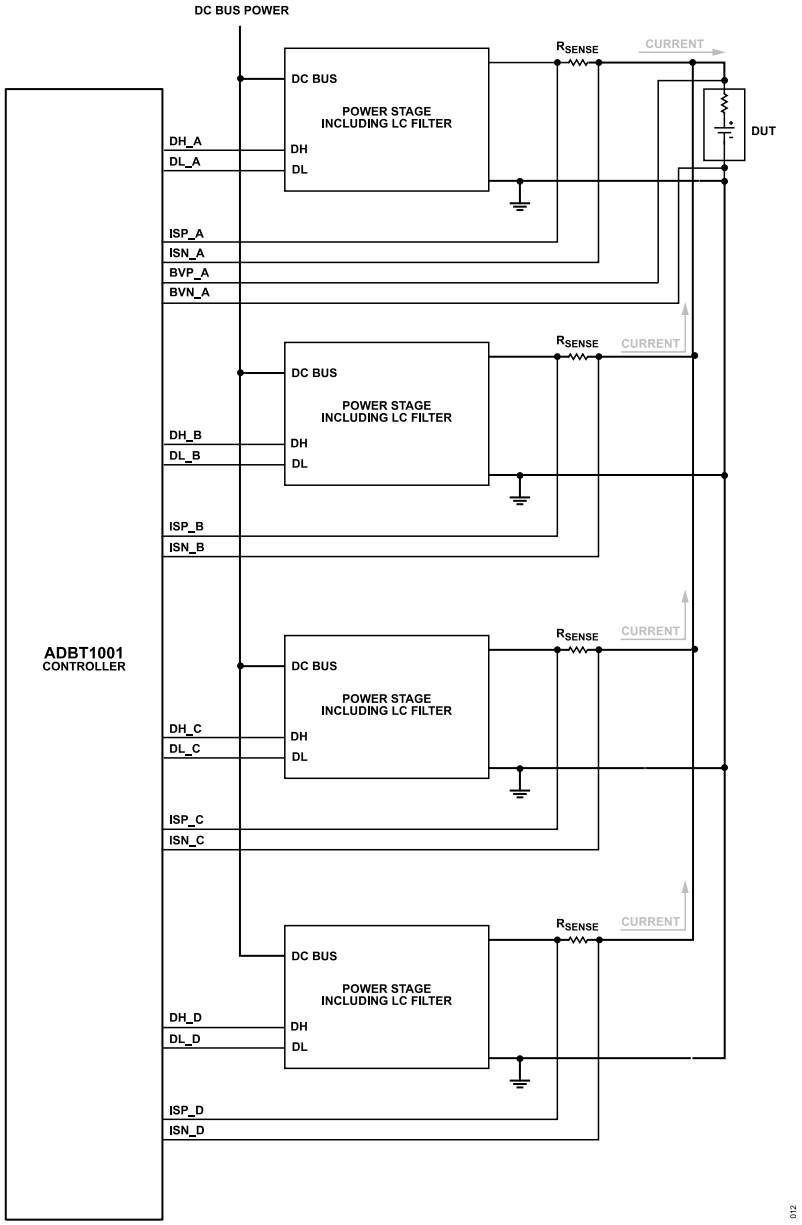

Figure 42. Four Channels in Parallel Use Case

APPLICATIONS INFORMATION

Precharge Operation

When connecting a cell to the power stage, there is a chance of a large current surge as a charge flows from the cell to the uncharged output capacitor (C1 in Figure 43). The device supports measurement of both the battery voltage (BVN_x and BVP_x) and the power stage output capacitor voltage (CVS_x). These measurements allow users to precharge C1 to the potential of the battery before closing the isolation switches (Q3 and Q4). This results in little to no current flowing upon connection of the battery to the power stage.

A GPIOx pin can be configured to provide control of the isolation switches.

Measurement of both the cell and output capacitor voltages is available via the SPI port and a set of memory mapped registers. Use the VSET bit to control of the output capacitor voltage.

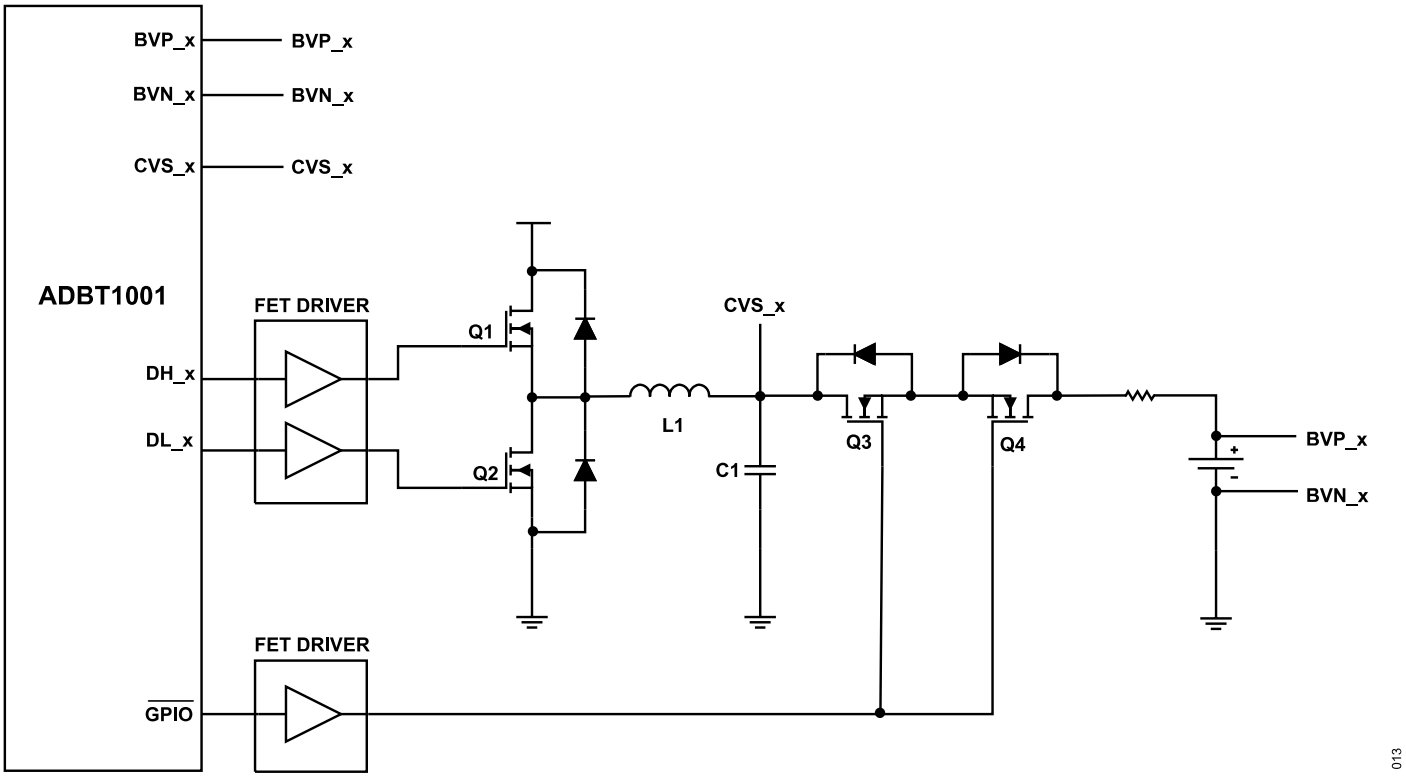

Figure 43. Precharge Function Diagram

OUTLINE DIMENSIONS

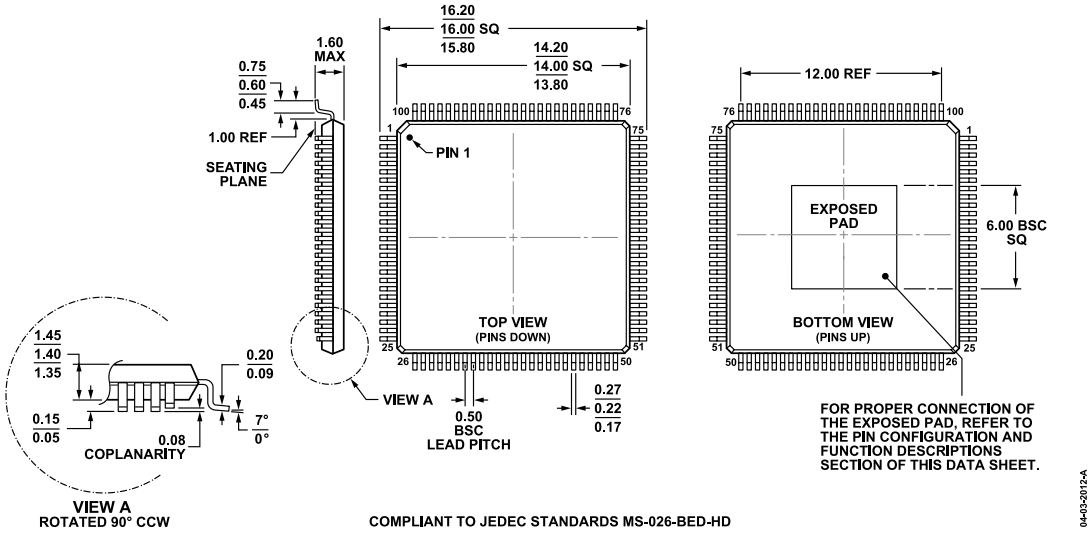

Figure 44. 100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP]
14 mm × 14 mm Body
(SW-100-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADBT1001BSWZ	0°C to 85°C	100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP]	(SW-100-2)
ADBT1001BSWZ-RL	0°C to 85°C	100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP]	(SW-100-2)

[1] Z = RoHS Compliant Part.