ISL94201

Multi-Cell Li-ion Battery Pack Analog Front-End

FN6719
Rev 0.00
July 3, 2008

The ISL94201 is an analog front end for a microcontroller in a multi-cell Li-ion battery pack. The ISL94201 supports battery pack configurations consisting of 4-cells to 7-cells in series and 1 or more cells in parallel. The ISL94201 provides an internal 3.3V voltage regulator, and cell voltage monitor level shifters.

Using an internal analog multiplexer the ISL94201 provides monitoring of each cell voltage plus internal and external temperature by a separate microcontroller with an A/D converter. Software on this microcontroller implements all battery pack control functionality.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL94201IRZ	942 01IRTZ	24 Ld 4x4 QFN	L24.4x4D

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

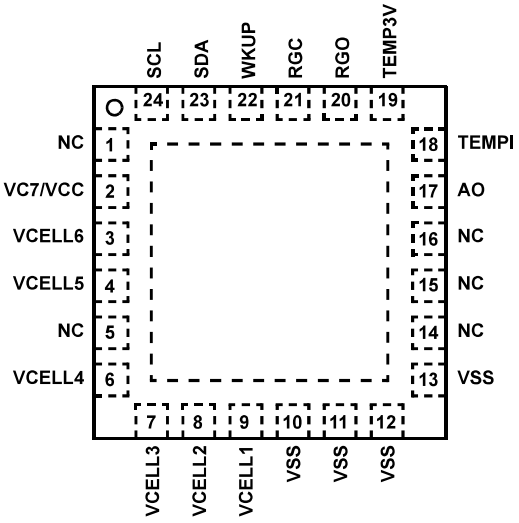
- Four Battery-Backed Software Controlled Flags
- 10% Accurate 3.3V Voltage Regulator (Minimum 25mA Out With External NPN Transistor Having Current Gain of 70)
- Monitored Cell Voltage Output Stable In 100µs
- Simple I^2C Host Interface
- Sleep Operation With Programmable Negative Edge or Positive Edge Wake-Up
- <10µA Sleep Mode
- Pb-Free (RoHS compliant)

Applications

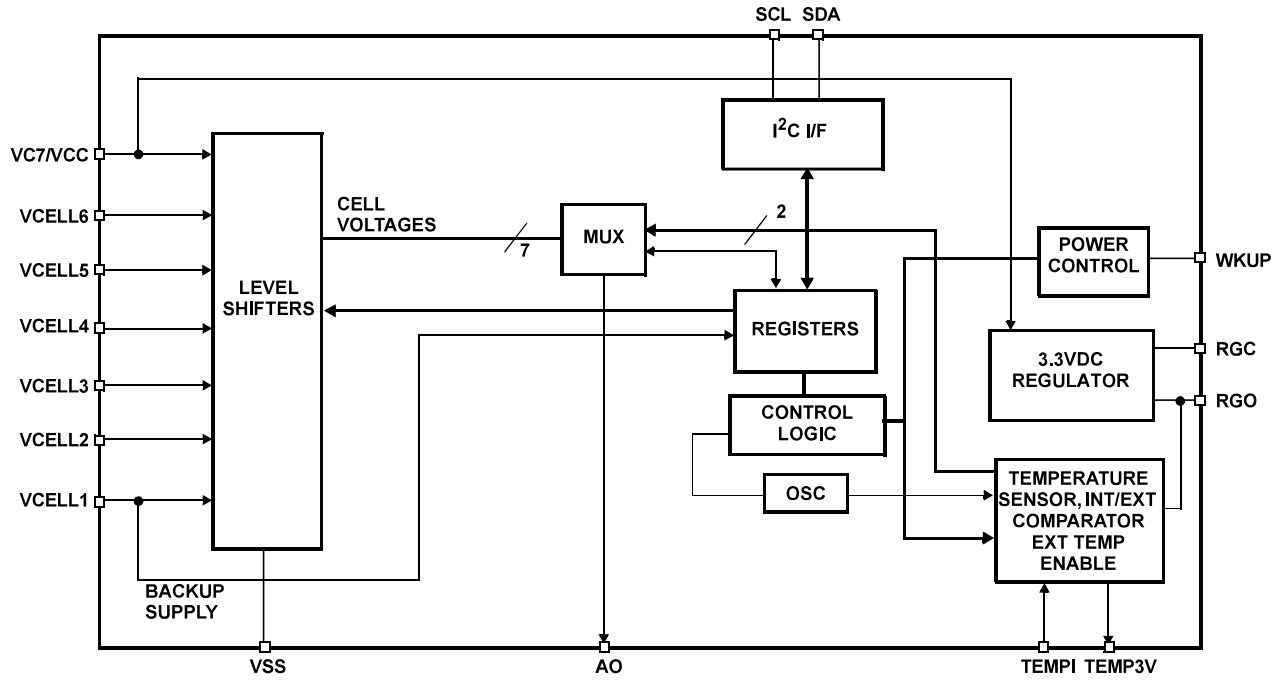
- Power Tools
- Battery Backup Systems
- E-Bikes
- Portable Test Equipment
- Medical Systems
- Hybrid Vehicle
- Military Electronics

Pinout

ISL94201
(24 LD QFN)
TOP VIEW



Functional Diagram



Pin Descriptions

SYMBOL	DESCRIPTION
VC7/VCC	**Battery cell 7 voltage input/VCC supply.** This pin is used to monitor the voltage of this battery cell externally at pin AO. This pin also provides the operating voltage for the IC circuitry.
VCELLN	**Battery cell N voltage input.** This pin is used to monitor the voltage of this battery cell externally at pin AO. VCELLN connects to the positive terminal of CELLN and the negative terminal of CELLN + 1.
VSS	Ground. This pin connects to the most negative terminal in the battery string.
AO	**Analog multiplexer output.** The analog output pin is used by an external microcontroller to monitor the cell voltages and temperature sensor voltages. The microcontroller selects the specific voltage being applied to the output by writing to a control register.
TEMP3V	**Temperature monitor output control.** This pin outputs a voltage to be used in a divider that consists of a fixed resistor and a thermistor. The thermistor is located in close proximity to the cells. The TEMP3V output is connected internally to the RGO voltage through a PMOS switch only during a measurement of the temperature, otherwise the TEMP3V output is off. The TEMP3V output can be turned on continuously with a special control bit. Microcontroller wake up control.
TEMPI	**Temperature monitor input.** This pin inputs the voltage across a thermistor to determine the temperature of the cells. When this input drops below TEMP3V/13, an external over-temperature condition exists. The TEMPI voltage is also fed to the AO output pin through an analog multiplexer so the temperature of the cells can be monitored by the microcontroller.
RGO	**Regulated output voltage.** This pin connects to the emitter of an external NPN transistor and works in conjunction with the RGC pin to provides a regulated 3.3V. The voltage at this pin provides feedback for the regulator and power for many of the ISL94201internal circuits as well as providing the 3.3V output voltage for the microcontroller and other external circuits.
RGC	**Regulated output control.** This pin connects to the base of an external NPN transistor and works in conjunction with the RGO pin to provide a regulated 3.3V. The RGC output provides the control signal for the external transistor to provide the 3.3V regulated voltage on the RGO pin.
WKUP	**Wake up Voltage.** This input wakes up the part when the voltage crosses a turn-on threshold (wake up is edge triggered). The condition of the pin is reflected in the WKUP bit (The WKUP bit is level sensitive.) WKPOL bit = ”1”: the device wakes up on the rising edge of the WKUP pin. Also, the WKUP bit is HIGH only when the WKUP pin voltage > threshold. WKPOL bit = ”0”, the device wakes up on the falling edge of the WKUP pin. Also, the WKUP bit is HIGH only when the WKUP pin voltage < threshold.
SDA	**Serial Data.** This is the bidirectional data line for an I^2C interface.
SCL	**Serial Clock.** This is the clock input for an I^2C communication link.

Absolute Maximum Ratings

Power Supply Voltage, VCC . . . . . V_{SS} - 0.5V to V_{SS} + 36.0V
Cell voltage, VCELL
VCELLN - (VCELLN - 1), VCELL1 - VSS . . . . . -0.5V to 5V
Terminal Voltage, V_{TERM1}
(SCL, SDA, TEMPI, RGO, AO, TEMP3V)
. . . . . V_{SS} - 0.5 to V_{RGO} + 0.5V
Terminal Voltage, V_{TERM3} (WKUP)
. . . . . V_{SS} - 0.5V to V_{CC} (V_{CC} <27V)
Terminal Voltage, V_{TERM4} (RGC) . . . . . V_{SS} - 0.5V to 5V
Terminal Voltage, V_{TERM5}, (all other pins)
. . . . . V_{SS} - 0.5V to V_{CC} + 0.5V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN	32	2

Continuous Package Power Dissipation 400mW
Storage Temperature . . . . . .-55 to +125°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C
Supply Voltage Range (Typical) . . . . . 5V to 10V
Operating Voltage:
VCC pin . . . . . 9.2V to 30.1V
VCELL1 - VSS . . . . . 2.3V to 4.3V
VCELLN - (VCELLN-1) . . . . . 2.3V to 4.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Operating Specifications

Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Operating Voltage	V_{CC}		9.2		30.1	V
Power-Up Condition 1	V_{PORVCC}	V_{CC} voltage (Note 3)		4	9.2	V
Power-Up Condition 2 Threshold	V_{POR123}	V_{CELL1} - V_{SS} and V_{CELL2} - V_{CELL1} and V_{CELL3} - V_{CELL2} (rising) (Note 3)	1.1	1.7	2.3	V
Power-Up Condition 2 Hysteresis	V_{PORhys}	V_{CELL1} - V_{SS} and V_{CELL2} - V_{CELL1} and V_{CELL3} - V_{CELL2} (falling) (Note 3)		70		mV
3.3V Regulated Voltage	V_{RGO}	0µA < I_{RGC} < 350µA	3.0	3.3	3.6	V
3.3VDC Voltage Regulator Control Current Limit	I_{RGC}	(Control current at output of RGC. Recommend NPN with gain of 70+)	0.35	0.50		mA
V_{CC} Supply Current	I_{VCC1}	Power-up defaults, WKUP pin = 0V.		400	510	µA
RGO Supply Current	I_{RGO1}	Power-up defaults, WKUP pin = 0V.		300	410	µA
V_{CC} Supply Current	I_{VCC2}	LDMONEN bit = 1, WKPOL bit = 1, VWKUP = 10V, [AO3:AO0] bits = 03H.		500	700	µA
RGO Supply Current	I_{RGO2}	LDMONEN bit = 1, WKPOL bit = 1, VWKUP = 10V, [AO3:AO0] bits = 03H.		450	650	µA
V_{CC} Supply Current	I_{VCC3}	Default register settings, except SLEEP bit = 1. WKUP pin = VCELL1			10	µA
RGO Supply Current	I_{RGO3}	Default register settings, except SLEEP bit = 1. WKUP pin = VCELL1			1	µA
VCELL Input Current (V_{CELL1})	I_{VCELL1}	AO3:AO0 bits = 0000H			14	µA
VCELL Input Current (V_{CELLN})	I_{VCELLN}	AO3:AO0 bits = 0000H			10	µA

Operating Specifications Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested **(Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
OVER-TEMPERATURE PROTECTION SPECIFICATIONS						
Internal Temperature Shutdown Threshold	T_{INTSD}			125		°C
Internal Temperature Hysteresis	T_{HYS}	Temperature drop needed to restore operation after over-temperature shutdown.		20		°C
Internal Over-temperature Turn On Delay Time	t_{ITD}			128		ms
External Temperature Output Current	I_{XT}	Current output capability at TEMP3V pin	1.2			mA
External Temperature Limit Threshold	T_{XTF}	Voltage at V_{TEMPI}; Relative to falling edge $\frac{V_{TEMP3V}}{13}$	-20	0	+20	mV
External Temperature Limit Hysteresis	T_{XTH}	Voltage at V_{TEMPI}.	60	110	160	mV
External Temperature Monitor Delay	t_{XTD}	Delay between activating the external sensor and the internal over-temperature detection.		1		ms
External Temperature Autoscan On-Time	t_{XTAON}	TEMP3V is ON (3.3V)		5		ms
External Temperature Autoscan Off-Time	t_{XTAOFF}	TEMP3V output is off.		635		ms
ANALOG OUTPUT SPECIFICATIONS						
Cell Monitor Analog Output Voltage Accuracy	V_{AOC}	$[V_{CELLN} - (V_{CELLN-1})]/2$ - AO	-15	4	30	mV
Cell Monitor Analog Output External Temperature Accuracy	V_{AOXT}	External temperature monitoring accuracy. Voltage error at AO when monitoring TEMPI voltage (measured with TEMPI = 1V)	-10		10	mV
Internal Temperature Monitor Output Voltage Slope	V_{INTMON}	Internal temperature monitor voltage change		-3.5		mV/°C
Internal Temperature Monitor Output	T_{INT25}	Output at +25°C		1.31		V
AO Output Stabilization Time	t_{VSC}	From SCL falling edge at data bit 0 of command to AO output stable within 0.5% of final value. AO voltage steps from 0V to 2V. (C_{AO} = 10pF) (Note 7)			0.1	ms
WAKE UP/SLEEP SPECIFICATIONS						
Device WKUP Pin Voltage Threshold (WKUP Pin Active High - Rising Edge)	V_{WKUP1}	WKUP pin rising edge (WKPOL = 1) Device wakes up and sets WKUP flag HIGH.	3.5	5.0	6.5	V
Device Wkup Pin Hysteresis (WKUP Pin Active High)	V_{WKUP1H}	WKUP pin falling edge hysteresis (WKPOL = 1) sets WKUP flag LOW (does not automatically enter sleep mode)		100		mV
Input Resistance On WKUP	R_{WKUP}	Resistance from WKUP pin to VSS (WKPOL = 1)	130	230	330	kΩ
Device WKUP Pin Active Voltage Threshold (WKUP Pin Active Low - Falling Edge)	V_{WKUP2}	WKUP pin falling edge (WKPOL = 0) Device wakes up and sets WKUP flag HIGH.	V_{CELL1} - 2.6	V_{CELL1} - 2.0	V_{CELL1} - 1.2	V

Operating Specifications Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested **(Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Device Wkup Pin Hysteresis (WKUP Pin Active Low)	V_{WKUP2H}	WKUP pin rising edge hysteresis (WKPOL = 0) sets WKUP flag LOW (does not automatically enter sleep mode).		200		mV
Device Wake-up Delay	t_{WKUP}	Delay after voltage on WKUP pin crosses the threshold (rising or falling) before activating the WKUP bit.	20	40	60	ms
SERIAL INTERFACE CHARACTERISTICS						
SCL Clock Frequency	f_{SCL}				100	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN}	Any pulse narrower than the max spec is suppressed.			50	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	From SCL falling crossing V_{IH}(min), until SDA exits the V_{IL}(max) to V_{IH}(min) window.			3.5	µs
Time the Bus Must Be Free Before Start of New Transmission	t_{BUF}	SDA crossing V_{IH}(min) during a STOP condition to SDA crossing V_{IH}(min) during the following START condition.	4.7			µs
Clock Low Time	t_{LOW}	Measured at the V_{IL}(max) crossing.	4.7			µs
Clock High Time	t_{HIGH}	Measured at the V_{IH}(min) crossing.	4.0			µs
Start Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing the V_{IH}(min) level.	4.7			µs
Start Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing V_{IL}(max) to SCL falling edge crossing V_{IH}(min).	4.0			µs
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the V_{IL}(max) to V_{IH}(min) window to SCL rising edge crossing V_{IL}(min).	250			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing V_{IH}(min) to SDA entering the V_{IL}(max) to V_{IH}(min) window.	300			µs
Stop Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing V_{IH}(min) to SDA rising edge crossing V_{IL}(max).	4.0			µs
Stop Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing V_{IH}(min).	4.0			µs
Data Output Hold Time	t_{DH}	From SCL falling edge crossing V_{IL}(max) until SDA enters the V_{IL}(max) to V_{IH}(min) window. (Note 4)	0			ns
SDA and SCL Rise Time	t_R	From V_{IL}(max) to V_{IH}(min).			1000	ns
SDA and SCL Fall Time	t_F	From V_{IH}(min) to V_{IL}(max).			300	ns
Capacitive Loading Of SDA Or SCL (Note 5)	Cb	Total on-chip and off-chip			400	pF
SDA and SCL Bus Pull-up Resistor-Off-Chip (Note 5)	R_{OUT}	Maximum is determined by t_R and t_F. For C_B = 400pF, max is about 2kΩ ~ 2.5kΩ For C_B = 40pF, max is about 15kΩ to 20kΩ	1			kΩ
Input Leakage Current (SCL, SDA)	I_{LI}		-10		10	µA
Input Buffer Low Voltage (SCL, SDA)	V_{IL}	Voltage relative to V_{SS} of the device.	-0.3		V_{RGO} x 0.3	V

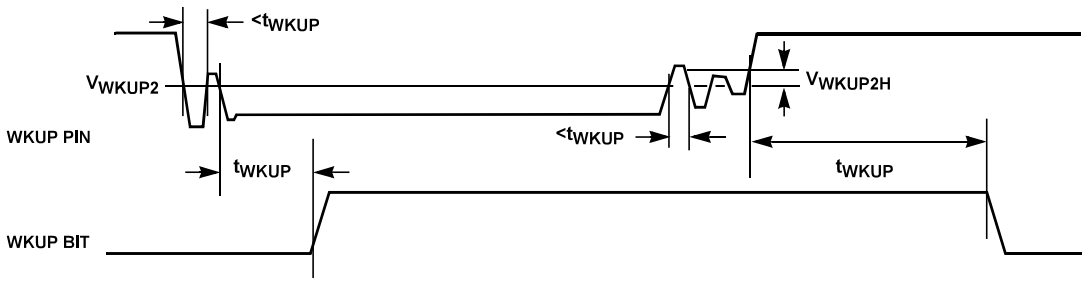
Operating Specifications Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested **(Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Buffer High Voltage (SCL, SDA)	V_{IH}	Voltage relative to V_{SS} of the device.	V_{RGO} x 0.7		V_{RGO} + 0.1	V
Output Buffer Low Voltage (SDA)	V_{OL}	I_{OL} = 1mA			0.4	V
SDA and SCL Input Buffer Hysteresis (Note 5)	I^2CHYST	Sleep bit = 0	0.05 * V_{RGO}			V

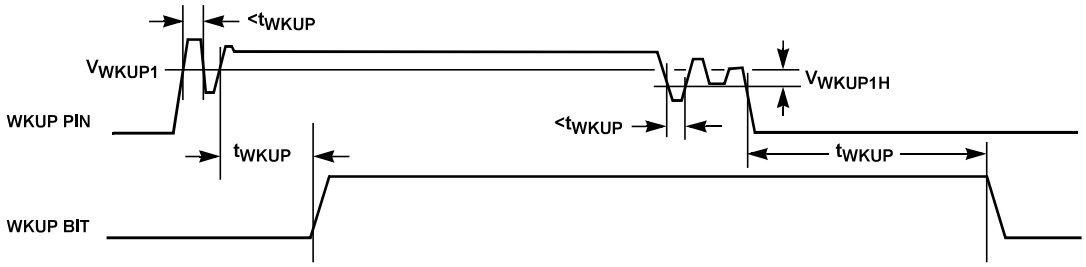
NOTES:

3. Power-up of the device requires all V_{CELL1}, V_{CELL2}, V_{CELL3}, and VCC to be above the limits specified.
4. The device provides an internal hold time of at least 300ns for the SDA signal to bridge the unidentified region of the falling edge of SCL.
5. Limits should be considered typical and are not production tested.
6. Typical 5Ω ±2Ω, based on characterization data.
7. Maximum output capacitance = 15pF.

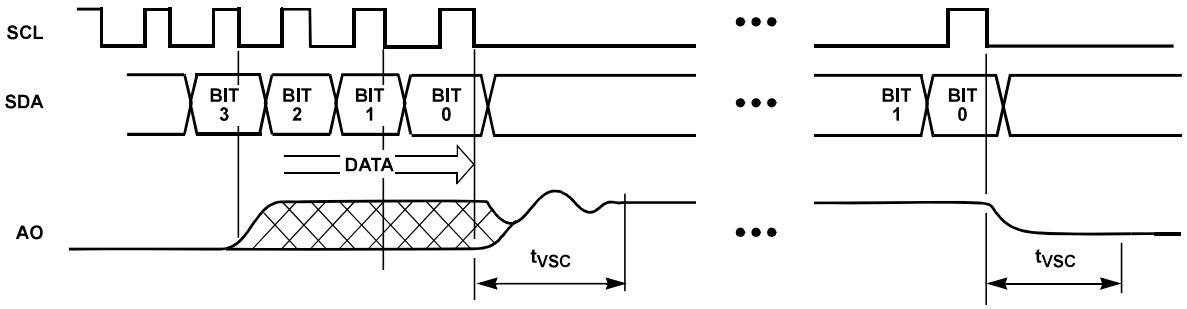
Wake up timing (WKPOL = 0)



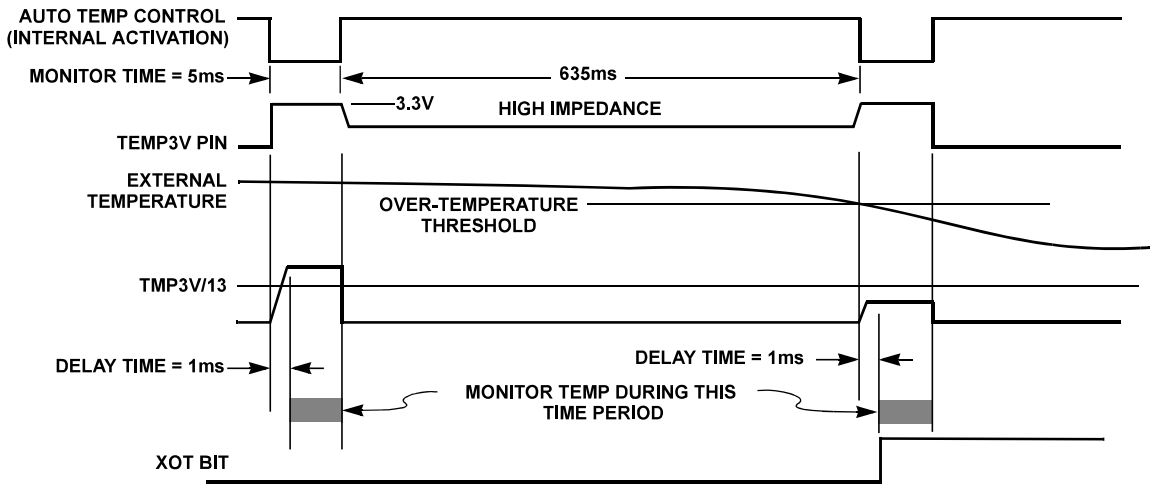
Wake up timing (WKPOL = 1)



Change in Voltage Source

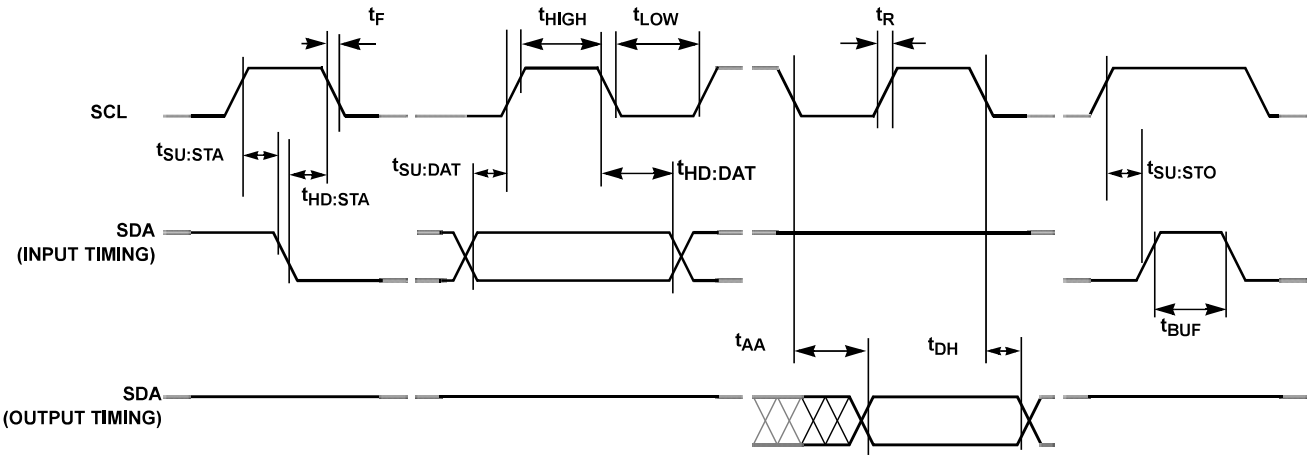


Automatic Temperature Scan



Serial Interface Timing Diagrams

Bus Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM LOW TO HIGH	WILL CHANGE FROM LOW TO HIGH
	MAY CHANGE FROM HIGH TO LOW	WILL CHANGE FROM HIGH TO LOW

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGES ALLOWED	CHANGING: STATE NOT KNOWN
	N/A	CENTER LINE IS HIGH IMPEDANCE

Registers

TABLE 1. REGISTERS

ADDR	REGISTER	READ/WRITE	7	6	5	4	3	2	1	0
00H	Config/Op Status	Read only	**Reserved**	**Reserved**	**SA** Single AFE	**WKUP** WKUP pin Status	**Reserved**	**Reserved**	**Reserved**	**Reserved**
01H	Operating Status (Note 10)	Read only	**Reserved**	**Reserved**	**XOT** Ext over temp	**IOT** Int over Temp	**Reserved**	**Reserved**	**Reserved**	**Reserved**
02H	Not Used	Read/Write	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
03H	Analog Out	Read/Write	**UFLG1** User Flag 1	**UFLG0** User Flag 0	**Reserved**	**Reserved**	**AO3**	**AO2**	**AO1**	**AO0**
							Analog output select bits			
04H	Control	Read/Write	**SLEEP** Force Sleep (Note 11)	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
05H	Not Used	Read/Write	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
06H	Not Used	Read/Write	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
07H	Feature Set	Read/Write (Write only if FSETEN bit set)	**ATMPOFF** Turn off automatic external temp scan	**DIS3** Disable 3.3V reg. (device requires external 3.3V)	**TMP3ON** Turn on Temp3V	**Reserved**	**Reserved**	**POR** Force POR	**DISWKUP** Disable WKUP pin	**WKPOL** Wake Up Polarity
08H	Write Enable	Read/Write	**FSETEN** Enable Feature Set writes	**Reserved**	**Reserved**	**UFLG3** User Flag 3	**UFLG2** User Flag 2	**Reserved**	**Reserved**	**Reserved**
09H:FFH	Reserved	NA	**RESERVED**							

NOTES:

8. A “1” written to a control or configuration bit causes the action to be taken. A “1” read from a status bit indicates that the condition exists.
9. “Reserved” indicates that the bit or register is reserved for future expansion. When writing to addresses 2, 3, 4, and 8: write a reserved bit with the value “0”. Do not write to reserved registers at addresses 09H through FFH. Ignore reserved bits that are returned in a read operation.
10. These status bits are automatically cleared when the register is read. All other status bits are cleared when the condition is cleared.
11. This SLEEP bit is cleared on initial power up, by the WKUP pin going high (when WKPOL = ”1”) or by the WKUP pin going low (when WKPOL = ”0”), and by writing a “0” to the location with an I^2C command.

Status Registers

TABLE 2. CONFIG/OP STATUS REGISTER (ADDR: 00H)

BIT	FUNCTION	DESCRIPTION
7	**RESERVED**	Reserved for future expansion.
6	**RESERVED**	Reserved for future expansion.
5	**SA** Single AFE	Indicates the device is an ISL94201. This bit is set in the chip and cannot be changed.
4	**WKUP** Wakeup pin status	This bit is set and reset by hardware. When ‘WKPOL’ is HIGH: ’WKUP’ HIGH = WKUP pin > Threshold voltage ‘WKUP’ LOW = WKUP pin < Threshold voltage When ‘WKPOL’ is LOW: ’WKUP’ HIGH = WKUP pin < Threshold voltage ‘WKUP’ LOW = WKUP pin > Threshold voltage
3	**RESERVED**	Reserved for future expansion.

TABLE 2. CONFIG/OP STATUS REGISTER (ADDR: 00H) (Continued)

BIT	FUNCTION	DESCRIPTION
2	RESERVED	Reserved for future expansion.
1	RESERVED	Reserved for future expansion.
0	RESERVED	Reserved for future expansion.

TABLE 3. OPERATING STATUS REGISTER (ADDR: 01H)

BIT	FUNCTION	DESCRIPTION
7	RESERVED	Reserved for future expansion.
6	RESERVED	Reserved for future expansion.
5	XOT Ext Over-temp	This bit is set to “1” when the external thermistor indicates an over-temperature condition. If the temperature condition has cleared, this bit is reset when the register is read.
4	IOT Int Over-temp	This bit is set to “1” when the internal thermistor indicates an over-temperature condition. If the temperature condition has cleared, this bit is reset when the register is read.
3	RESERVED	Reserved for future expansion.
2	RESERVED	Reserved for future expansion.
1	RESERVED	Reserved for future expansion.
0	RESERVED	Reserved for future expansion.

Control Registers

TABLE 4. ANALOG OUT CONTROL REGISTER (ADDR: 03H)

BITS	FUNCTION		DESCRIPTION	
7	UFLG1 User Flag 1		General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.	
6	UFLG0 User Flag 0		General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.	
5:4	RESERVED		Reserved for future expansion	
BIT 3 AO3	BIT 2 AO2	BIT 1 AO1	BIT 0 AO0	OUTPUT VOLTAGE
0	0	0	0	No Output (low power state)
0	0	0	1	V_{CELL1}
0	0	1	0	V_{CELL2}
0	0	1	1	V_{CELL3}
0	1	0	0	V_{CELL4}
0	1	0	1	V_{CELL5}
0	1	1	0	V_{CELL6}
0	1	1	1	V_{CELL7}
1	0	0	0	External Temperature
1	0	0	1	Internal Temperature
1	x	1	x	RESERVED
1	1	x	x	RESERVED

Configuration Registers

The device is configured for specific application requirements using the Configuration Registers. The configuration registers consist of SRAM memory. This memory is powered by the RGO output. In a sleep condition, an internal switch converts power for the contents of these registers from RGO to the VCELL1 input.

TABLE 5. CONTROL REGISTER (ADDR: 04H)

BIT	FUNCTION	DESCRIPTION
7	**SLEEP** Force Sleep	Setting this bit to “1” forces the device to go into a sleep condition. This turns off the voltage regulator. The SLEEP bit is automatically reset to “0” when the device wakes up. This bit does not reset the AO3:AO0 bits.
6:0	**RESERVED**	Reserved for future expansion.

TABLE 6. FEATURE SET CONFIGURATION REGISTER (ADDR: 07H)

BIT	FUNCTION	DESCRIPTION
7	**ATMPOFF** Turn off automatic external temp scan	When set to ‘1’ this bit disables the automatic temperature scan. When set to ‘0’, the temperature is turned on for 5ms in every 640ms.
6	**DIS3** Disable 3.3V regulator	Setting this bit to “1” disables the internal 3.3V regulator. Setting this bit to “1” requires that there be an external 3.3V regulator connected to the RGO pin.
5	**TMP3ON** Turn on Temp 3.3V	Setting this bit to “1” turns ON the TEMP3V output to the external temperature sensor. The output will remain on as long as this bit remains “1”.
4	**RESERVED**	Reserved for future expansion.
3	**RESERVED**	Reserved for future expansion.
2	**POR** Force POR	Setting this bit to “1” forces a POR condition. This resets all internal registers to zero.
1	**DISWKUP** Disable WKUP pin	Setting this bit to “1” disables the WKUP pin function. CAUTION: Setting this pin to ‘1’ prevents a wake up condition. If the device then goes to sleep, it cannot be waken without a communication link that resets this bit, or by power cycling the device.
0	**WKPOL** Wake Up Polarity	Setting this bit to “1” sets the device to wake up on a rising edge at the WKUP pin. Setting this bit to “0” sets the device to wake up on a falling edge at the WKUP pin.

TABLE 7. WRITE ENABLE REGISTER (ADDR: 08H)

BIT	FUNCTION	DESCRIPTION
7	**FSETEN** Enable discharge set writes	When set to “1”, allows writes to the Feature Set register. When set to “0”, prevents writes to the Feature Set register (Addr: 07H). Default on initial power up is “0”.
6	**RESERVED**	Reserved for future expansion.
5	**RESERVED**	Reserved for future expansion.
4	**UFLG3** User Flag 3	General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.
3	**UFLG2** User Flag 3	General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.
2	**RESERVED**	Reserved for future expansion.
1	**RESERVED**	Reserved for future expansion.
0	**RESERVED**	Reserved for future expansion.

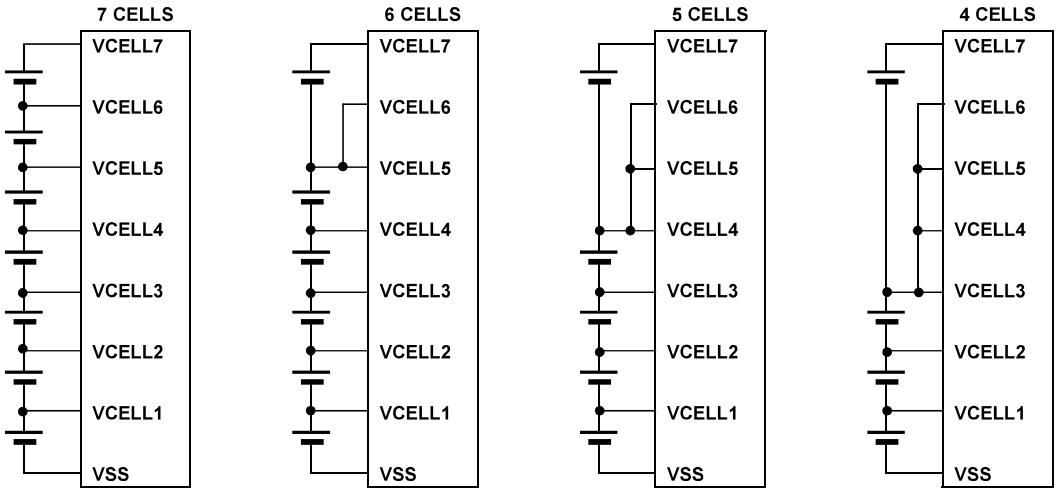
Device Description

Design Theory

Instructed by the microcontroller, the ISL94201 performs cell voltage and temperature monitoring.

Battery Connection

The ISL94201supports packs of 5 to 7 series connected Li-ion cells. Connection guidelines for each cell combination are shown in Figure 1.



Note: Multiple cells can be connected in parallel

FIGURE 1. BATTERY CONNECTION OPTIONS

System Power-Up/Power-Down

The ISL94201 powers up when the voltages on V_{CELL1}, V_{CELL2}, V_{CELL3} and VCC all exceed their POR threshold. At this time, the ISL94201 wakes up and turns on the RGO output.

RGO provides a regulated 3.3VDC ±10% voltage at pin RGO. It does this by using a control voltage on the RGC pin to drive an external NPN transistor (see Figure 2.) The transistor should have a beta of at least 70 to provide ample current to the device and external circuits and should have a V_{CE} of greater than 30V (preferably 50V). The voltage at the emitter of the NPN transistor is monitored and regulated to 3.3V by the control signal RGC. RGO also powers most of the ISL94201internal circuits. A 500Ω resistor is recommended in the collector of the NPN transistor to minimize initial current surge when the regulator turns on.

Once powered up, the device remains in a wake up state until put to sleep by the microcontroller (typically when the cells drop too low in voltage) or until the V_{CELL1}, V_{CELL2}, V_{CELL3} or VCC voltages drop below their POR threshold.

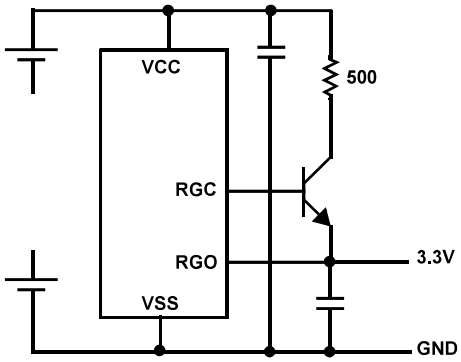


FIGURE 2. VOLTAGE REGULATOR CIRCUITS

WKUP Pin Operation

There are two ways to design a wake up of the ISL94201. In an active LOW connection (WKPOL = “0” - default), the device wakes up when a charger is connected to the pack. This pulls the WKUP pin low when compared to a reference based on the V_{CELL1} voltage. In an active HIGH connection (WKPOL = ‘1’) the device wakes up when the WKUP pin is pulled high by a connection through an external switch.

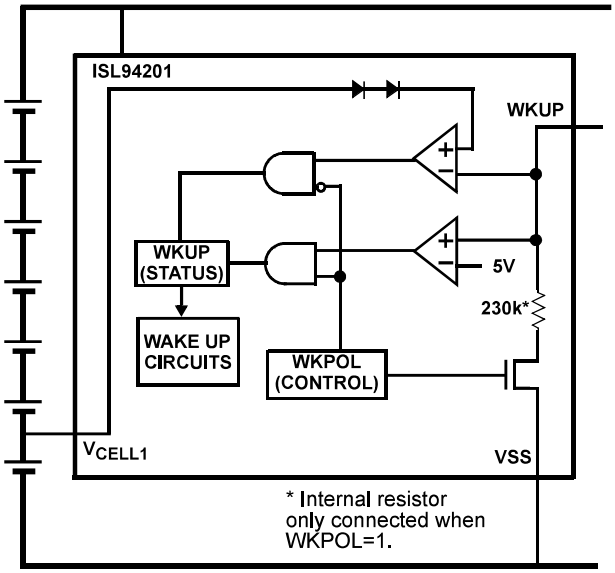


FIGURE 3. WAKE UP CONTROL CIRCUITS

Protection Functions

In the default recommended condition, the ISL94201automatically detects internal over-temperature, and external over-temperature conditions. The designer programs the microcontroller to respond to the over-temperature indications.

OVER-TEMPERATURE SAFETY FUNCTIONS

External Temperature Monitoring

The external temperature is monitored by using a voltage divider consisting of a fixed resistor and a thermistor. This divider is powered by the ISL94201TEMP3V output. This output is normally controlled so it is on for only short periods to minimize current consumption.

Without microcontroller intervention, and in the default state, the ISL94201provides an automatic temperature scan. This scan circuit repeatedly turns on TEMP3V output (and the external temperature monitor) for 5ms out of every 640ms. In this way, the external temperature is monitored even if the microcontroller is asleep.

When the TEMP3V output turns on, the ISL94201waits 1ms for the temperature reading to stabilize, then compares the external temperature voltage with an internal voltage divider that is set to TEMP3V/13. When the thermistor voltage is below the reference threshold after the delay, an external temperature fail condition exists. To set the external over-temperature limit, set the value of R_X resistor to 12x the resistance of the thermistor at the over-temp threshold.

The TEMP3V output pin also turns on when the microcontroller sets the AO3:AO0 bits to select that the external temperature voltage. This causes the TEMPI voltage to be placed on AO and activates (after 1ms) the over-temperature detection. As long as the AO3:AO0 bits point to the external temperature, the TEMP3V output remains on.

Because of the manual scan of the temperature, it may be desired to turn off the automatic scan, although they can be used at the same time without interference. To turn off the automatic scan, set the ATMPOFF bit.

The microcontroller can over-ride both the automatic temperature scan and the microcontroller controlled temperature scan by setting the TEMP3ON configuration bit. This turns on the TEMP3V output to keep the temperature control voltage on all the time, for a continuous monitoring of an over-temperature condition. This likely will consume a significant amount of current, so this feature is usually used for special or test purposes.

Analog Multiplexer Selection

The ISL94201devices can be used to externally monitor individual battery cell voltages and temperatures. Each quantity can be monitored at the analog output pin (AO). The desired voltage is selected using the I^2C interface and the AO3:AO0 bits. See Figure 5.

VOLTAGE MONITORING

Since the voltage on each of the Li-ion Cells are normally higher than the regulated supply voltage, and since the voltages on the upper cells is much higher than is tolerated by a microcontroller, it is necessary to both level shift and divide the voltage before it can be monitored by the microcontroller or an external A/D converter. To get into the voltage range required by the external circuits, the voltage level shifter divides the cell voltage by 2 and references it to VSS. Therefore, a Li-ion cell with a voltage of 4.2V becomes a voltage of 2.1V on the AO pin.

TEMPERATURE MONITORING

The voltage representing the external temperature applied at the TEMPI terminal is directed to the AO terminal through a MUX, as selected by the AO control bits (see Figures 4 and 5). The external temperature voltage is not divided by 2 as are the cell voltages. Instead it is a direct reflection of the voltage at the TEMPI pin.

A similar operation occurs when monitoring the internal temperature through the AO output, except there is no external “calibration” of the voltage associated with the internal temperature. For the internal temperature monitoring, the voltage at the output is linear with respect to temperature. See “Operating Specifications” for information about the output voltage at +25°C and the output slope relative to temperature on page 4.

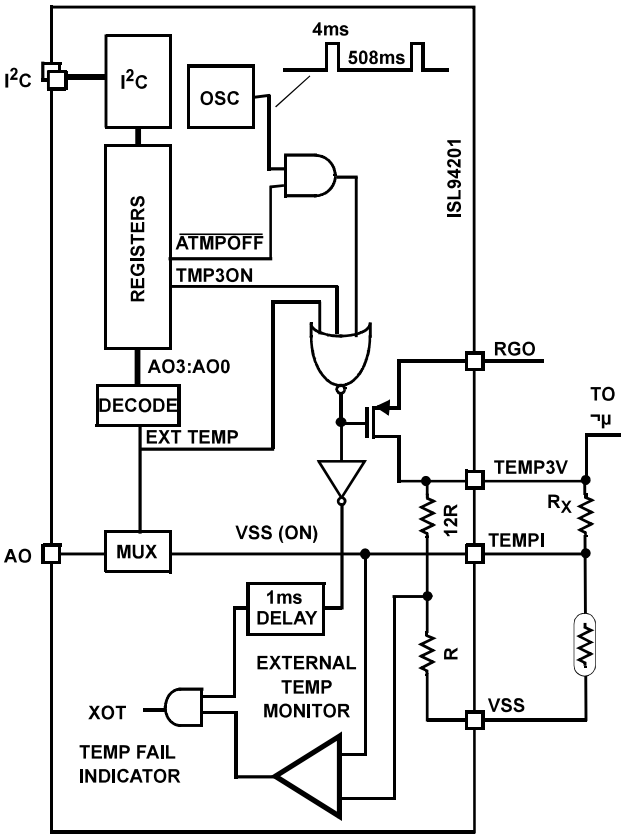


FIGURE 4. EXTERNAL TEMPERATURE MONITORING AND CONTROL

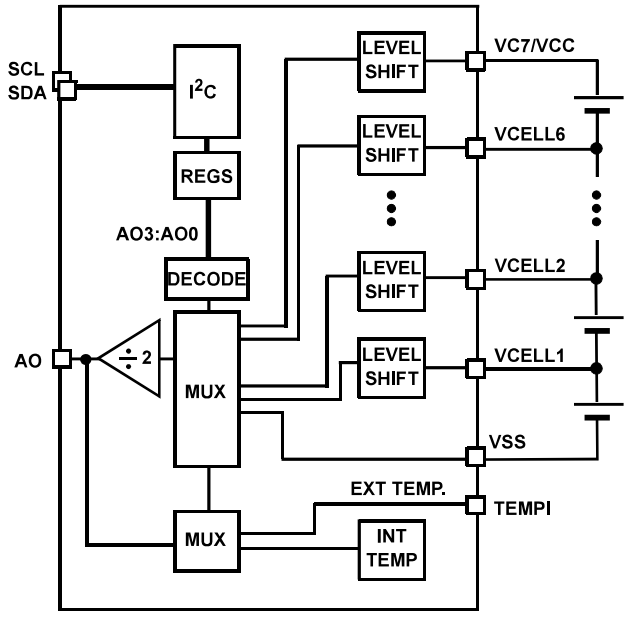


FIGURE 5. ANALOG OUTPUT MONITORING DIAGRAM

User Flags

The ISL94201contains four flags in the register area that the microcontroller can use for general purpose indicators. These bits are designated UFLG3, UFLG2, UFLG1, and UFLG0. The microcontroller can set or reset these bits by writing into the appropriate register.

The user flag bits are battery backed up, so the contents remain even after exiting a sleep mode. However, if the microcontroller sets the POR bit to force a power on reset, all of the user flags will also be reset. In addition, if the voltage on cell1 ever drops below the POR voltage, the contents of the user flags (as well as all other register values) could be lost.

Serial Interface

INTERFACE CONVENTIONS

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the ISL94201devices operate as slaves in all applications.

When sending or receiving data, the convention is the most significant bit (MSB) is sent first. So, the first address bit sent is Bit 7.

CLOCK AND DATA

Data states on the SDA line can change only while SCL is LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 6.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 7.

STOP CONDITION

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition is only issued after the transmitting device has released the bus. See Figure 7.

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge that it received the eight bits of data. See Figure 8.

The device responds with an acknowledge after recognition of a start condition and the correct slave byte. If a write operation is selected, the device responds with an acknowledge after the receipt of each subsequent eight bits. The device acknowledges all incoming data and address bytes, except for the slave byte when the contents do not match the device's internal slave address.

In the read mode, the device transmits eight bits of data, releases the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continues to transmit data. The device terminates further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

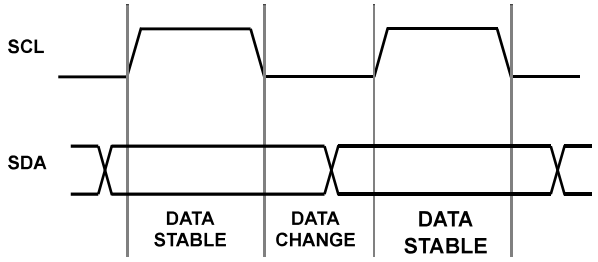


FIGURE 6. VALID DATA CHANGES ON I^2C BUS

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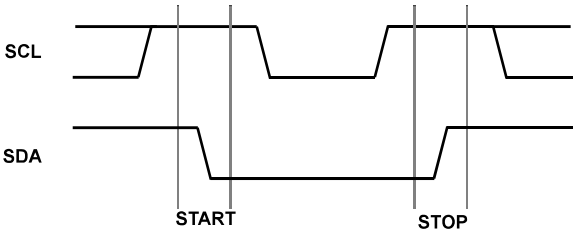


FIGURE 7. I^2C START AND STOP BITS

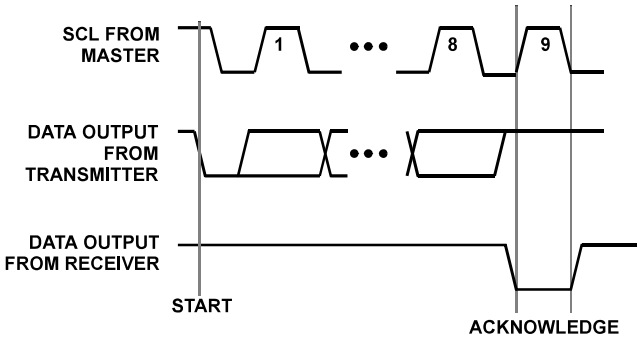


FIGURE 8. ACKNOWLEDGE RESPONSE FROM RECEIVER

WRITE OPERATIONS

For a write operation, the device requires a slave byte and an address byte. The slave byte specifies the particular device on the I^2C bus that the master is writing to. The address specifies one of the registers in that device. After receipt of each byte, the device responds with an acknowledge, and awaits the next eight bits from the master. After the acknowledge, following the transfer of data, the master terminates the transfer by generating a stop condition. See Figure 9.

When receiving data from the master, the value in the data byte is transferred into the register specified by the address byte on the falling edge of the clock following the 8th data bit.

After receiving the acknowledge after the data byte, the device automatically increments the address. So, before sending the stop bit, the master may send additional data to the device without re-sending the slave and address bytes. After writing to address 0AH, the address "wraps around" to address 0. Do not continue to write to addresses higher than address 08H, since these addresses access registers that are reserved. Writing to these locations can result in unexpected device operation.

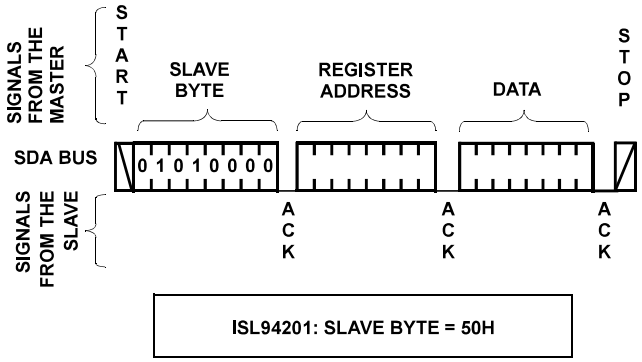


FIGURE 9. WRITE SEQUENCE

Read Operations

Read operations are initiated in the same manner as write operations with the host sending the address where the read is to start (but no data). Then, the host sends an ACK, a repeated start, and the slave byte with the LSB = 1. After the device acknowledges the slave byte, the device sends out one bit of data for each master clock. After the slave sends eight bits to the master, the master sends a NACK (Not acknowledge) to the device, to indicate the data transfer is complete, then the master sends a stop bit. See Figure 10.

After sending the eighth data bit to the master, the device automatically increments its internal address pointer. So the master, instead of sending a NACK and the stop bit, can send additional clocks to read the contents of the next register - without sending another slave and address byte.

If the last address read or written is known, the master can initiate a current address read. In this case, only the slave byte is sent before data is returned. See Figure 10.

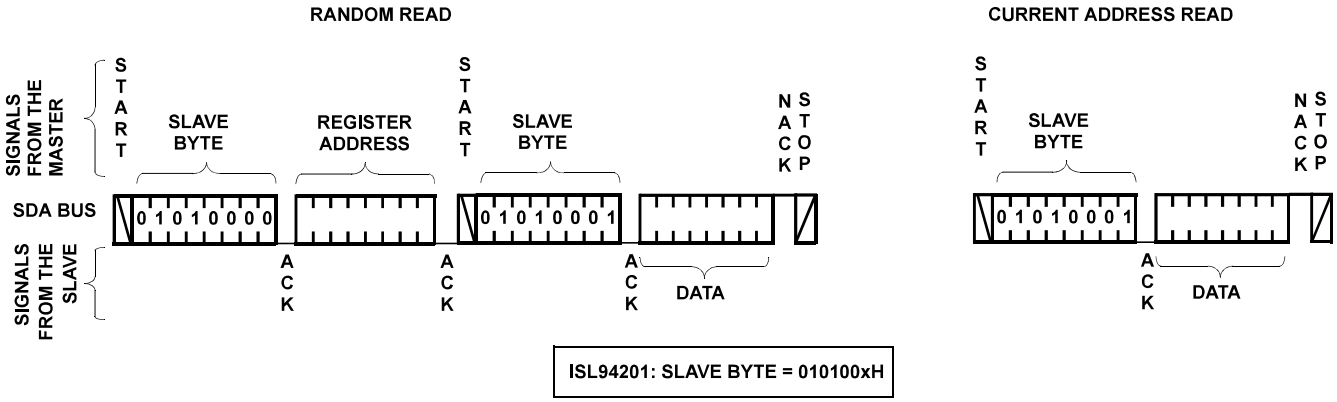


FIGURE 10. READ SEQUENCE

Register Protection

The Feature Set configuration register is write protected on initial power up. In order to write to these registers it is necessary to set a bit to enable each one. These write enable bits are in the Write Enable register (Address 08H).

Write the FSETEN bit (Addr 8:bit 7) to “1” to enable changes to the data in the Feature Set register (Address 7).

The microcontroller can reset this bits back to zero to prevent inadvertent writes that change the operation of the pack.

Operation State Machine

Figure 11 shows a device state machine which defines how the ISL94201responds to various conditions.

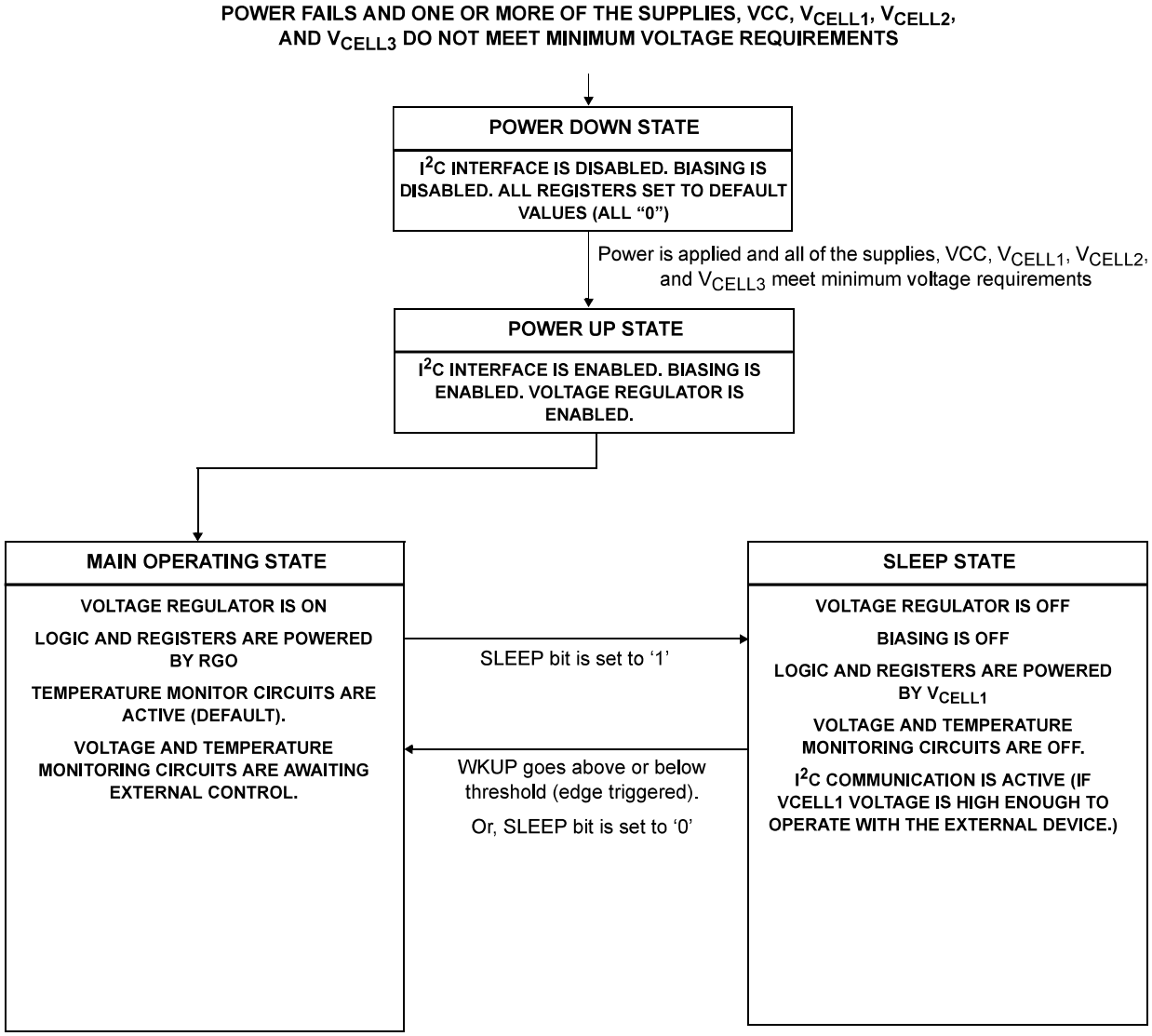


FIGURE 11. DEVICE OPERATION STATE MACHINE

Applications Circuits

The following application circuits are ideas to consider when developing a battery pack implementation. There are many more ways that the pack can be designed.

Also refer to the ISL9208 or ISL9216 application guide for additional circuit design guidelines.

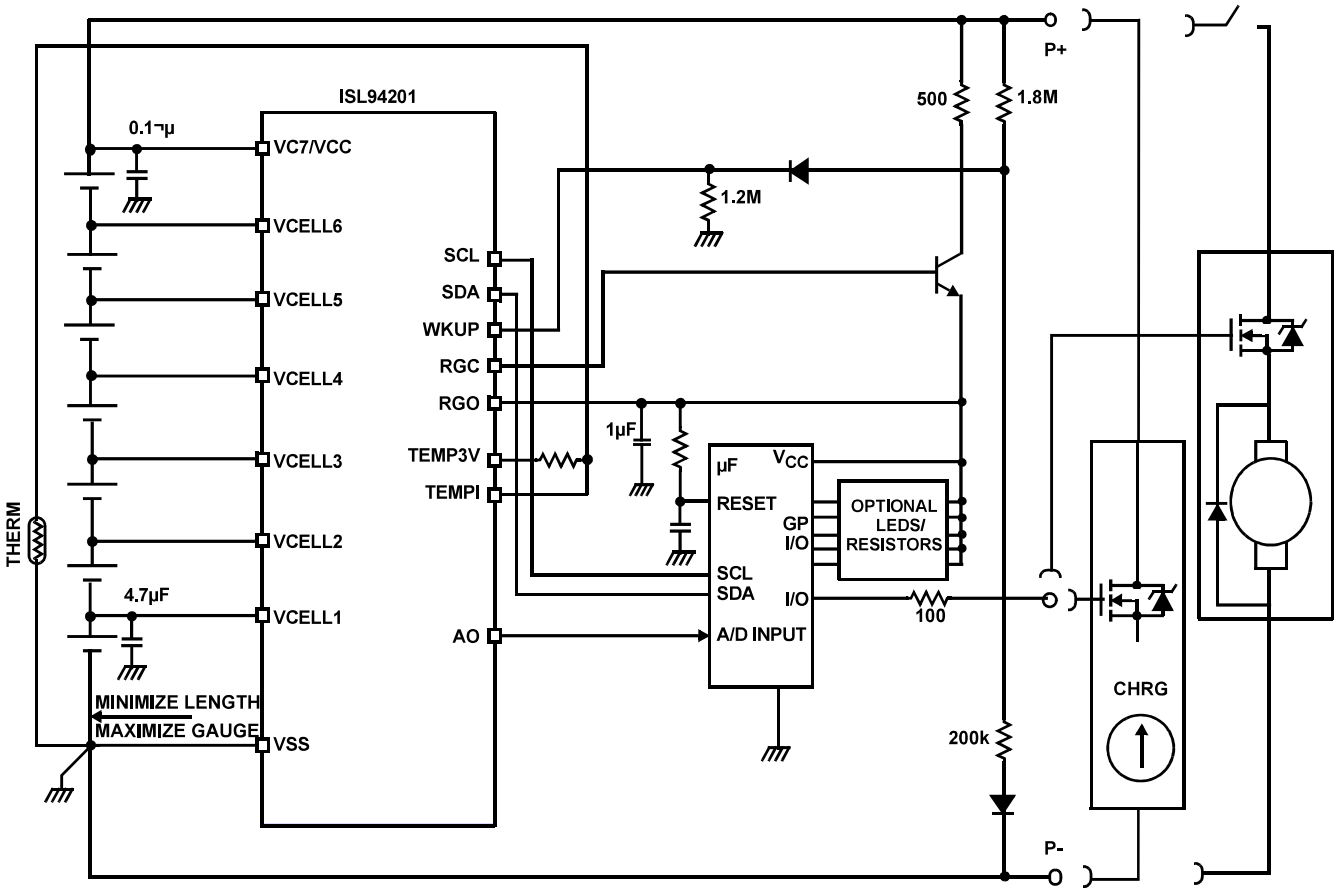


FIGURE 12. 7-CELL APPLICATION CIRCUIT INTEGRATED CHARGE/DISCHARGE

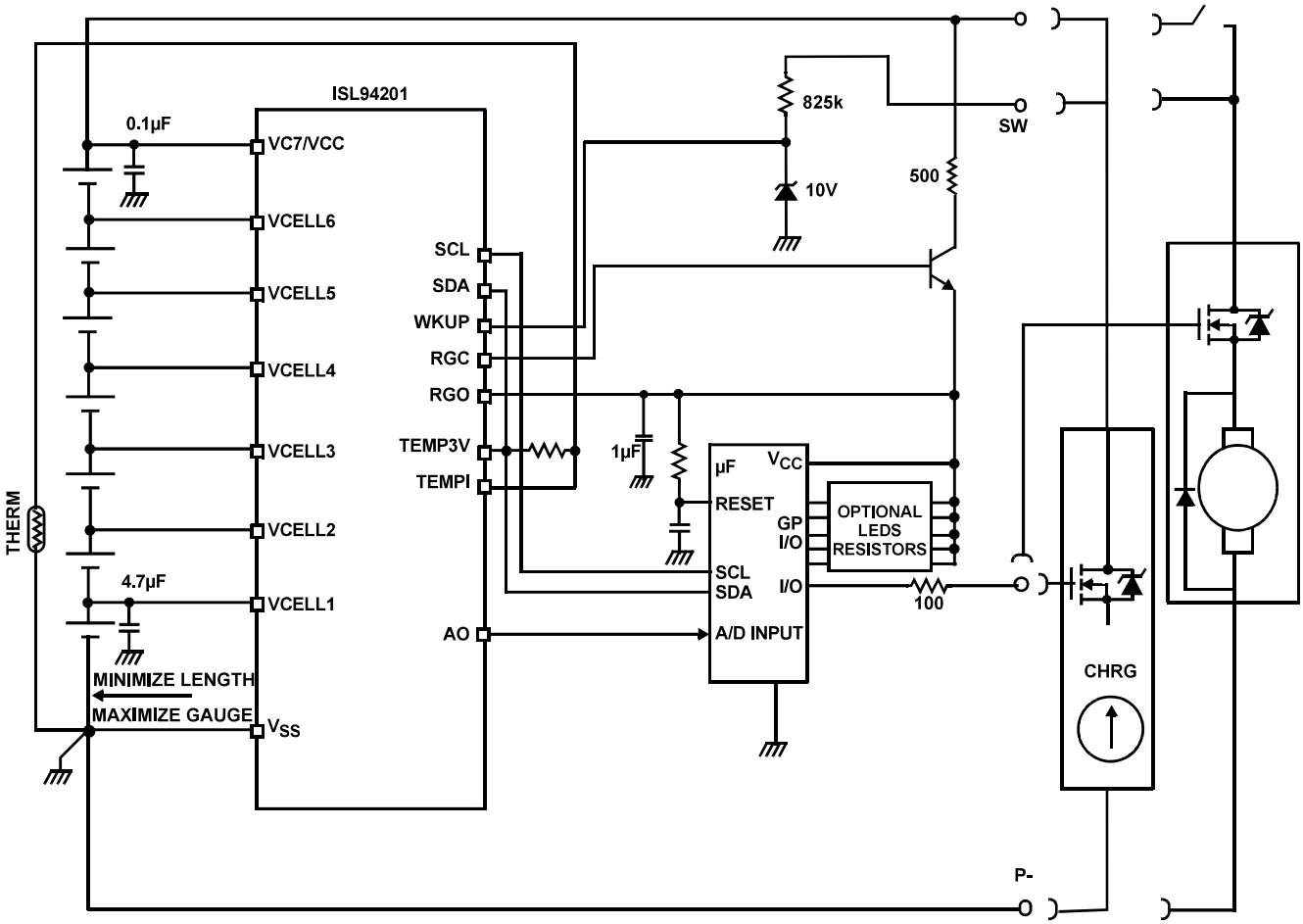
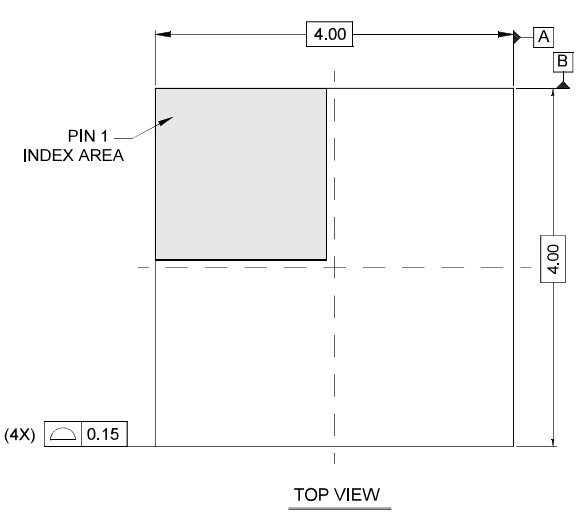


FIGURE 13. 7-CELL APPLICATION CIRCUIT WITH SWITCH WAKE-UP

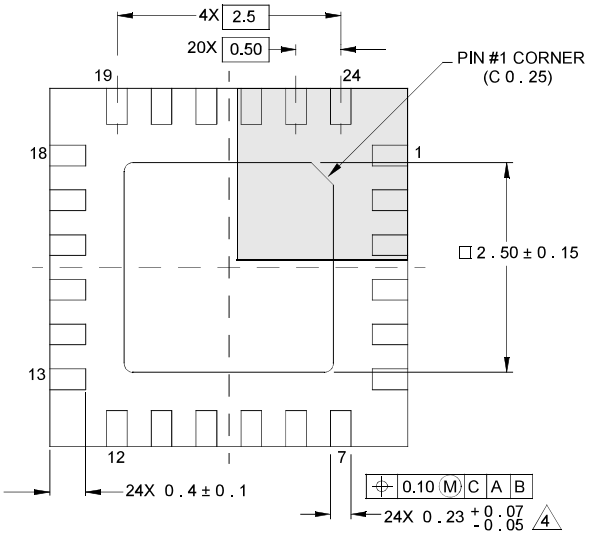
Package Outline Drawing

L24.4x4D

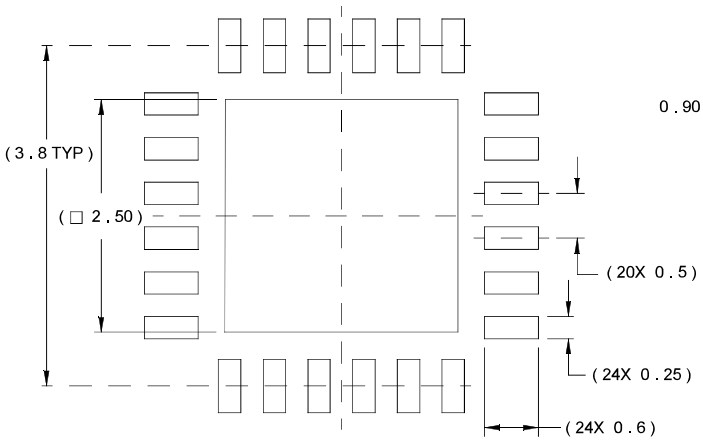
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



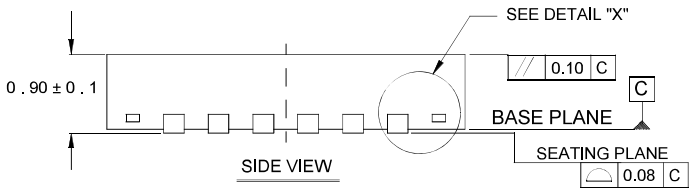
TOP VIEW



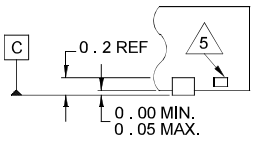
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.