L9963E

Datasheet

Automotive Multicell battery monitoring and balancing IC

TQFP 10x10 64L
exposed pad down

Product status link
L9963E

Product summary		
Order code	Package	Packing
L9963E	TQFP64EP	Tray
L9963E-TR		Tape and Reel

Product label
SUSTAINABLE TECHNOLOGY

Features

- AEC-Q100 qualified
- Measures 4 to 14 cells in series, with 0 µs desynchronization delay between samples. Supports also busbar connection without altering cell results
- Coulomb counter supporting pack overcurrent detection in both ignition on and off states. Fully synchronized current and voltage samples
- 16-bit voltage ADC with maximum error of ±2 mV in the [0.5 – 4.3] V range, after soldering, in [-40; +105] °C Tj range
- 2.66 Mbps isolated serial communication with regenerative buffer, supporting dual access ring. Less than 4 us latency between start of conversion of the 1st and the 31st device in a chain. Less than 4 ms to convert and read 96 cells in a system using 8 L9963E and L9963T transceiver. Less than 8 ms to convert and read 210 cells in a system using 15 L9963E and L9963T transceiver. Less than 16 ms to convert and read 434 cells in a system using 31 L9963E and L9963T transceiver. Supports both XFMR and CAP based isolation
- 200 mA passive internal balancing current for each cell in both normal and silent-balancing mode. Possibility of executing cyclic wake up measurements. Manual/Timed balancing, on multiple channels simultaneously; Internal/External balancing
- Fully redundant cell measurement path, with ADC Swap, for enhanced safety and limp home functionality
- Intelligent diagnostic routine providing automatic failure validation. Redundant fault notification through both SPI Global Status Word (GSW) and dedicated FAULT line
- Two 5 V regulators supporting external load connection with 25 mA (VCOM) and 50 mA (VTREF) current capability
- 9 GPIOs, with up to 7 analog inputs for NTC sensing
- Robust hot-plug performance. No Zeners needed in parallel to each cell
- Full ISO26262 compliant, ASIL-D systems ready

Application

- Automotive: 48 V and high-voltage battery packs
- Backup energy storage systems and UPS
- E-bikes, e-scooters
- Portable and semi-portable equipment

Description

The L9963E is a Li-ion battery monitoring and protecting chip for high-reliability automotive applications and energy storage systems. Up to 14 stacked battery cells can be monitored to meet the requirements of 48 V and higher voltage systems.

Each cell voltage is measured with high accuracy, as well as the current for the on-chip coulomb counting. The device can monitor up to 7 NTCs. The information is transmitted through SPI communication or isolated interface.

Multiple L9963E can be connected in a daisy chain and communicate with one host processor via the transformer isolated interfaces, featuring high-speed, low EMI, long distance, and reliable data transmission.

Passive balancing with programmable channel selection is offered in both normal and low power mode (silent balance). The balancing can be terminated automatically based on internal timer interrupt. Nine GPIOs are integrated for external monitoring and control. The L9963E features a comprehensive set of fault detection and notification functions to meet the safety standard requirements.

1 Device introduction

The L9963E is intended for operation in both hybrid (HE) and full electric (FE) vehicles using lithium battery packs. The IC embeds all the features needed to perform battery management. A single device can monitor from 4 up to 14 cells. Several devices can be stacked in a vertical arrangement in order to monitor up to 31 battery packs for a total of 434 series cells.

The device can be supplied with the same battery it monitors, and generates stable internal references by means of a voltage regulator and a bootstrap. Both units need to be surrounded by external components to be functional. It also features two internal bandgaps that are constantly monitored by internal circuitry to guarantee measurement precision. The microcontroller can also monitor the precision of the bandgap by reading the conversion of an internally generated voltage reference (VTREF).

L9963E main activity consists in monitoring cells and battery pack status through stack voltage measurement, cell voltage measurement, temperature measurement and coulomb counting. Measurement and diagnostic tasks can be executed either on demand or periodically, with a programmable cycle interval. Measurement data is available for an external microcontroller to perform charge balancing and to compute the State Of Health (SOH) and State Of Charge (SOC). In a typical use, the IC works in normal mode performing measurement conversions, diagnostics and communication; the device can also be put into a cyclic wake up state, in order to reduce the current consumption from the battery: while in this state, the main functions are activated periodically.

Passive cell balancing can be performed either via internal discharge path or via external MOSFETs. The controller can either manually control the balancing drivers or start a balancing task with a fixed duration. In the second case, the balancing may be programmed to continue also when the IC enters a low power mode called Silent Balancing, in order to avoid unnecessary current absorption from the battery pack.

Thanks to the GPIOs, the device also offers the possibility to operate a distributed cell temperature sensing via external NTCs resistances. In general, the GPIOs can be used to perform both absolute and differential voltage conversions. They can also be configured as digital inputs/outputs. The IC supports up to 7 NTCs.

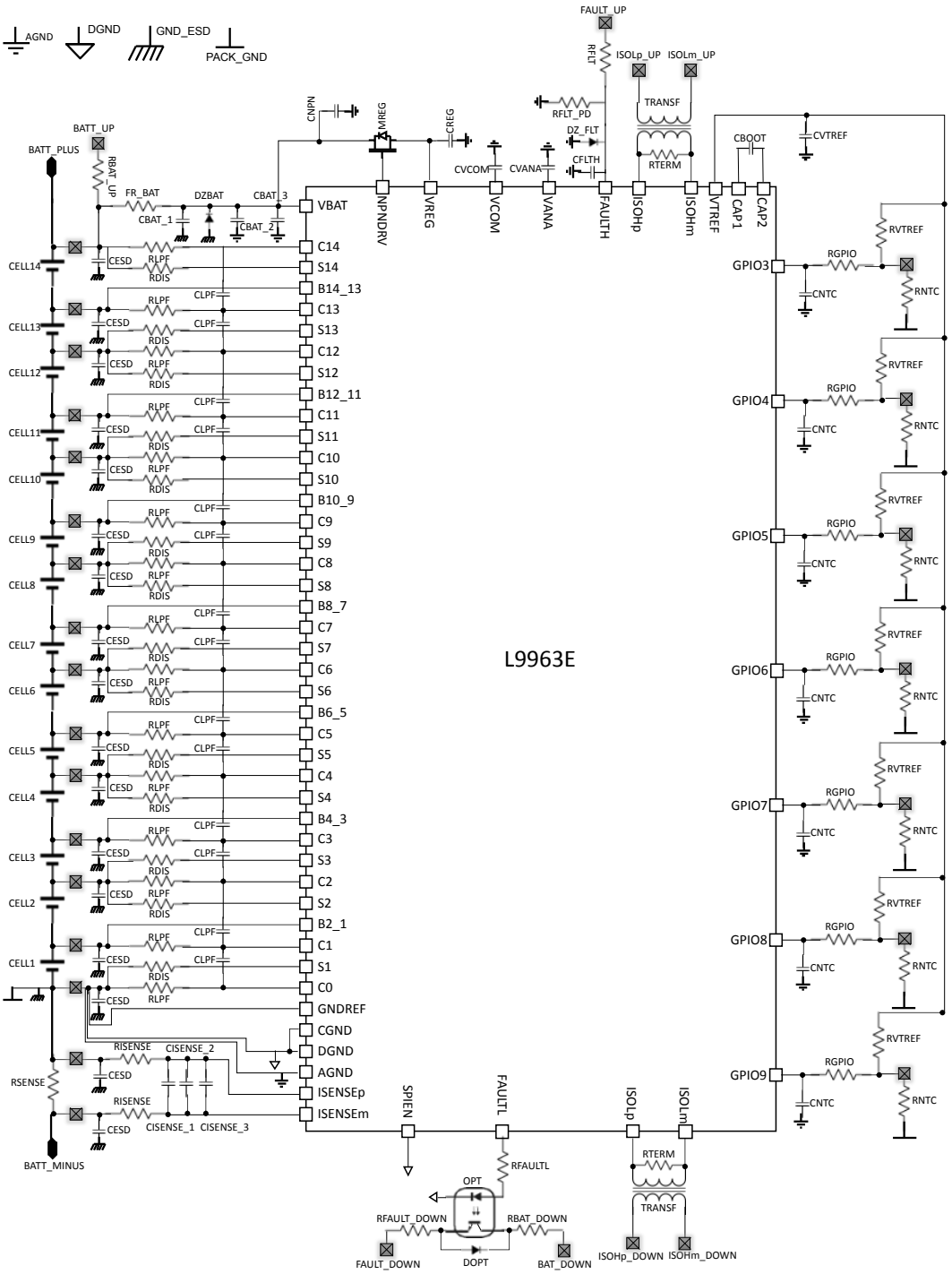
The external microcontroller can communicate with L9963E via SPI protocol, depending on the status of one pin at the startup (SPIEN pin). The physical layer can be either a classical 4-wire based SPI or a 2-wire, transformer/capacitive based, isolated interface through a dedicated isolated transceiver device. L9963E, in fact, can be used as a transceiver, acting as a bridge between the two physical layers. In case of multiple L9963E vertically arrayed, each L9963E communicates with the others by means of a vertical isolated interface. The microcontroller can either address a single device of the chain or send broadcast commands.

L9963E has been engineered to perform automatic validation of any failure involving the cells or the whole battery pack. The device is able to detect the loss of the connection to a cell or GPIO terminal. Moreover it features a HardWare Self Check (HWSC) that verifies the correct functionality of the internal analog comparators and the ADCs. All these checks are automatically performed in case a failure involving both cells or the battery pack is detected, in order to always provide reliable information to the external microcontroller. The current sensing interface used for coulomb counting is also capable of detecting failures such as open wires and overcurrent in sleep mode. Conversions for coulomb counting are validated by built in self-test of the precision and detecting any counter overflow. The cell balancing terminals can detect any short/open fault and the internal powerMOS are protected against overcurrent.

The stack voltage is monitored for OV/UV by three parallel and independent systems. They have been engineered to protect the IC against AMR violation, to detect any overvoltage event as per LV 148 and to provide the possibility to trim the OV/UV levels according to the application and the total number of cells. Moreover, all internal voltage regulators are equipped with UV/OV detection circuitry, that is also self-validated upon failure detection via HWSC. Ground loss detection has also been implemented. In case of overtemperature, thermal shutdown protects the IC. GPIOs are capable of detecting ‘stuck @’ faults when used as digital outputs. Communication integrity is guaranteed by CRC check, while trimming and calibration data is continuously checked against corruption. Protocol errors such as incorrect address, inconsistent frame and communication interruption will be detected.

Critical failure modes will trigger the assertion of a dedicated FAULT line (implemented via two GPIOs), propagating through the L9963E chain via external optocouplers and reaching the microcontroller. L9963E can guarantee the FAULT line integrity via a heartbeat routine.

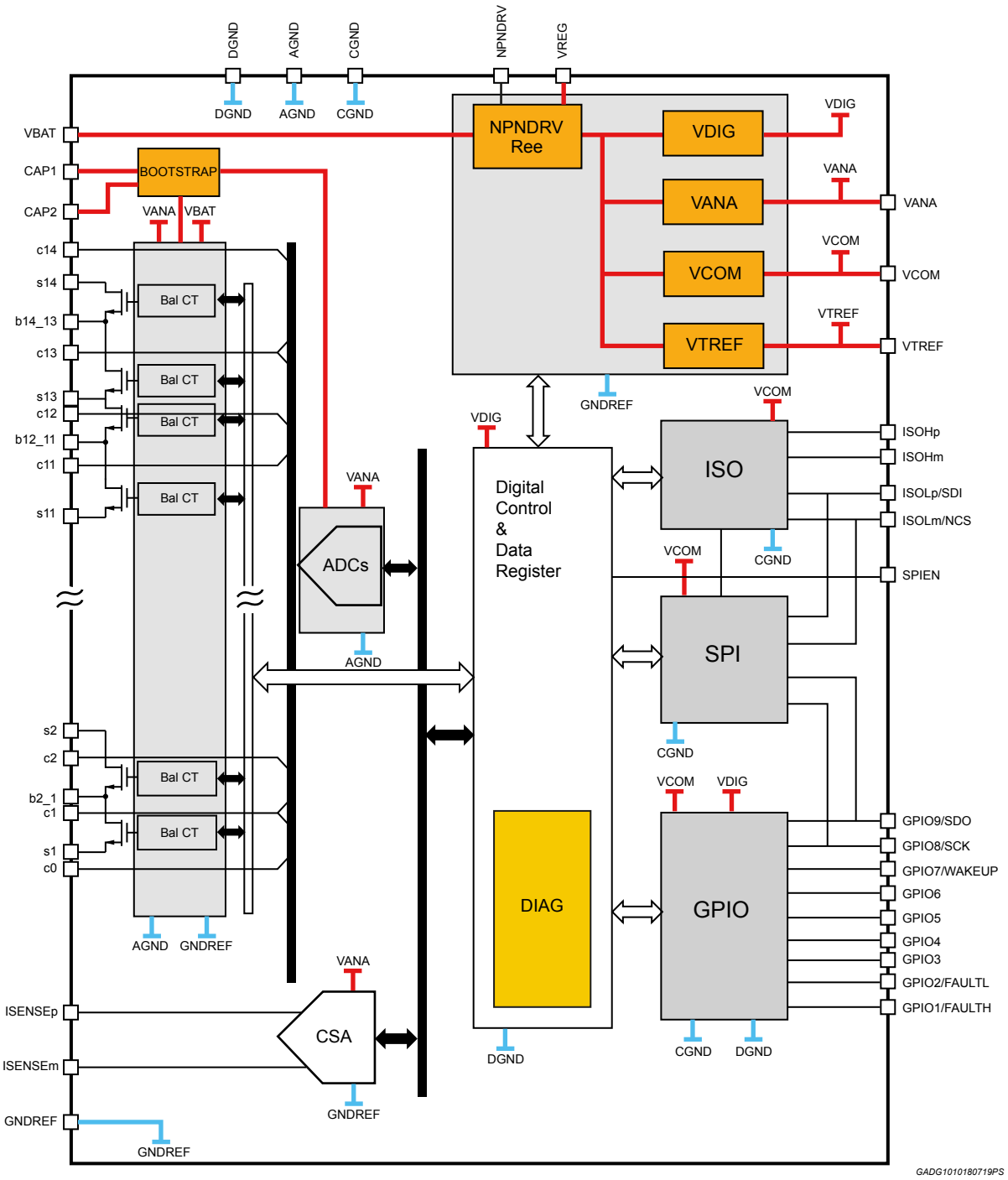
Figure 1. Typical application



2 Block diagram and pin description

2.1 Block diagram

Figure 2. **Block diagram**



2.2 Pin description

Figure 3. Pin connections (top view)

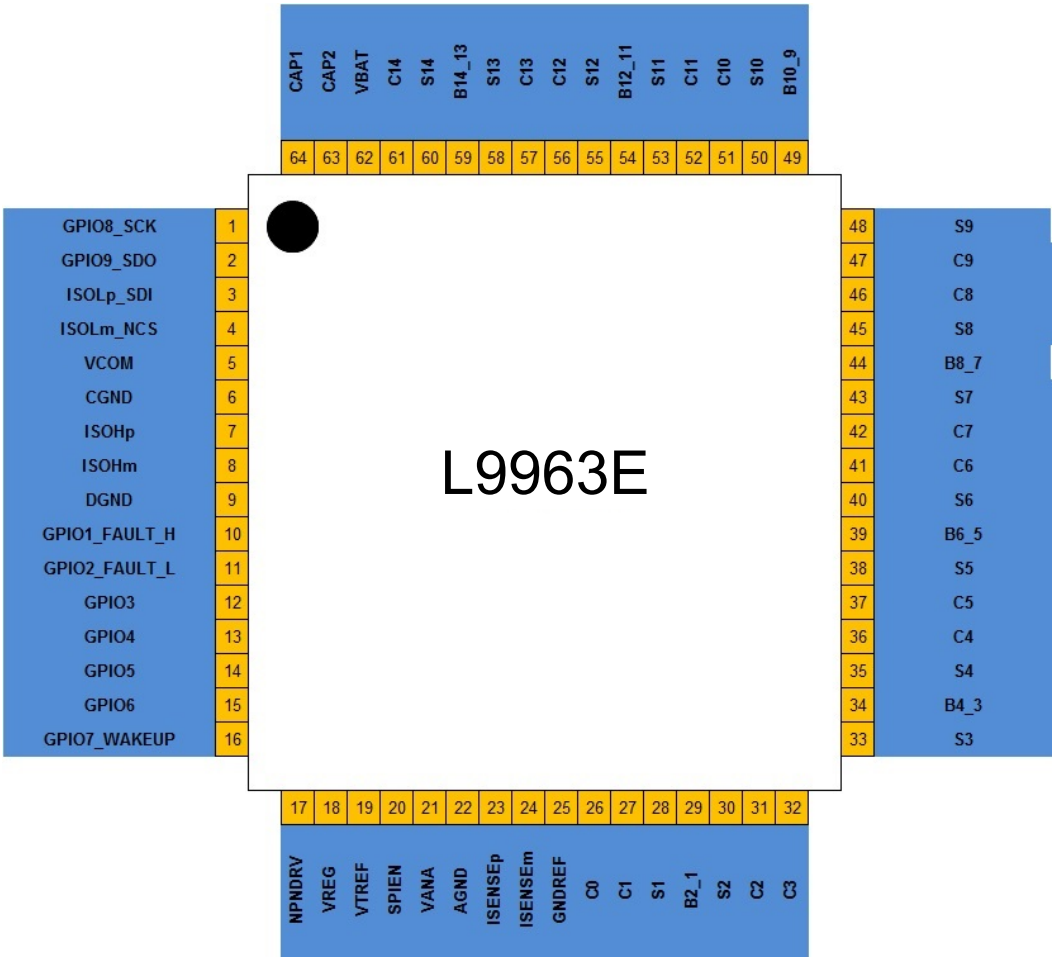


Table 1. Pin function

Pin #	Pin name	Description	I/O type(1)
1	GPIO8_ SCK	General-purpose I/O / Serial clock input (SPI). Its configuration is locked to Digital Input in case SPIEN = 1. Refer to Section 4.9 General purpose I/O: GPIOs. Generally used to sense NTCs when not configured as SPI. Refer to Section 6.9 NTC analog front end.	DO/DI/AI
2	GPIO9_ SDO	General-purpose I/O / Serial data output (SPI). Its configuration is locked to Digital Output in case SPIEN = 1. Refer to Section 4.9 General purpose I/O: GPIOs. Generally used to sense NTCs when not configured as SPI. Refer to Section 6.9 NTC analog front end.	DO/DI/AI
3	ISOLp_SDI	Non-inverting, low-side isolated serial communication port (isolated SPI) / Serial data input (SPI). Its configuration is locked to Digital Input in case SPIEN = 1. Refer to Section 4.2 Serial communication interface. When used as isolated SPI, refer to Section 6.8 ISO lines circuit.	DI/AIO
4	ISOLm_NCS	Inverting, low-side isolated serial communication port (isolated SPI) / Active low, Chip-Select input (SPI). Its configuration is locked to Digital Input in case SPIEN = 1. Refer to Section 4.2 Serial communication interface. When used as isolated SPI, refer to Section 6.8 ISO lines circuit.	DI/AIO

Pin #	Pin name	Description	I/O type(1)
5	VCOM	Regulated power supply used for communication interfaces. Connect a tank capacitor as indicated in Table 73. Can be used to supply external loads with a maximum I_{VCOM_ext} current budget.	P
6	CGND	Communication ground. Connect to DGND on top.	G
7	ISOHp	Non-inverting, high-side isolated serial communication port. Refer to Section 4.2.3 Isolated Serial Peripheral Interface. Refer to Section 6.8 ISO lines circuit.	AIO
8	ISOHm	Inverting, high-side isolated serial communication port. Refer to Section 4.2.3 Isolated Serial Peripheral Interface. Refer to Section 6.8 ISO lines circuit.	AIO
9	DGND	Digital ground. Connect to AGND on top.	G
10	GPIO1_ FAULTH	Digital input used for FAULTH receiver. Refer to Section 4.3 FAULT line.	DI
11	GPIO2_ FAULTL	Digital output used for FAULTL transmitter. Refer to Section 4.3 FAULT line.	DO
12	GPIO3	General-purpose I/O. Refer to Section 4.9 General purpose I/O: GPIOs. Generally used to sense NTCs. Refer to Section 6.9 NTC analog front end.	AI/DI/DO
13	GPIO4		AI/DI/DO
14	GPIO5		AI/DI/DO
15	GPIO6		AI/DI/DO
16	GPIO7_ WAKEUP	General-purpose I/O. Refer to Section 4.9 General purpose I/O: GPIOs. Generally used to sense NTCs. Refer to Section 6.9 NTC analog front end. Can be configured to act as wake up input. Refer to Section 4.9.4 GPIO7: wake up feature.	AI/DI/DO
17	NPNDRV	Internal voltage regulator controller output. Connect to the base of the external NPN transistor.	AO
18	VREG	Regulated analog power supply for core circuitry. Connect a tank capacitor as indicated in Table 73. It is disabled in low power modes (Silent Balancing, Sleep and during the OFF phase of Cyclic Wakeup). VCOM, VANA and VTREF regulators are fed by pre-regulated VREG.	P
19	VTREF	Buffered, precise analog reference voltage for driving multiple NTCs. Connect a tank capacitor as indicated in Table 73. It has a maximum IVTREF_ext current budget.	P
20	SPIEN	At first power up, after VCOM is out of undervoltage, this pin is sampled to determine port L configuration. Connect to VCOM to configure SPI mode. Connect to AGND to select isolated SPI communication. If left floating, this pin has a 100KΩ internal Pull down, forcing isolated SPI mode.	DI
21	VANA	Precise ADC analog supply. Connect a tank capacitor as indicated in Table 73.	P
22	AGND	Analog/ESD ground. Ground supply of chip.	G
23	ISENSEp	Non-inverting input of current measurement. Refer to Table 73.	AI
24	ISENSEm	Inverting input of current measurement. Refer to Table 73.	AI
25	GNDREF	Analog/reference GND. Connect to AGND on top	G
26	C0	Connect to the negative terminal of 1st cell.	AI
27	C1	Cell voltage input. Connect to the positive terminal of 1st cell.	AI
28	S1	Cell balancing FET control output for 1st cell.	AO
29	B2_1	Common terminal for cell balancing S1 and S2.	AO
30	S2	Cell balancing FET control output for 2nd cell.	AO
31	C2	Cell voltage input. Connect to the positive terminal of 2nd cell.	AI
32	C3	Cell voltage input. Connect to the positive terminal of 3rd cell.	AI
33	S3	Cell balancing FET control output for 3rd cell.	AO
34	B4_3	Common terminal for cell balancing S3 and S4.	AO
35	S4	Cell balancing FET control output for 4th cell.	AO

Pin #	Pin name	Description	I/O type(1)
36	C4	Cell voltage input. Connect to the positive terminal of 4th cell.	AI
37	C5	Cell voltage input. Connect to the positive terminal of 5th cell.	AI
38	S5	Cell balancing FET control output for 5th cell.	AO
39	B6_5	Common terminal for cell balancing S5 and S6.	AO
40	S6	Cell balancing FET control output for 6th cell.	AO
41	C6	Cell voltage input. Connect to the positive terminal of 6th cell.	AI
42	C7	Cell voltage input. Connect to the positive terminal of 7th cell.	AI
43	S7	Cell balancing FET control output for 7th cell.	AO
44	B8_7	Common terminal for cell balancing S7 and S8.	AO
45	S8	Cell balancing FET control output for 8th cell.	AO
46	C8	Cell voltage input. Connect to the positive terminal of 8th cell.	AI
47	C9	Cell voltage input. Connect to the positive terminal of 9th cell.	AI
48	S9	Cell balancing FET control output for 9th cell.	AO
49	B10_9	Common terminal for cell balancing S9 and S10.	AO
50	S10	Cell balancing FET control output for 10th cell.	AO
51	C10	Cell voltage input. Connect to the positive terminal of 10th cell.	AI
52	C11	Cell voltage input. Connect to the positive terminal of 11th cell.	AI
53	S11	Cell balancing FET control output for 11th cell.	AO
54	B12_11	Common terminal for cell balancing S11 and S12.	AO
55	S12	Cell balancing FET control output for 12th cell.	AO
56	C12	Cell voltage input. Connect to the positive terminal of 12th cell.	AI
57	C13	Cell voltage input. Connect to the positive terminal of 13th cell.	AI
58	S13	Cell balancing FET control output for 13th cell.	AO
59	B14_13	Common terminal for cell balancing S13 and S14.	AO
60	S14	Cell balancing FET control output for 14th cell.	AO
61	C14	Cell voltage input. Connect to the positive terminal of 14th cell.	AI
62	VBAT	Power supply of chip. This pin is also sensed by internal ADC through a voltage divider. Refer to Table 73.	P
63	CAP2	Pin2 external bootstrap capacitance. Refer to Table 73.	AI
64	CAP1	Pin1 external bootstrap capacitance. Refer to Table 73.	AI
-	GNDEP	Ground terminal, connect to AGND plane	G

1. *I/O type legend: AI = Analog Input; AO = Analog Output; AIO = Analog I/O; DI = Digital Input; DO = DigitalOutput; DIO = Digital I/O; P = Power; G = Ground; NC = Not Connect.*

3 Product electrical ratings

3.1 Operating range

Within the operating range the part operates as specified and without parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation, unless the AMR are exceeded.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

All voltages are related to the potential at substrate ground AGND, unless otherwise noted.

Table 2. Operating ranges

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VBAT	Global	Supply voltage	9.6		64	V
		Transient operation, 40 ms pulse, repetitive as per VDA320 E48-02 test.	64		70	V
VBAT, VREG, VCOM, VTREF		Supply voltage in case of transceiver use only (see Section 6.12 Transceiver mode)	4.6	5	5.4	V
C0	Global	Lower Cell Terminal Voltage	-0.3		0.3	V
B(n,n-1); Sn	Global	Cell Terminal Voltage	0		VBAT	V
C(n) for n=1 to 9	Global	Cell Terminal Voltage	0		VBAT – 4.5	V
C(n) for n=10 to 14	Global	Cell Terminal Voltage	3		VBAT + 0.3	V
C(n)-C(n-1) for n=1 to 14		Cell Terminal Differential Voltage	0		4.7	V
S(n+1)-B(n+1,n); B(n+1,n)-S(n) for n=1 to 13 odd		Cell Balance Terminal Differential Voltage	0		4.7	V
C(n)-S(n) for n=1 to 14		Cell Terminal Differential Voltage	0		4.7	V
VBAT – C(14)		Battery / high Terminal Differential Voltage	-0.3		61	V
ISOHP/M, ISOLP/M	Global		-0.3		VCOM	V
GPIOn	Local		-0.3		VCOM	V
SPIEN	Local		-0.3		VCOM	V
VTREF	Local			5		V
|ISENSEP – ISENSEM|	Local	CSA Input Differential Mode Range	-0.15		0.15	V
|ISENSEP + ISENSEM| / 2	Local	CSA Input Common Mode Range (Referenced to GNDREF)	-0.225		0.225	V
VCOM	Local			5		V
VANA	Local	Info only		3.3		V
VREG	Local			6.5		V
NPNDRV	Local		VREG-0.3		10	V
CAP1	Local		0		VBAT	V
CAP2	Local		VREG		VBAT + VREG	V

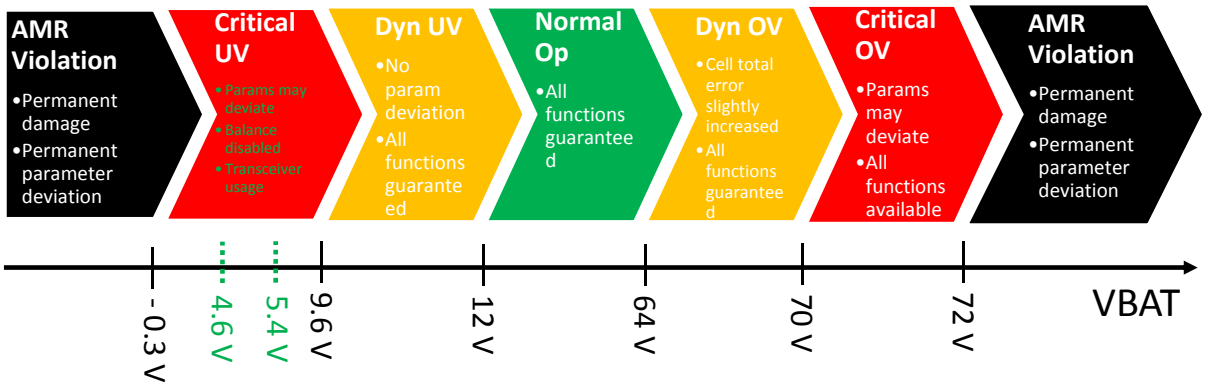
3.1.1 Supply voltage ranges

The device operates up to 14 cells of battery for hybrid and electric vehicles. The device can cover the voltage range of the main automotive Lithium batteries, up to a maximum of 4.6 V per cell in operating conditions. The IC has been engineered to sustain transient OV events as per LV 148

All operative ranges are listed in the picture below.

If the stand by V3V3 regulator goes in POR, the device is put in reset.

Figure 4. Device operation in the VBAT supply voltage ranges



3.2 Absolute maximum ratings

Exceeding any Absolute Maximum Rating (AMR) may cause permanent damage to the integrated circuit.

All voltages are related to the potential at substrate ground AGND.

Table 3. Absolute Maximum Rating

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VBAT, C14	-		-0.3	-	72	V
C0	-		-0.3	-	0.3	V
C(n); B(n,n-1); Sn	-		-0.3	-	72	V
C(n)-C(n-1) for n=1 to 14	-	In this range, the device is not damaged, but leakage from pins may exceed I_{CELL_LEAK} (see Table 39) if ADCs are enabled; it doesn't exceed if ADCs are disabled	-72	-	72	V
C(n)-C(n-1) for n=1 to 14	-	In this range, the leakage from pins I_{CELL_LEAK} is guaranteed (see Section 6.10.5 Busbar connection) if ADCs are enabled or disabled	-6	-	6	V
S(n+1)-B(n+1,n) B(n+1,n)-S(n) for n=1 to 13 odd	-		-0.3	-	V_{BAL_CLAMP}	V
C(n)-S(n) for n=1 to 14	-	Vreg < 2 V	-72	-	72	V
VBAT-C14	-		-72	-	72	V
ISOHP/M, ISOLP/M	-		-0.3	-	6	V
GPIOn	-		-0.3	-	5.5	V
SPIEN	-		-0.3	-	12	V
VTREF	-		-0.3	-	6	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ISENSEP/M	-		-0.3	-	4.5	V
VCOM	-		-0.3	-	6	V
VANA	-		-0.3	-	4.5	V
VREG	-		-0.3	-	12	V
NPNDRV	-		-0.3	-	12	V
CAP1	-		-0.3	-	VBAT + 0.3V	V
CAP2	-		VREG – 0.3V	-	VBAT + 7V	V
DGND, CGND	-		-0.3	-	+ 0.3	V
GNDREF shorted to AGND	-			-		

Table 4. ESD protection

Item	Parameter	Test conditions	Min.	Typ.	Max.	Unit
All pins Except Isolated Communication Terminals and Global pins(1)	-	HBM(2)	-2	-	2	kV
Isolated Communication Terminals(1)(2) and Global pins versus all GND+EP connected			-4	-	4	kV
All pins except Corner Pins	-	CDM(3)	-500	-	500	V
Corner Pins			-750	-	750	V
All pins	-	Latch up(4)	-100	-	100	mA

1. *Tested per AEC-Q100-002.*
2. *Isolated Communication Terminals: ISOHP, ISOHM, ISOLP_SDI, ISOLM_NCS.*
3. *Tested per AEC-Q100-011.*
4. *Tested per AEC-Q100-004, Class-2, Level-A.*

Pins are all GND connected together.

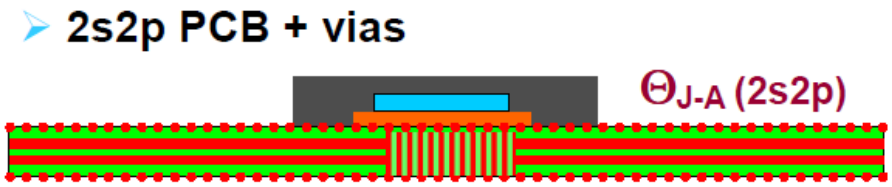
3.3 Temperature ranges and thermal data

Table 5. Temperature ranges and thermal data

Symbol	Parameter	Test conditions	Min	Max	Unit
T_{amb}	Operating and testing temperature (ECU environment)	-	-40	105	°C
T_J	Junction temperature for all parameters	-	-40	125	°C
T_{stg}	Storage temperature	-	-65	150	°C
T_{ot}	Thermal shut-down temperature (junction)	-	175	200	°C
T_{ot}	Temperature ADC accuracy	-	-10	+10	°C
O_{Thys}	Thermal shut-down temperature hysteresis	-	5	15	°C
$R_{Thj\text{-}amb}$	Thermal resistance junction-to-ambient(1)	-		22	°C/W

1. *In “2s2p”, the “s” suffix stands for “Signal” and the number before indicates how many PCB layers are dedicated to signal wires. The “p” suffix stands for “Power” and the number before indicates how many PCB layers are dedicated to power planes.*

Figure 5. **Sketch of a 2s2p PCB with thermal vias**



3.4 Power management

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Table 6. **Power Management**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{BAT_NORM}, Total Supply Current in Normal Mode from VBAT pin	-	Normal state (refer to Section 4.1 Device functional state); no load on VTREF; the chip performs continuously data transmission via isolated communication interfaces to higher and lower sides in a stack daisy chain. Application info: IBAT is not affected by communication. Current needed for COM interfaces is drawn out of VREG regulator.	1		2.5	mA
$I_{BAT\_NORM\_ADC}$, Total Supply Current in Normal Mode from VBAT pin	-	Normal state; No load on VTREF; no communication; The chip performs continuously sampling and converting.	5.5		9	mA
$I_{REG\_NORM\_CSEN1}$, Total Supply Current in Normal Mode from VREG MOS	-	Normal state; No load on VTREF; no communication; no ADC conversion; Curr sense. Enabled by coulombcounter_en = 1			21	mA
$I_{REG\_NORM\_CSEN0}$, Total Supply Current in Normal Mode from VREG MOS	-	Normal state; No load on VTREF; no communication; no ADC conversion; Curr sense Disabled by coulombcounter_en = 0			20	mA
$I_{REG\_NORM\_ADC\_CSEN1}$, Total Supply Current in Normal Mode from VREG MOS	-	Normal state; No load on VTREF; no communication; The chip performs continuously sampling and converting. Curr sense Enabled by coulombcounter_en = 1			38	mA
$I_{REG\_NORM\_ADC\_CSEN0}$, Total Supply Current in Normal Mode from VREG MOS	-	Normal state; No load on VTREF; no communication; The chip performs continuously sampling and converting. Curr sense Disabled by coulombcounter_en = 0			37	mA
$I_{REG\_NORM\_COMM}$, Additional supply current drawn from VREG for communication	-	Normal state; No load on VTREF; The chip performs continuously data transmission via isolated communication interfaces to higher and lower sides in a stack daisy chain. (measured with out_res_tx_isoh/l = 11, highest differential amplitude, highest consumption).	8	10.8	13	mA
I_{BAT_SLP}, Supply Current in Sleep Mode	-	Lowest power state; Both internal oscillator and external wakeup detection on.	10		50	µA
$I_{BAT\_SLP\_BAL\_CONF}$	-	Supply Current in Silent Balance Mode (enabled only regulators necessary to bias balance preregulators, refer to Section 4.1 Device functional state).	1.2	2	2.8	mA
$I_{BAT\_BALANCE}$	-	Delta current when the balancing of all 14 cells are activated.	0.4	0.55	0.7	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{REG\_GPIO\_DIGOUT}$	-	Delta current from VREG pin needed to use 1 GPIO as digital output.	0.4	0.8	1.2	mA

Average DC current consumption in application can be estimated according to the following equations:

Estimation of the average DC current consumption in application

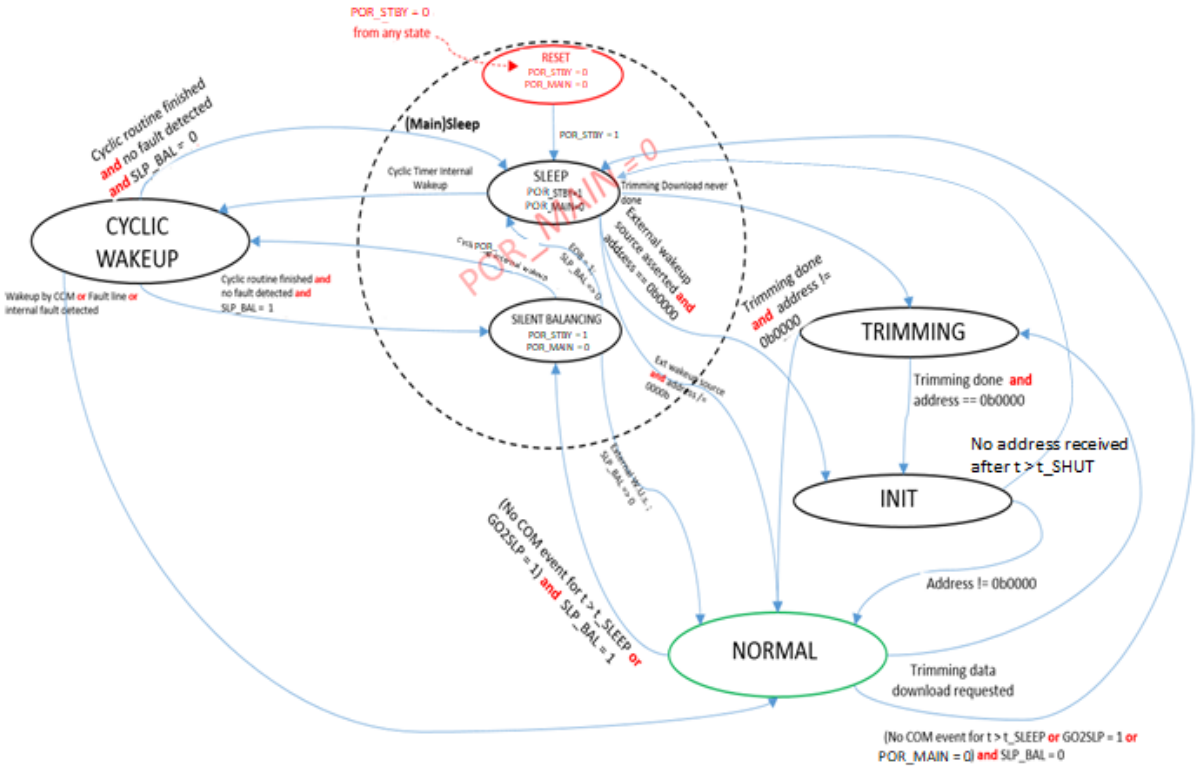
$$
\begin{cases}
I_{AVG} = \left(I_{BAT_{NORM_{ADC}}} + I_{REG_{NORM_{ADC}}} + \frac{N_{BAL}}{14} I_{BAT_{BALANCE}} + I_{REG_{GPIO_{DIGOUT}}} N_{DIGOUT}\right) \times W_{CONV} \\
+\left(I_{BAT_{NORM}} + I_{REG_{NORM}} + \frac{N_{BAL}}{14} * I_{BAT_{BALANCE}} + I_{REG_{GPIO_{DIGOUT}}} N_{DIGOUT}\right) \times W_{BAL\_OL} + I_{LP} \times W_{LP} \\
W_{CONV} = \frac{2T_{CYCLEADC_{SLEEP}}}{T_{PERIOD}} + \frac{T_{CYCLEADC_{000}}}{N_{CYCLE_{GPIO}} T_{PERIOD}} + \frac{T_{GPIO_{OPEN_{SET}}} + T_{CYCLEADC_{000}}}{N_{CYCLE_{GPIO_{TERM}}} T_{PERIOD}} \\
+\frac{2T_{Cx_{OPEN_{SET}}} + 2T_{CYCLEADC_{000}}}{N_{CYCLE_{CELL_{TERM}}} T_{PERIOD}} + \frac{3T_{CYCLEADC_{000}}}{N_{CYCLE_{HWSC}} T_{PERIOD}} \\
W_{BAL\_OL} = \frac{2T_{BAL_{OL}}}{N_{CYCLE_{BAL_{TERM}}} T_{CYCLE_{SLEEP}}} \\
W_{LP} = 1 - W_{CONV} - W_{BAL\_OL} \\
T_{PERIOD} = \begin{cases} T_{CYCLE\_SLEEP} \; if \; Cyclic \; Wakeup \; mode \; is \; activated \\ T_{CYCLE} \; if \; operating \; in \; Normal \; mode \end{cases} \\
I_{REG_{NORM_{ADC}}} = \begin{cases} I_{REG_{NORM_{ADCCSEN0}}} \; if \; CSA \; is \; disabled \\ I_{REG_{NORM_{ADCCSEN1}}} \; if \; CSA \; is \; enabled \end{cases} \\
I_{REG_{NORM}} = \begin{cases} I_{REG_{NORMCSEN0}} \; if \; CSA \; is \; disabled \\ I_{REG_{NORMCSEN1}} \; if \; CSA \; is \; enabled \end{cases} \\
I_{SLEEP} = \begin{cases} I_{BAT\_SLP} \; if \; N_{BAL} = 0 \\ I_{BAT\_SLP\_BAL\_CONF} \; if \; N_{BAL} > 0 \end{cases} \\
I_{LP} = \begin{cases} I_{SLEEP} + \frac{N_{BAL}}{14} \times I_{BAT_{BALANCE}} \; if \; Cyclic \; Wakeup \; mode \; is \; activated \\ I_{BAT\_NORM} + I_{REG_{NORM}} + \frac{N_{BAL}}{14} \times I_{BAT_{BALANCE}} + I_{REG_{GPIO_{DIGOUT}}} N_{DIGOUT} \; if \; operating \; in \; Normal \; mode \end{cases}
\end{cases}
\tag{1}
$$

4 Functional description

In the following paragraphs, the functionalities of the device are listed and described in detail.

4.1 Device functional state

Figure 6. **Device functional states**



4.1.1 Reset and Sleep states

Reset state: when stand-by logic is reset, all registers on device are reset. The battery voltage is still under threshold.

From here, as soon as the POR_STBY goes high the Stby Logic gets its supply power and the **Sleep** state is reached.

4.1.1.1 Operations in Reset state

No operation is possible in Reset state

Sleep state:

This state is reached:

- coming from **Reset** state on POR_STBY rising
- from other states in case a Go2SLP cmd is sent by uP or no communication is received for t > t_SLEEP
- from **Init** State in case the device address is still 0b0000 after t > t_SHUT
- from **Cyclic_Wup** state once the Cyclic Wup job is done and a silent balancing is not to be resumed.

In this state the device is sensitive to External Sources in order to wake up the Main Logic. External sources are: ISO lines, Fault line, SPI_CS (SPI_CLK) pins, also a GPIO pin for “Master” units.

In this state a slow oscillator is working allowing the device to wake itself up every t = t_{CYCLIC_SLEEP} + t_{CYCLIC_WUP} and move to **Cyclic Wup** state.

During **Sleep** state, the current consumption is significantly reduced to I_{SLEEP} current value: only the Communication wake up sources monitoring, low-speed oscillator for cyclic wake up timer, and the corresponding reference and power supply are activated.

Different events can cause a wake up, depending on the configuration decided by the microcontroller:

- **ISO COMM/SPI SIGNAL**: this wake-up during a regular SLEEP mode state moves the L9963E FSM to Init or Normal State. A proper signal will be detected as pre-wake up (simple edge readout), and later it must be followed by a wake-up signal that will be decoded by the L9963E which, in the meanwhile, has entered in a higher consumption mode (regulators turned ON, isolated RX/TX enabled). Any protocol frame recognized as electrically consistent will wake up the device. However, the command will not be interpreted and thus no execution takes place;
- **INTERNAL COUNTER**: it is possible that the microcontroller defines an automatic wake up of L9963E (when put in SLEEP mode) every T_{CYCLE_SLEEP}, in order to perform the diagnostics in the CYCLIC WAKEUP state;
- **GPIO SIGNAL**: in case GPIO7 is configured as wake up source (**GPIO7_WUP_EN = 1**), a high logic level on it will wake up L9963E;
- **FAULT**: in case a fault is detected in an upper L9963E, a proper signal is communicated through the FAULT line. The receiver connected to GPIO1/FAULTH pin will detect the event and the device will be forced to evolve into the normal state, in order to transmit the fault downward.

The wake-up event coming from external wake up sources is verified by the Stby logic (pattern confirmation step) before waking up the main logic (the main logic is kept under reset and its clock is gated off until the Sleep state is left).

The wakeup sequence lasts T_{WAKEUP}.

4.1.1.2 *Operations in Sleep state*

Only the Stand-by logic is working in Sleep state.

Table 7. Operations in Sleep state

Operation	Timing mode	Functions involved
Wake up Management	Always ON	Timers, Pin Input Buffer and ISO lines receiver ON. External sources activity detection, receivers and input buffers powered
Awakening Pattern Detection	Once	Comparison logic

4.1.2 Init state

In **Init** state, after having been woken up, the device waits for the uP to send the Address assignment command. Refer to Section 4.1.2.2 Addressing procedure.

If the address command is received before the Init timer expires (t_SHUT), the device address is stored into a stand-by logic register (**chip_ID**) and the device goes to **Normal** state.

The **chip_ID** field is then locked and no longer editable. Two actions can correctly re-initialize the device (including the **chip_ID**):

- Hard reset: (POR_STBY)
- Soft reset: it is recommended to set **SW_RST** and **GO2SLP** in the same frame
  - Note that Soft reset will leave communication timeout (**CommTimeout**) unmodified
  - Note that Soft reset will also clear the **chip_ID**
  - If only SW_RST is sent, the device will wait for CommTimeout and then move to Sleep state

If the Init timer (t_SHUT) expires before the command is received, the device goes back to **Sleep** state.

All references are powered, interfaces are ready data transmission. The commands sent by the micro-controller can be read from both ISO lines and SPI pins. However, while in Init state, only the **chip_ID**, **isotx_en_h** and **iso_freq_sel** fields are writable. It is not possible to write/read other registers.

Any failure is masked until the device receives an address.

4.1.2.1 *Operations in Init state*

Here below a list of operations the device can perform during Init State.

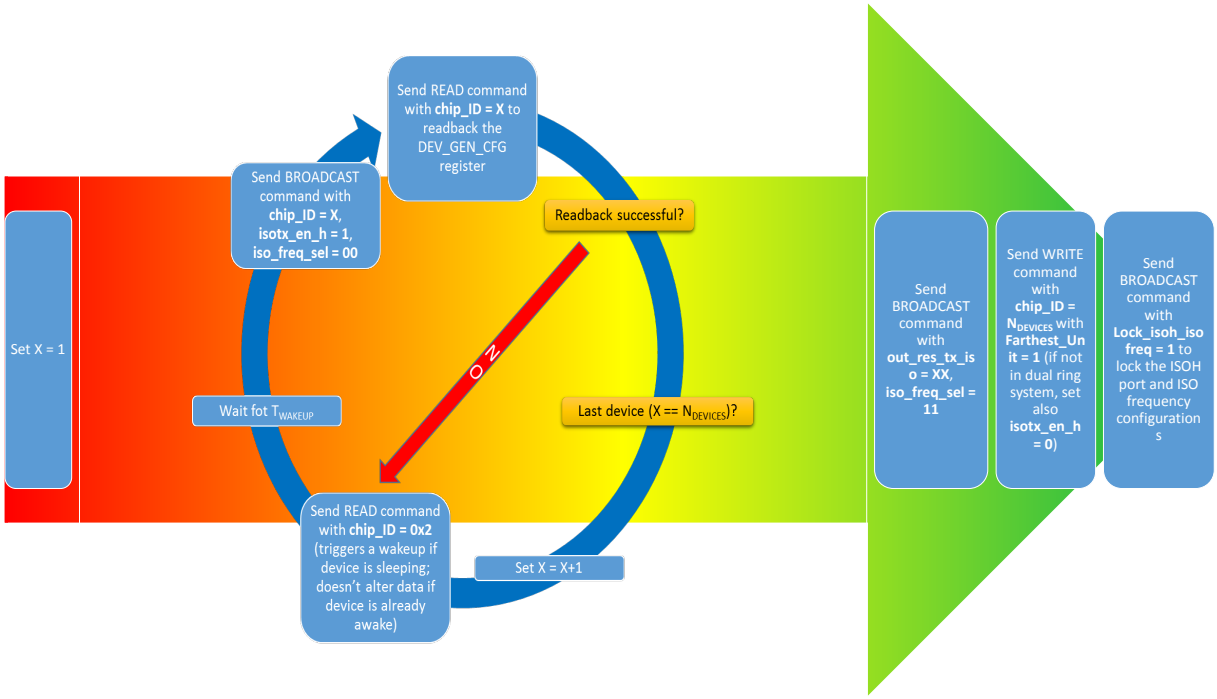
Table 8. Operations in Init state

Operation	Timing mode	Functions involved
Communication	Always ON	SPI/isolated SPI Logic and storage
Init Timeout	Always ON	t_SHUT timer

4.1.2.2 *Addressing procedure*

The following algorithm describes the correct daisy-chain addressing procedure for a stack of $N_{DEVICES}$:

Figure 7. Daisy chain addressing algorithm



Switching to high frequency (**iso_freq_sel = 11**) before initialization procedure has been completed is not recommended, since it might prevent other units from being initialized.

Once initialization procedure is done, it is possible to lock ISOH port status and ISO frequency configuration by setting **Lock_isoh_isofreq = 1**: the lock adds more safety against unwanted write access to **iso_freq_sel** and **isotx_en_h** bit in DEV_GEN_CFG register.

4.1.3 Normal state

All references are powered, and the **ADCs** and interfaces are ready for measurement and data transmission respectively. The commands sent by the micro-controller can be read from both ISO lines and SPI pins.

On receiving a valid command, the L9963E executes the corresponding operations, such as voltage, current and over-temperature measurement.

Some core safety operations (e.g. OV, UV, OT, UV, and VBAT monitoring) are checked in the background automatically.

In case the communication with MCU is missing for t > t_SLEEP (programmable via **CommTimeout**, maskable via **comm_timeout_dis**) or a GO2SLP command is received, the device moves either to **Sleep** state or to **Silent Balancing** state, depending on **slp_bal_conf** bit and balancing state.

A Soft RESET command received when in Normal state clears all registers except **CommTimeout**. The device is kept in Normal and doesn't move to Reset state.

4.1.4 Power up sequence

Final **Normal** state is reached through a power up sequence, which involves the turn ON of all regulators. The following power up sequence is performed correctly if VBAT pin voltage lays in the operating range (refer to Table 2):

- VREG is the first regulator to turn ON
- As soon as VREG reaches enough voltage dynamic (> 3 V), also VANA regulator starts to turn ON
- When VANA regulator voltage reaches V_{VANA_UV} threshold and related digital filter time T_{POR_FILT} + T_{VTREF_DELAY} expires, VTREF regulator is turned ON if VTREF_EN = 1. By default, VTREF is disabled and will not be turned on during first power up sequence.
- After T_{BOOT_DELAY} in respect to VTREF enable, Bootstrap circuit is enabled in charge phase (CAP2 connected to VREG, CAP1 to GND)
- After T_{VCOM_DELAY} in respect to VTREF enable, VCOM regulator is turned ON

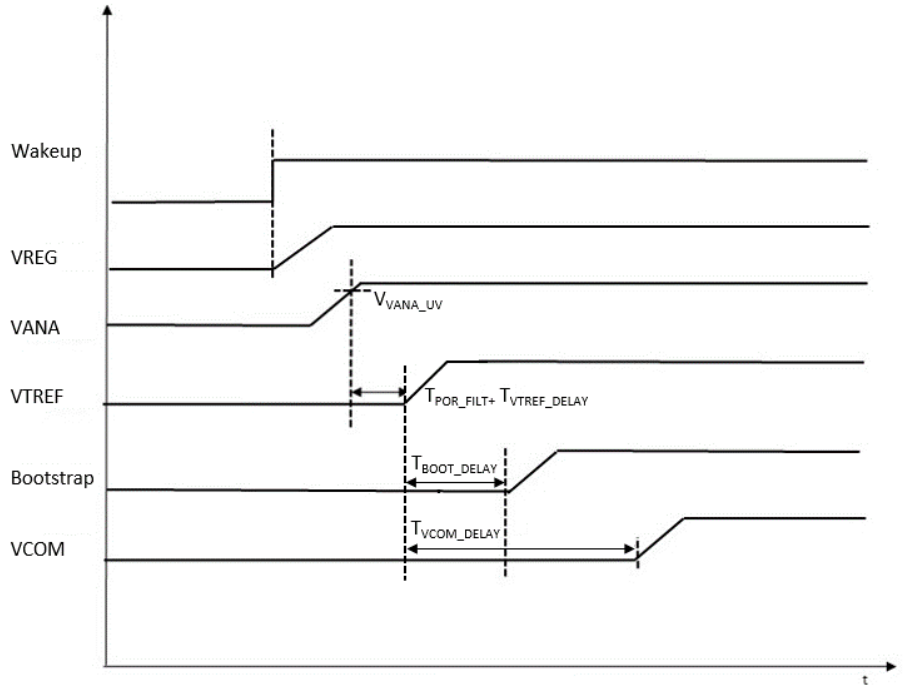
Normally, the power up sequence lasts T_{WAKEUP}. In case it lasts longer than a specific timeout, the device moves back to a low power state (Sleep or Silent Balancing, depending on the previous state). The following timeouts are implemented:

- timeout_VCOM_UP_first, valid only for the first power up
- timeout_VCOM_UP, valid for each wake up
- timeout_OSCI_MAIN, valid for each wake up

During power down:

- VCOM, VTREF and Bootstrap are turned off at the same time
- VREG is turned off after T_{VREG_OFF}
- When VREG falls below 4 V (typical value), VANA starts falling along with VREG.

Figure 8. Power up Sequence



The device is still able to communicate if VTREF and Bootstrap power up fails: VCOM regulator is started anyway. It is not recommended to send any SPI frame to the device before T_{WAKEUP} expires. Any incoming frame while L9963E is still performing the power up routine might be discarded.

4.1.5 Silent Balancing state

There is the possibility to perform the balancing of one (or more) cells with a reduced current consumption with respect to doing that in **Normal** mode: this state is called **Silent Balancing**.

In **Silent_Bal** the same resources as in **Sleep** state are active, in addition to the balance predrivers and the necessary bias circuitry.

To enter in **Silent Balancing** state from **Normal** state, the following conditions shall be verified:

1. Cell balancing must be ON
2. The **slp_bal_conf** flag shall be set to '1'
3. A "go to sleep" condition shall be verified (either an explicit GO2SLP command or communication timeout expiration)

If a cell balancing is previously demanded in **Normal** mode and the **slp_bal_conf** flag is set to 1, when a condition to go to sleep (low consumption) occurs the device enters **Silent Balancing**, not Sleep state and the required cell-balancing starts (or continues).

3 possible leaving ways from **Silent Balancing** mode:

- any wake up signal on communication or **FAULT Line** can force the chip to stop the balancing and then go back to the **Normal** state. Any protocol frame recognized as electrically consistent will wake up the device. However, the command will not be interpreted and thus no execution takes place.
- an external Fault must bring the device to Normal state and stop the balancing.
- as soon as the required balancing target is finished, the EOB (End of Balancing) bit is set to one and the chip enters the **Sleep** state.

If the Cyclic signal is raised the device goes to **Cyclic_Wup** state, runs the diagnosis then it goes back to **Silent Balancing** (if **slp_bal_conf** flag = 1) where the balancing resumes.

4.1.5.1 Operations in Silent Balancing state

Here below a list of operations the device can perform during Silent Balancing state.

Table 9. Operations in Silent Balancing state

Operation	Timing mode	Functions involved
Balancing low power	Always ON	Balancing timer, Drivers ON, Balance short comparators
Wakeup management	Always ON	Wakeup logic and wakeup sources interfaces ON

4.1.6 Cyclic wake up state

From both Sleep and Silent Balancing states, the device moves periodically (once every t_{CYCLIC_SLEEP}) to Cyclic_Wup state in order to perform a fault monitoring.

Diagnostic checks are done in this state as well as always-on monitorings. ADC must be ON to check possible critical battery conditions. Any detected fault moves the device to the Normal state.

An "On-demand" operation is only possible once the device has moved to Normal in case of any detected fault

Possible ways to leave this state:

- Any fault detected during this mode moves the device to the Normal state.
- A wake up from Fault line or Comm lines moves the device to the Normal state. Any protocol frame recognized as electrically consistent will wakeup the device. However, the command will not be interpreted and thus no execution takes place
- If the defined monitoring tasks are finished, the device can move to the SLEEP or SILENT BALANCING states automatically based on the state before **Cyclic Conversions** (**slp_bal_conf** flag).

4.1.6.1 Operations in Cyclic wake up state

Here below a list of operations the device can perform during Cyclic wake up state.

Table 10. Operations in Cyclic Wakeup state

Operation	Timing mode	Functions involved
Battery fast OV/UV	Always ON	Threshold Comparator
Battery OV/UV	Once	ADCV measurements vs. threshold
Cells OV/UV	Once	ADCV measurements vs. threshold
GPIO OT/UT	Once	ADCV measurements vs. threshold
OC Monitor	Always ON	ADCC measurements vs. threshold
OT Monitor	Always ON	ADCT measurements vs. threshold
GPO Short Detection	Always ON	Logical Comparison
Clock Monitor	Always ON	Frequency comparison to secondaty monitor
Downward Fault Signalling	Always	Receivers and Transmitters
Cell Open	Once	ADCV measurements vs. threshold
Balancing Open	Once	Voltage Comparator, Timer
Wake up Management	Always ON	Wake up logic and wakeup sources interfaces ON

Cyclic operations have their own periods written by MCU in specific SPI registers.

In case the “On-demand” and “cyclic” timing modes are both possible, an “on-demand” command starts a single operation immediately, breaking the cyclic period, and resets the cyclic counter.

In GPIO short detection the detection is guaranteed only in the duty phase, if the pin is configured as an output.

4.1.7 Sleep parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Table 11. Sleep parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{GPIO7_WAKEUP}	GPIO7 deglitch filter when used as Wakeup Source	Tested by SCAN		150		µs
$T_{UV\_SHORT\_DELAY}$	Delay after POR. Used to latch VCOM_UV and VTREF_UV	Tested by SCAN		40		µs
T_{WAKEUP}	Time necessary to complete Wake up from SLEEP mode (between Wake up source and VCOM out of UV condition)				2	ms
t_SHUT		Tested by SCAN		60		s
t_SLEEP_00	Communication Timeout CommTimeout = 00	Tested by SCAN		32		ms
t_SLEEP_01	Communication Timeout CommTimeout = 01	Tested by SCAN		256		ms
t_SLEEP_10	Communication Timeout CommTimeout = 10	Tested by SCAN		1024		ms
t_SLEEP_11	Communication Timeout CommTimeout = 11	Tested by SCAN		2048		ms
$t_{CYCLIC\_SLEEP\_000}$		Tested by SCAN		100		ms
$t_{CYCLIC\_SLEEP\_001}$		Tested by SCAN		200		ms
$t_{CYCLIC\_SLEEP\_010}$		Tested by SCAN		400		ms

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{CYCLIC\_SLEEP\_011}$		Tested by SCAN		800		ms
$t_{CYCLIC\_SLEEP\_100}$		Tested by SCAN		1600		ms
$t_{CYCLIC\_SLEEP\_101}$		Tested by SCAN		3200		ms
$t_{CYCLIC\_SLEEP\_110}$		Tested by SCAN		6400		Ms
$t_{CYCLIC\_SLEEP\_111}$		Tested by SCAN		12800		Ms
T_{VREG_OFF}		Tested by SCAN		500		µs
FMAIN_OSC_stby	Internal standby Oscillator frequency		20	32	45	KHz
FAUX_OSC_stby	Internal standby redundant Oscillator frequency		20	32	45	KHz
timeout_VCOM_UP_first	Timeout at first power up. From wakeup event to VCOM_UV release	Tested by SCAN		8		ms
timeout_VCOM_UP	Default power up timeout. From wakeup event to VCOM_UV release	Tested by SCAN		4		ms
timeout_OSCI_MAIN	From wakeup event to main oscillator stable	Tested by SCAN		10		ms
timeout_POR_MAIN	VANA settling time timeout	Tested by SCAN		1.5		ms
T_{BOOT_DELAY}	Delay between VTREF enable and Bootstrap enable	Tested by SCAN		200		µs
T_{VTREF_DELAY}	Delay between VANA_UV release (POR_STBY asserted after T_{POR_FILT}) and VTREF enable	Tested by SCAN		630		µs
T_{VCOM_DELAY}	Delay between VTREF enable and VCOM enable	Tested by SCAN		400		µs
$T_{WAKEUP\_TIMEOUT\_ISO}$	Timeout of the pulse counter for wakeup detection (isolated SPI)	Tested by SCAN	282			µs
$T_{WAKEUP\_TIMEOUT\_SPI}$	Timeout of the pulse counter for wakeup detection (SPI)	Tested by SCAN	84		138	µs
$T_{WAKEUP\_NCS\_HIGH}$	Minimum NCS high time before sending SPI wake up frame	Tested by SCAN	400			µs

4.2 Serial communication interface

Two types of serial communication ports are included in L9963E: SPI and isolated interface:

- SPI can be used for the local communication between MCU and the closest L9963E
- Isolated SPI can be used for the global communication between several L9963E stacked in a daisy chain

Refer to Section 6.11 Communication architectures for all the different application scenarios.

The frequencies on the 2 communication interfaces are different and not related.

From micro-controller point of view a daisy chain of many L9963E devices is controlled as a single device addressable by using both the device ID and the device's internal register addresses.

4.2.1 Communication interface selection

Two communication ports are available:

- **Port H**: implemented via the ISOHp and ISOHm pins. It always works as Isolated SPI interface. It can be enabled by setting **isotx_en_h = 1**
- **Port L**: implemented via the ISOLp_SDI, ISOLm_NCS, GPIO8_SCK, GPIO9_SDO pins. It is always enabled and its configuration is latched upon first powe up and depends on the **SPIEN** pin

Table 12. **Port L configuration determination**

Electrical condition	Latched when	Configuration	Wake up source
SPIEN = 1	Upon VCOM_UV release	Port L configured as SPI. Master Unit. SPIEN must be connected to VCOM	SPI wake up logic
SPIEN = 0 (default condition if pin is left floating)	Upon VCOM_UV release	Port L configured as isolated SPI. Slave Unit. SPIEN must be connected to AGND	ISOL wake up comparator

In case the first power up fails and L9963E comes back to Sleep state without having latched the PORT L operating mode, both wake up sources will be kept active in order to allow subsequent power up trigger in both operating configurations.

When the first power up completes successfully, only the wake up source related to the units with **SPIEN = 1** is **Master** units of the daisy chain. A **Master** Unit differs from the **Slave** one (**SPIEN = 0**) because:

- It manages the asynchronicity between SPI CLK and the programmable bit-rate on the isolated line;
- It exploits an internal buffer to store answers received from the slaves on ISOH port;
- It implements timeout mechanisms and frame error checks described in Section 4.2.4.4 Special frames;
- It forwards commands only if they are addressing Slave units. Any command addressed to the Master unit is not propagated on the ISOH port;
- In case Master Unit has port H disabled (**isotx_en_h = 0**), trying to communicate with a Slave unit will return the corresponding Master's register content;

Interaction between **Port H** and **Port L** is managed by L9963E. The IC is capable of converting analog signals incoming on the isolated twisted pair to digital signals suitable for SPI, and viceversa. Passing a signal through a single unit takes a single pulse period ($2*T_{BIT\_HIGH\_LOW\_FAST}$ or $2*T_{BIT\_HIGH\_LOW\_SLOW}$, depending on the programmed operating frequency), which can be used to account for the insertion delay of an L9963E in the daisy chain.

4.2.1.1 *Wake up via communications interface*

To wake up the device from low power modes, any communication frame in low frequency (F_{ISO_SLOW}) can be sent:

- If port L is configured in SPI mode, a sequence of at least 37 clock pulses on SCK line with active low chip select NCS will wake up the device. Pulses must be received within $T_{WAKEUP\_TIMEOUT\_SPI}$ timeout starting from the NCS assertion. Before sending the wake up frame, NCS must have been set high for at least $T_{WAKEUP\_NCS\_HIGH}$.
- If port L is configured in isolated SPI mode, a sequence of at least 37 differential pulses on ISOLP/ISOLM pins, whose minimum duration is $T_{DET\_MIN\_WU}$ and whose amplitude is greater than **Wakeup_thr** will wake up the device. Pulses must be received within $T_{WAKEUP\_TIMEOUT\_ISO}$ timeout starting from the first valid pulse.
- If port H is enabled, a sequence of at least 37 differential pulses, whose minimum duration is $T_{DET\_MIN\_WU}$ and whose amplitude is greater than **Wakeup_thr** will wake up the device. Pulses must be received within $T_{WAKEUP\_TIMEOUT\_ISO}$ timeout starting from the first valid pulse.

Note: Depending on pulses re-synchronization uncertainty with the internal standby oscillator, the wake up event may occur even if COM pulses are less than 37 (min. number of pulses in the best case is 8). However, 37 pulses will always guarantee a correct wake up.

In case the first power up fails and SPIEN value is not correctly latched, port L will listen to both wake up sources, until a correct power up sequence is achieved and port L configuration is determined.

4.2.2 Serial Peripheral Interface (SPI)

The SPI pinout is listed in the following table:

Table 13. **L9963E pin used as SPI**

L9963E pin	SPI function	Configuration
ISOLp_SDI	Serial Data Input (SDI)	Digital input

L9963E pin	SPI function	Configuration
ISOLm_NCS	Chip Select (CS)	Digital input. Active low.
GPIO8_SCK	Serial Clock (SCK)	Digital input.
GPIO9_SDO	Serial Data Out (SDO)	Digital output

A 40-bit frame is used including a 6-bit CRC.

Refer to Section 4.2.4 SPI protocol details for further details about the protocol.

Table 14. SPI interface quick look

Parameter	Description
Protocol	Out of frame
Single Frame Length	40 bit
Addressable Devices	15
Frame protection	6 bit CRC
Max. Frequency	5 MHz
CPOL	0
CPHA	0
Master/Slave configuration	MCU Master / L9963E Slave

4.2.3 Isolated Serial Peripheral Interface

The Isolated SPI interface allows units with different ground levels and on different boards to communicate with each other. Physically the interface is based on a twisted-pair wire with transformer isolators.

The isolated SPI pinout is listed in the following table:

Table 15. Isolated SPI pinout

Pin	SPI Function	Configuration
ISOLp_SDI	Port L positive differential input/output	Analog input/output
ISOLm_NCS	Port L negative differential input/output	Analog input/output
ISOHp	Port H positive differential input/output	Analog input/output
ISOHm	Port H negative differential input/output	Analog input/output

Figure 9. **Isolated SPI interface**

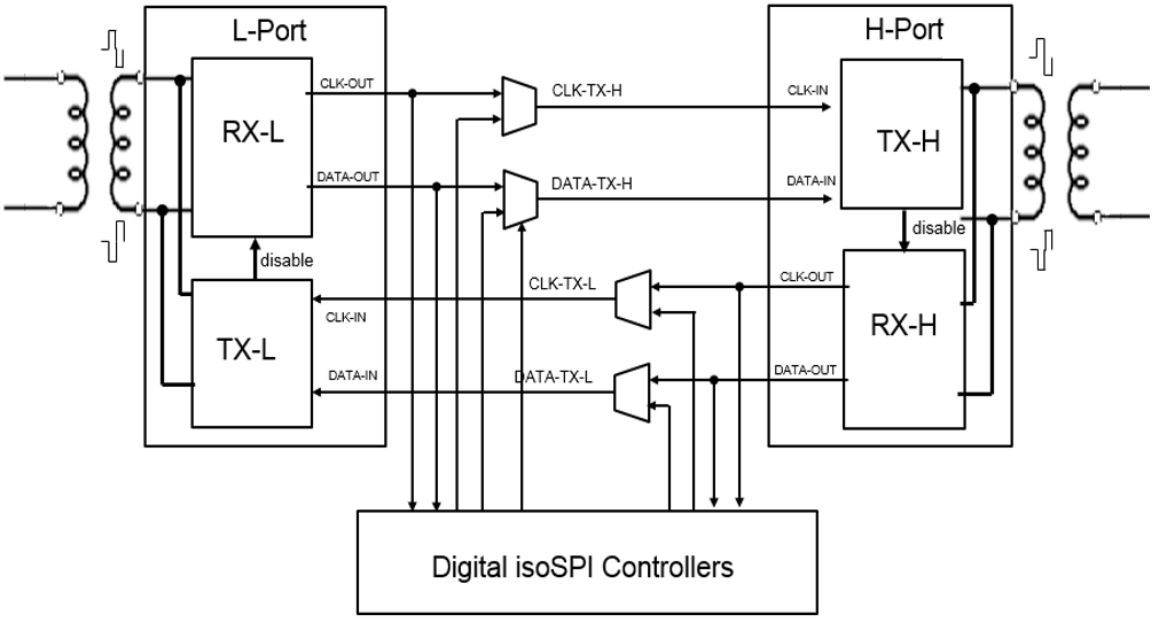


Table 16. **Isolated SPI quick look**

Parameter	Description
Protocol	Half-Duplex / Out of frame
Single Frame Length	40 bit
Addressable Devices	31
Frame protection	6 bit CRC
Max. Bit-rate	2.66 Mbps (high speed configuration)
	333 kbps (low speed configuration, default)
Master/Slave configuration	L9963E Slave

The transmission line on the isolated SPI exploits a single twisted pair. Communication data is transmitted/ received over a pulse-shaped signal, in a half-duplex protocol.

Line bit-rate can be selected by programming the **iso_freq_sel** bit via SPI. A single bit is made of a pulse time (T_{PULSE}) followed by two pause slices ($2T_{PULSE}$).:

- $T_{PULSE} = 2T_{BIT\_HIGH\_LOW\_FAST}$ for the high speed configuration
- $T_{PULSE} = 2T_{BIT\_HIGH\_LOW\_SLOW}$ for the low speed configuration

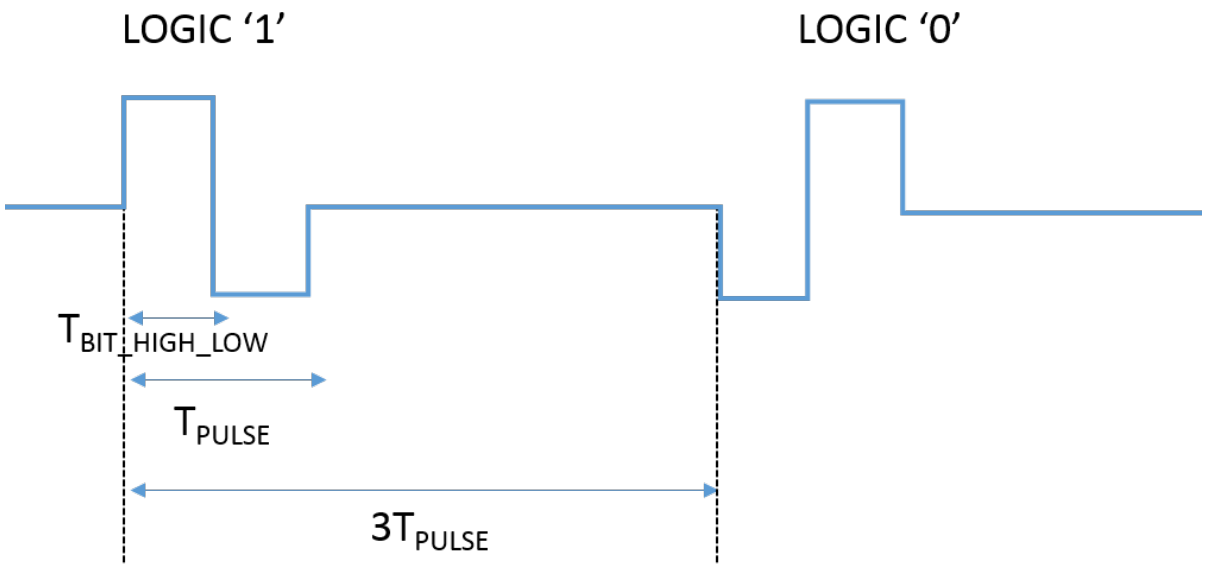
Once the operating frequency has been programmed and the ISOH port has been enabled/disabled, it is possible to lock these settings by writing the **Lock_isoh_isofreq** bit to ‘1’, to avoid unwanted changes due to wrong MCU write frame.

Lock_isoh_isofreq is added to the reg map into a separate register in respect to **isotx_en_h** and **iso_freq_sel**, in order to avoid that a single frame can both unlock and write fields

Lock_isoh_isofreq bit (default 0) is reset every time the device goes to a low power mode. When **Lock_isoh_isofreq** is set to ‘1’, **isotx_en_h** and **iso_freq_sel** bits are write protected

Architecture and MCU command’s time constraints are specified taking into account signal propagation delay over the communication bus. Refer to Inter-frame delay for further details.

Figure 10. **Isolated SPI pulse shape and logical meaning**



4.2.3.1 *ISO communicator receiver and transmitter*

An isolated receiver and transmitter are connected to the couple of pins ISOLP/M and ISOHP/M. Depending on the communication phase, they can be enabled or disabled.

4.2.3.1.1 ISO communicator receiver

The receiver is able to convert a differential input signal into a single ended signal that is provided to the logic.

In order to guarantee a correct communication and guarantee **Wake up via Communication Interface** the input common mode must be included into range $V_{CM\_ISO\_IN}$.

At power up by default the device is configured for a low frequency communication (F_{ISO_SLOW}); higher frequency F_{ISO_FAST} can be configured by acting on the **iso_freq_sel** bit.

4.2.3.1.2 ISO communicator transmitter

The transmitter is able to force as differential output the single ended signal that is provided by the logic.

Transmitter output impedance can be programmed via **out_res_tx_iso** ($R_{DIFF\_ISO\_OUT1...3}$), as described in Table 18. It affects differential pulse amplitude. In order to guarantee a correct communication in case of high frequency configuration the bit length must be at least $T_{BIT\_LENGTH\_FAST}$ and the duration of high and low level of a single bit into a period $T_{BIT\_LENGTH\_FAST}$ must be $T_{BIT\_HIGH\_LOW\_FAST}$.

In case of low frequency configuration $T_{BIT\_LENGTH\_SLOW}$ and $T_{BIT\_HIGH\_LOW\_SLOW}$ are valid.

4.2.3.2 *Dual access ring*

L9963E supports dual access ring topology (refer to Section 6.11.3 Dual access ring for the application scenario). The device accepts commands from both ports (ISOL/SPI and ISOH ports) and generates answers in both directions.

This kind of functionality is present by default and cannot be disabled.

In the typical application scenario featuring a number of $N_{DEVICES}$ L9963E, two of them are configured as SPI devices (referred to as bottom and top Masters), while the remaining is configured as isolated SPI slaves (refer to Section 4.2.1 Communication interface selection for Master and Slave behavior).

Referring to Figure 51, the Section 4.1.2.2 Addressing procedure follows the standard approach, except for the top Master, that must be initialized through its own SPI interface.

Once the initialization is complete, MCU is able to communicate with any Slave through any of the 2 Masters SPI interface. It is also possible to verify the loop integrity, accessing one Master through the opposite one.

In case the access to a Slave is performed exploiting the bottom Master, the corresponding answer must be retrieved through the bottom Master itself (the same applies for the dual case of the top Master).

4.2.3.3 *Electrical parameters*

4.2.3.3.1 Receiver

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT <64 V; -40 °C < Tambient < 105 °C

Table 17. Isolated receiver electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DIFF\_ISO\_IN3}$	Differential input voltage threshold	|V(ISOP) – V(ISOM)|	100	250	400	mV
$V_{CM\_ISO\_IN}$	Input voltage common mode range	|V(ISOP) + V(ISOM)| /2 Design info	0		1.9	V
R_{ISO_DIFF}	Differential input resistance	VIF enabled, no communication Resistance measured between ISOP and ISOM pins	5		15	kΩ
R_{ISO_EXT}	External termination resistance connected between ISOxP and ISOxM pins	Info only, not tested		120		Ω
I_{ISO_LEAK}	ISO input leakage current	0 V < ISOHP/M, ISOLP/M < VCOM			5	µA
$T_{DET\_MIN\_WU}$	Minimum pulse duration to be detected	Application info	400			ns
Wakeup_thr	Wake up comparator threshold		80	200	320	mV

4.2.3.3.2 Transmitter

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Table 18. Isolated transmitter electrical parameters

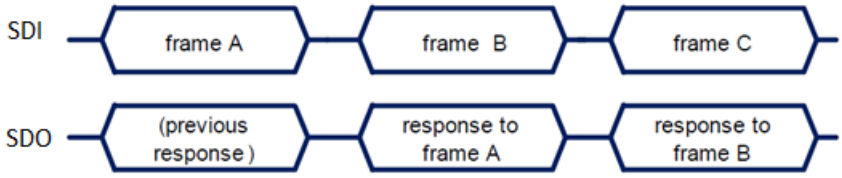
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DIFF\_ISO\_OUT1}$	Total output resistance: sum of pullup and pulldown resistance contribution	R_{pullup} measured with V(ISOHL/MP) = 1.5 V $R_{pulldown}$ measured with V(ISOHL/MP) = 0.9 V (out_res_tx_iso = 00, default)	310	440	570	Ω
$R_{DIFF\_ISO\_OUT2}$		(out_res_tx_iso = 01)	220	314	410	Ω
$R_{DIFF\_ISO\_OUT3}$		(out_res_tx_iso = 11)	170	244	310	Ω
$V_{CM\_ISO\_OUT}$	Output voltage common mode	|V(ISOP) + V(ISOM)|/2	1		1.4	V
$T_{BIT\_HIGH\_LOW\_FAST}$	High/low level bit duration into a whole period in case of high frequency configuration	Application info iso_freq_sel = 11		62.5		ns
$T_{BIT\_HIGH\_LOW\_SLOW}$	High/low level bit duration into a whole period in case of low frequency configuration	Application info iso_freq_sel = 00		500		ns
$T_{BIT\_LENGTH\_FAST}$	Bit duration with high frequency configured	Guarantee by SCAN iso_freq_sel = 11		375		ns
$T_{BIT\_LENGTH\_SLOW}$	Bit duration with low frequency configured	Guarantee by SCAN iso_freq_sel = 00		3		µs
F_{ISO_FAST}	Isolated Communication Rate	High frequency communication Application info		2.66		Mbps

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		For terminals ISOHP/M, and ISOLP/M iso_freq_sel = 11				
F_{ISO_SLOW}	Isolated Communication Rate	Low frequency communication Application info For terminals ISOHP/M, and ISOLP/M iso_freq_sel = 00		333.3		Kbps
$T_{ANSWER\_DELAY\_FAST}$	Delay between receival of a command and generation of the answer	High speed mode Guarantee by SCAN iso_freq_sel = 11		4.5		µs
TANSWER_DELAY_SLOW	Delay between receival of a command and generation of the answer	Low speed mode Guarantee by SCAN iso_freq_sel = 00		9		µs

4.2.4 SPI protocol details

The protocol is **out-of-frame** in order to manage the propagation delay of the commands sent by MCU and the answers generated by the L9963E stacked in the vertical interface. A command sent at the N-th frame will receive its feedback at the (N+1)th frame.

Figure 11. Out of frame protocol description



MCU can access the devices in different ways.

4.2.4.1 *Single access*

The single access behavior is based on a Write and Read approach.

The execution of each WRITE command sent by MCU can be immediately verified by interpreting the answer incoming from the addressed device. Any reply is buffered into L9963E Master unit, which passes it to the MCU on its next command.

Figure 12. Write and read access

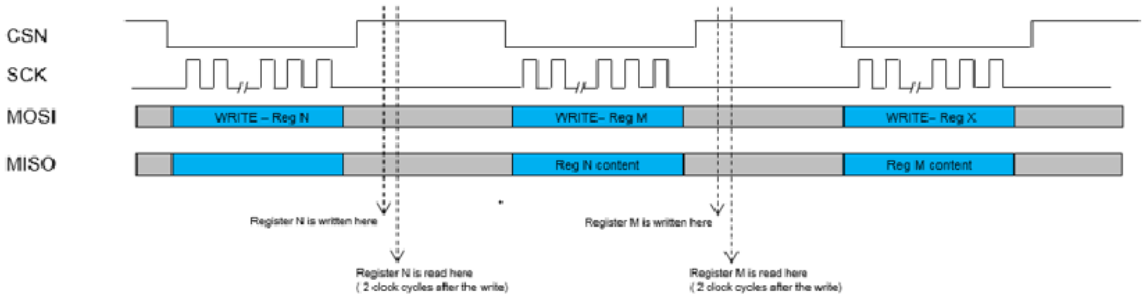
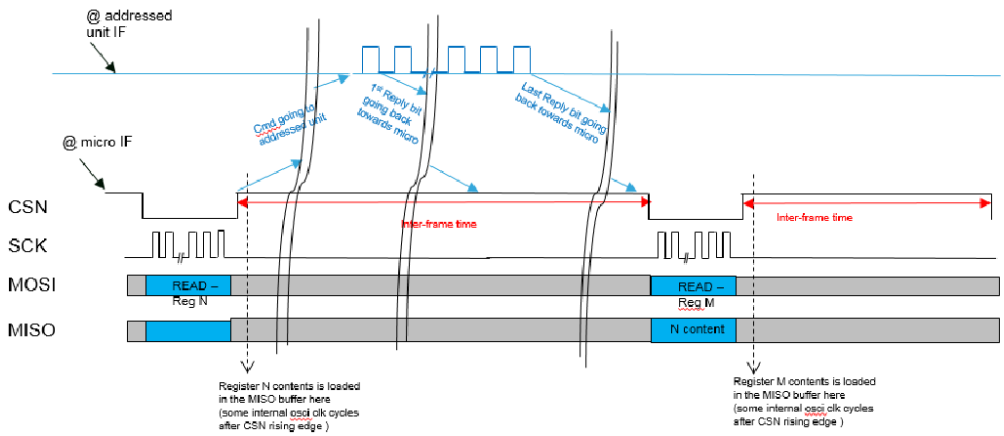


Table 19. SPI protocol: single access addressed frame (write and read)

	39	38	37 36 35 34 33	32 31 30 29 28 27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
MOSI	P.A.=1	R/W	Dev ID	Address	GSW	DATA WRITE	CRC
MISO	P.A.=0	Burst = 0	Dev ID	Address feedback	GSW	DATA READ	CRC

READ commands require the same inter-frame time as the WRITE ones. Any reply is buffered into L9963E Master unit, which passes it to the MCU on its next command.

Figure 13. **Single read access**



Frame fields are described in the table below:

Table 20. **Single access frames field description**

Field	Length	Value	Description
P.A.	1 bit	0	Answer sent by any Slave unit (MISO)
		1	Command sent by Master unit (MOSI)
R/W	1 bit	0	Read
		1	Write
Dev ID	5 bit	From 0x1 to 0x1F	Identifies the x-th L9963E unit in a daisy chain
Address	7 bit	From 0x00 to 0x5F	Identifies the y-th register of the device
Address feedback			
GSW	2 bit	From 0x0 to 0x3	Refer to Section 4.2.4.5 Global Status Word (GSW)
DATA WRITE	18 bit	Depends on the register	Data to be written in the y-th register of the x-th device. It is discarded in case of READ command.
CRC	6 bit	From 0x00 to 0x3F	CRC calculated on the [39-7] field of the frame. Refer to Section 4.2.4.6 CRC calculation
Burst	1 bit	0	Answer to a single access command
DATA READ	18 bit	Depends on the register	Answer containing the data read from the y-th register of the y-th device

4.2.4.2 *Burst access*

The Burst Access supports only READ commands. It can be used to reduce the time needed to readout long data series from a single unit. The addressed unit receives the Burst command and starts replying the requested data frame by frame towards the MCU. Any reply is buffered into L9963E Master unit, which passes it to the MCU on its next command.

Figure 14. Burst access

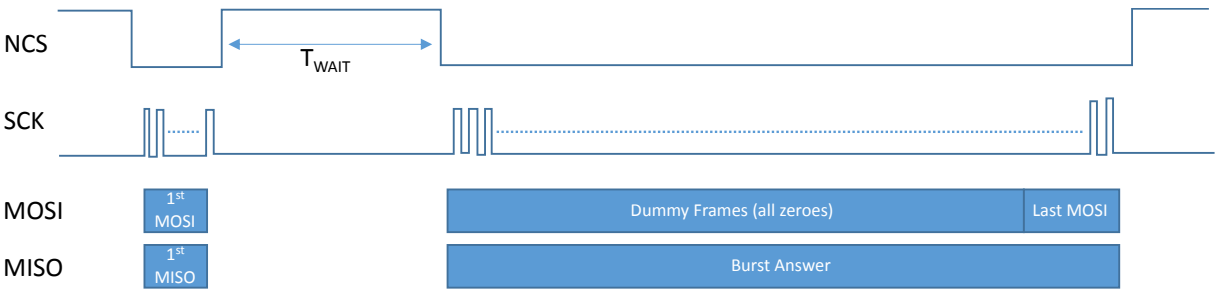


Table 21 describes the burst frame sequence.

- In case L9963E is configured in SPI mode, its internal buffer will store answers incoming from upper units. Apply the following strategy to download the burst data:
  - First frame (sent with a single NCS window as a normal command)
    - First MOSI contains the corresponding Burst command (see Table 23 for available commands)
    - First MISO stores the answer to the previous MCU command, as per out-of-frame behavior
  - Wait for burst answer to come back to the Master unit
    - 400 µs (in case iso_freq_sel = 11)
    - 3 ms (in case iso_freq_sel = 00)
  - Intermediate frames (all downloaded keeping NCS low)
    - Intermediate MOSI can be dummy commands (e.g. all zeroes). They are not interpreted by the L9963E SPI logic
    - Intermediate MISO contain burst data formatted as in Table 21
  - Last frame (attached to intermediate frames, keeping NCS low)
    - Last MOSI must be a valid command, because it will be interpreted by L9963E SPI logic
    - Last MISO contains last burst data register (MISOn) as shown in Table 21
- In case L9963E transceiver is interposed between MCU and L9963E, refer to the L9963T datasheet. The Application Information section hosts a paragraph explaining how to handle burst commands.

Table 21. SPI protocol: answer to a burst read request

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	P.A.=1	R/W=0	Dev ID					Command							GSW		Unused (Any Data Is Possible)																						CRC		
MISO1	P.A.=0	Burst = 1	Dev ID					Command feedback							GSW		DATA READ																						CRC		
MISO2	P.A.=0	Burst = 1	Dev ID					1	1	Frame Num (00010)					GSW		DATA READ																						CRC		

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO3	P.A.=0	Burst = 1	Dev ID					1	1	Frame Num (00011)					GSW		DATA READ																					CRC			
MISO4	P.A.=0	Burst = 1	Dev ID					1	1	Frame Num ….					GSW		DATA READ																					CRC			
MISOn	P.A.=0	Burst = 1	Dev ID					1	1	Frame Num ….					GSW		DATA READ																					CRC			
MISO20	P.A.=0	Burst = 1	Dev ID					1	1	Frame Num (10011)					GSW		DATA READ																					CRC			

Frame fields related to the burst access are described in the table below:

Table 22. Burst access special frame fields

Field	Length	Value	Description
P.A.	1 bit	0	Answer sent by any Slave unit (MISO)
		1	Command sent by Master unit (MOSI)
R/W	1 bit	0	Read
		1	Write
Dev ID	5 bit	From 0x1 to 0x1F	Identifies the x-th L9963E unit in a daisy chain
Command	7 bit	From 0x78 to 0x7D	Identifies a set of registers to be read out of the device
Command feedback			
GSW	2 bit	From 0x0 to 0x3	Refer to Section 4.2.4.5 Global Status Word (GSW)
CRC	6 bit	From 0x00 to 0x3F	CRC calculated on the [39-7] field of the frame. Refer to Section 4.2.4.6 CRC calculation
Burst	1 bit	1	Identifies the frame being part of a burst
DATA READ	18 bit	Depends on the register	Answer containing the data read from the y-th register of the y-th device
Frame Num	5 bit	From 0x02 to 0x14	Identifies the n-th frame of a burst answer. In the first frame it is replaced by the Command feedback.

Several burst commands are available:

Table 23. Available burst commands

Command code	Description	Reference
0x78	All cells voltage, Sum of cells, Stack Voltage divider, Instantaneous Current, Balancing status. This command clears the measurement data_ready bit (refer to Section 4.4 Cell voltage measurement)	Table 24

Command code	Description	Reference
0x7A	Diagnostic info. This command is intended to provide a rapid overview of the fault status, allowing the MCU to perform proper masking procedure. The command does not reset diagnostic latches.	Table 25
0x7B	Coulomb Counter, Instantaneous Current, Configuration Integrity, Oscillator, Balancing Timer Monitor, GPIO measurements. This command clears the Coulomb Counter registers and the measurement data_ready bit (refer to Section 4.13.1 Coulomb counting and Section 4.4 Cell voltage measurement)	Table 26

Fields with green shading are reset upon burst read.

Table 24. 0x78 burst command

frame num.	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	VCELL1_EN	d_rdy_Vcell1	VCell1															
2	VCELL2_EN	d_rdy_Vcell2	VCell2															
3	VCELL3_EN	d_rdy_Vcell3	VCell3															
4	VCELL4_EN	d_rdy_Vcell4	VCell4															
5	VCELL5_EN	d_rdy_Vcell5	VCell5															
6	VCELL6_EN	d_rdy_Vcell6	VCell6															
7	VCELL7_EN	d_rdy_Vcell7	VCell7															
8	VCELL8_EN	d_rdy_Vcell8	VCell8															
9	VCELL9_EN	d_rdy_Vcell9	VCell9															
10	VCELL10_EN	d_rdy_Vcell10	VCell10															
11	VCELL11_EN	d_rdy_Vcell11	VCell11															
12	VCELL12_EN	d_rdy_Vcell12	VCell12															
13	VCELL13_EN	d_rdy_Vcell13	VCell13															
14	VCELL14_EN	d_rdy_Vcell14	VCell14															
15	vsum_batt19_2																	
16	vsum_batt1_0		VBATT_DIV															
17	data_ready_vsum	data_ready_vbattdiv	SOC	OVR_LATCH	CONF_CYCLIC_EN	DUTY_ON	VSUM_OV	VSUM_UV	TimedBalacc	TimedBalTimer							bal_on	eof_bal
18	CUR_INST_calib																	

Table 25. **0x7A burst command**

frame num.	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	OVR_LATCH	TCYCLE_OVF	sense_plus_open	sense_minus_open	Otchip	VANA_OV	VDIG_OV	VTREF_UV	VTREF_OV	VREG_UV	VREG_OV	VCOM_OV	VCOM_UV	wu_gpio7	wu_spi	wu_isoline	wu_faulth	wu_cyc_wup
2	loss_agnd	loss_dgnd	loss_cgnd	loss_gndref	TrimmCalOk	CoCouOvF	EoBtimeerror	GPIO9_fastchg_OT	GPIO8_fastchg_OT	GPIO7_fastchg_OT	GPIO6_fastchg_OT	GPIO5_fastchg_OT	GPIO4_fastchg_OT	GPIO3_fastchg_OT	GPIO9_OPEN	GPIO8_OPEN	GPIO7_OPEN	GPIO6_OPEN
3	GPIO5_OPEN	GPIO4_OPEN	GPIO3_OPEN	EEPROM_DWNLD_DONE	BAL14_OPEN	BAL13_OPEN	BAL12_OPEN	BAL11_OPEN	BAL10_OPEN	BAL9_OPEN	BAL8_OPEN	BAL7_OPEN	BAL6_OPEN	BAL5_OPEN	BAL4_OPEN	BAL3_OPEN	BAL2_OPEN	BAL1_OPEN
4	VBAT_COMP_BIST_FAIL	VREG_COMP_BIST_FAIL	VCOM_COMP_BIST_FAIL	VTREF_COMP_BIST_FAIL	BAL14_SHORT	BAL13_SHORT	BAL12_SHORT	BAL11_SHORT	BAL10_SHORT	BAL9_SHORT	BAL8_SHORT	BAL7_SHORT	BAL6_SHORT	BAL5_SHORT	BAL4_SHORT	BAL3_SHORT	BAL2_SHORT	BAL1_SHORT
5	EEPROM_CRC_ERR_CAL_FF	HWSC_DONE	VBAT_OPEN	CELL14_OPEN	CELL13_OPEN	CELL12_OPEN	CELL11_OPEN	CELL10_OPEN	CELL9_OPEN	CELL8_OPEN	CELL7_OPEN	CELL6_OPEN	CELL5_OPEN	CELL4_OPEN	CELL3_OPEN	CELL2_OPEN	CELL1_OPEN	CELL0_OPEN

frame num.	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
6	EEPROM_CRC_ERR_SECT_0	Comm_timeout_flt	EEPROM_CRC_ERR_CAL_RAM	RAM_CRC_ERR	VCELL14_UV	VCELL13_UV	VCELL12_UV	VCELL11_UV	VCELL10_UV	VCELL9_UV	VCELL8_UV	VCELL7_UV	VCELL6_UV	VCELL5_UV	VCELL4_UV	VCELL3_UV	VCELL2_UV	VCELL1_UV
7	VBATT_WRN_OV	VBATT_WRN_UV	VBATTCRIT_UV	VSUM_UV	VCELL14_OV	VCELL13_OV	VCELL12_OV	VCELL11_OV	VCELL10_OV	VCELL9_OV	VCELL8_OV	VCELL7_OV	VCELL6_OV	VCELL5_OV	VCELL4_OV	VCELL3_OV	VCELL2_OV	VCELL1_OV
8	bal_on	eof_bal	VBATTCRIT_OV	VSUM_OV	GPIO9_OT	GPIO8_OT	GPIO7_OT	GPIO6_OT	GPIO5_OT	GPIO4_OT	GPIO3_OT	GPIO9_UT	GPIO8_UT	GPIO7_UT	GPIO6_UT	GPIO5_UT	GPIO4_UT	GPIO3_UT
9	GPO6on	GPO5on	GPO4on	GPO3on	VCELL14_BAL_UV	VCELL13_BAL_UV	VCELL12_BAL_UV	VCELL11_BAL_UV	VCELL10_BAL_UV	VCELL9_BAL_UV	VCELL8_BAL_UV	VCELL7_BAL_UV	VCELL6_BAL_UV	VCELL5_BAL_UV	VCELL4_BAL_UV	VCELL3_BAL_UV	VCELL2_BAL_UV	VCELL1_BAL_UV
10	Fault_L_line_status	GPO9on	GPO8on	GPO7on	GPO9short	GPO8short	GPO7short	GPO6short	GPO5short	GPO4short	GPO3short	GPIO_BIST_FAIL						
11	HeartBeat_fault	FaultHline_fault	FaultH_EN	HeartBeat_En	MUX_BIST_FAIL													

frame num.	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
12	curr_sense_ovc_sleep	HeartBeatCycle			BIST_BAL_COMP_HS_FAIL							BIST_BAL_COMP_LS_FAIL						
13	curr_sense_ovc_norm	OSCFail	clk_mon_en	clk_mon_init_done	OPEN_BIST_FAIL													

Table 26. 0x7B burst command

frame num.	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	CoulombCounter_en	CoCouOvF	CoulombCntTime															
2	sense_plus_open	sense_minus_open	CoulombCounter_msb															
3	curr_sense_ovc_sleep	curr_sense_ovc_norm	CoulombCounter_lsb															
4	CUR_INST_synch																	
5	CUR_INST_calib																	
6	GPIO3_OT	d_rdy_gpio3	GPIO3_MEAS															
7	GPIO4_OT	d_rdy_gpio4	GPIO4_MEAS															
8	GPIO5_OT	d_rdy_gpio5	GPIO5_MEAS															
9	GPIO6_OT	d_rdy_gpio6	GPIO6_MEAS															
10	GPIO7_OT	d_rdy_gpio7	GPIO7_MEAS															
11	GPIO8_OT	d_rdy_gpio8	GPIO8_MEAS															
12	GPIO9_OT	d_rdy_gpio9	GPIO9_MEAS															
13	TrimmCalOk	d_rdy_vtref	VTREF_MEAS															
14	GPIO3_UT	GPIO4_UT	GPIO5_UT	GPIO6_UT	GPIO7_UT	GPIO8_UT	GPIO9_UT	bal_on	eof_bal	OTchip	TempChip							

4.2.4.3 *Broadcast access*

The Broadcast access allows sending a WRITE command over the communication bus to all the L9963E units. Broadcast READ is not supported.

The broadcast write is followed by an echo frame generated by the L9963E Master unit. This is necessary in order to avoid multiple devices accessing the communication bus simultaneously, in order to generate a conflict error.

Table 27. SPI protocol: broadcast access frame

	39	38	37 36 35 34 33	32 31 30 29 28 27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
MOSI	P.A.=1	R/W = 1	Dev ID = 0000	Address	GSW	DATA WRITE	CRC
MISO	1	1	Special Answer (0000)	Address ECHO	GSW ECHO	DATA WRITE ECHO	CRC

L9963E Master unit will answer to a broadcast READ command with the following frame:

Table 28. SPI protocol: broadcast read answer frame

	39	38	37 36 35 34 33	32 31 30 29 28 27 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
MOSI	P.A.=1	R/W = 0	Dev ID = 0000	Address	GSW	DATA WRITE	CRC
MISO	0	0	Special Answer (0000)	Address ECHO	GSW = 00	0x0	CRC

Table 29. Broadcast access frame field description:

Field	Length	Value	Description
P.A.	1 bit	1	Command sent by Master unit (MOSI)
R/W	1 bit	1	Write
Dev ID	5 bit	0x0	The 0x0 address identifies broadcast commands
Address Address ECHO	7 bit	From 0x00 to 0x5F	Identifies the y-th register of the device
GSW	2 bit	0b00	Refer to Section 4.2.4.5 Global Status Word (GSW)
CRC	6 bit	From 0x00 to 0x3F	CRC calculated on the [39-7] field of the frame. Refer to Section 4.2.4.6 CRC calculation
DATA WRITE DATA WRITE ECHO	18 bit	Depends on the register	Data to be written in the y-th register of the x-th device
Special Answer	5 bit	0x0	Identifies the ECHO frame issued in a broadcast write protocol

4.2.4.4 *Special frames*

Table 30. SPI protocol special frames

Frame Type	Frame Code	Frame Issued
Default	0x0000000016	After a wake up event
Not Expected Frame	0xC1FCFFFC6C	In a Burst access, in case the MCU clocks a number of answer frames higher than the expected
Timeout Frame	0xC1FCFFFC87	In case no answer is received after the timeout TSPI_ERR.
Busy Frame	0xC1FCFFFCDE	In case the MCU sends a frame while the Master device is still transmitting or waiting for an answer (TSPI_ERR not expired)
CRC Error Frame	0xC1FCFFFD08	In case a unit configured in SPI mode (SPIEN = 1) receives a corrupted frame. When a unit is configured in isolated SPI mode (SPIEN = 0), no answer will be issued upong CRC error detection.

4.2.4.5 *Global Status Word (GSW)*

The global status word is made of 2 bits. The MSB (bit 25) is dedicated to the the internal fault detection (all failures except the FAULTH detection), while the LSB (bit 24) implements the **Rolling counter**:

Table 31. GSW code description

GSW	Description
0X(1)	L9963E hasn't detected any internal failure (but could be propagating a failure from an upper device in the stack)
1X(1)	L9963E has detected an internal failure (and could be also propagating a failure from an upper device in the stack)

1. *'X' = don't care.*

The GSW can be exploited by the MCU fault handling routine to understand which device of the daisy chain has self-detected a failure.

4.2.4.6 *CRC calculation*

Each frame is equipped with a 6-bit CRC code in order to guarantee information integrity. In case a unit receives a corrupted frame, it will be discarded.

Table 32. CRC calculation information

CRC	
Length	6 bit
Polynomial	$X^6 + X^4 + X^3 + 1$
Seed	0b111000

4.3 FAULT line

The FAULTL/FAULTH pin pair provides an isolated communication interface exploiting optical-isolators to implement uni-directional transmission of the failure signal from the highest L9963E in the stack down to the µC.

The FAULT line main purpose is to interrupt the MCU activity in case one of the daisy-chained L9963E detects a failure. Recommended interrupt handling routine should implement a strategy to detect which of the several L9963E has self-detected a failure. This can be easily done by sending a communication frame to each L9963E, reading back the corresponding fault bit of the **Global Status Word (GSW)**.

Any failure is propagated/generated by an upper device via its FAULTL pin. It is then sensed by a lower device on its FAULTH pin.

For the circuit and the BOM, refer to Section 6.7 FAULT line circuit.

4.3.1 State transitions in case of failure detection

FAULT line is functional in the following states: **Normal, Cyclic Wakeup, Silent Balancing** and **Sleep.**

Table 33. FAULT line functionality and L9963E states

State	Functions available	State transition in case of failure
Normal	Fault self-detection and propagation. Heartbeat generation.	None
Cyclic Wakeup	Fault self-detection (during ON phase) and propagation (always)	Go to Normal
Silent Balancing	Fault propagation	Go to Normal (in case of external failure)
Sleep	Fault propagation	Go to Normal (in case of external failure)

4.3.2 FAULT line configuration

In case a failure is detected, the FAULTL pin is driven to its active state, while if no failure occurs, the FAULTL pin holds its inactive value. Pin states depend on FAULT line configuration (selectable via the **HeartBeat_En** bit) and on L9963E state.

Table 34. FAULTH line configuration and FAULTL pin states

L9963E State	HeartBeat_En	FAULTL Inactive state	FAULTL Active state
Normal	0	Low	High
	1	Programmable PWM	High
Sleep, Silent Balancing, Cyclic Wakeup	X	Low	High (once moved to Normal)

The FAULT line stays asserted and L9963E is kept in **Normal** unless communication timeout occurs. The MCU is responsible for clearing any fault latch. Once all failures are cleared, the FAULTL pin returns to its inactive state.

When the heartbeat is activated, the PWM period THB_CYCLE can be programmed via the **HeartBeatCycle** register. The pulse duration in the inactive state is fixed to THB_PULSE. The heartbeat presence allows to guarantee the integrity of the FAULT line. Moreover, each L9963E is capable of sensing its upper companion activity by monitoring the heartbeat continuity.

In case the heartbeat is disabled, the MCU can still verify the continuity of the FAULT line by forcing the unit on the top of the chain to raise its FAULTL pin. This can be done by setting **FaultL_force = 1** via SPI.

Before moving L9963E moves to a low power state (**Sleep**, **Cyclic Wakeup** or **Silent Balancing**), MCU must disable the heartbeat functionality by programming **HeartBeat_En = 0**. Such an operation must be performed at least TFIL_H_LONG before sending the broadcast **GO2SLP** command, in order to avoid false fault detections (refer to Figure 15 for an example).

4.3.3 Failure sources

There are two failure sources:

- **Internal**: L9963E detects a failure (self-detection)
- **External**: a failure incoming from an upper unit is being input to the FAULTH pin (propagation)

4.3.3.1 Internal failure detection

If L9963E self-detects a failure, it drives the FAULTL pin to its active state, regardless of any activity on the FAULTH pin.

For further information about all the failures and the subsequent actions, refer to Section 4.11.28 Safety mechanisms summary.

4.3.3.2 External failure detection

Failure detection from external sources is sensed on FAULTH pin only if **FaultH_EN = '1'** and **Farthest_Unit = '0'**. The unit at the top of the stack does not receive any signal input to the FAULTH pin. Hence, external failure detection must be disabled by setting **FaultH_EN = '0'** and **Farthest_Unit = 1** via SPI.

For all other units, the detection criteria are adapted to the FAULT line configuration programmed by **HeartBeat_En** bit, as shown in the table below.

Table 35. FAULTH filtering strategies

L9963E State	Configuration	Fault detection condition	Description
Normal	HeartBeat_En = 1	FAULTH = 1 for t > $T_{FIL\_H\_LONG}$	Static '1' detected on FAULTH pin, **FaultHline_fault = 1**
		FAULTH = 0 for t > 1.2*T_{HB_CYCLE}	Absence of heartbeat from upper device, **HeartBeat_fault = 1**
	HeartBeat_En = 0	FAULTH = 1 for t > $T_{FIL\_H\_SHORT}$	High logic level detected on FAULTH pin, **FaultHline_fault = 1**
Sleep, Silent Balancing, Cyclic Wakeup	HeartBeat_En = X	FAULTH = 1 for t > $T_{FIL\_H\_SHORT}$	High logic level detected on FAULTH pin, **FaultHline_fault = 1**

The MCU at the bottom of the chain is supposed to adopt the filtering strategy described in Table 35 for failure detection.

Summary of L9963E fault line configurations is available in the following table:

Table 36. Summary of L9963E FAULT line configurations

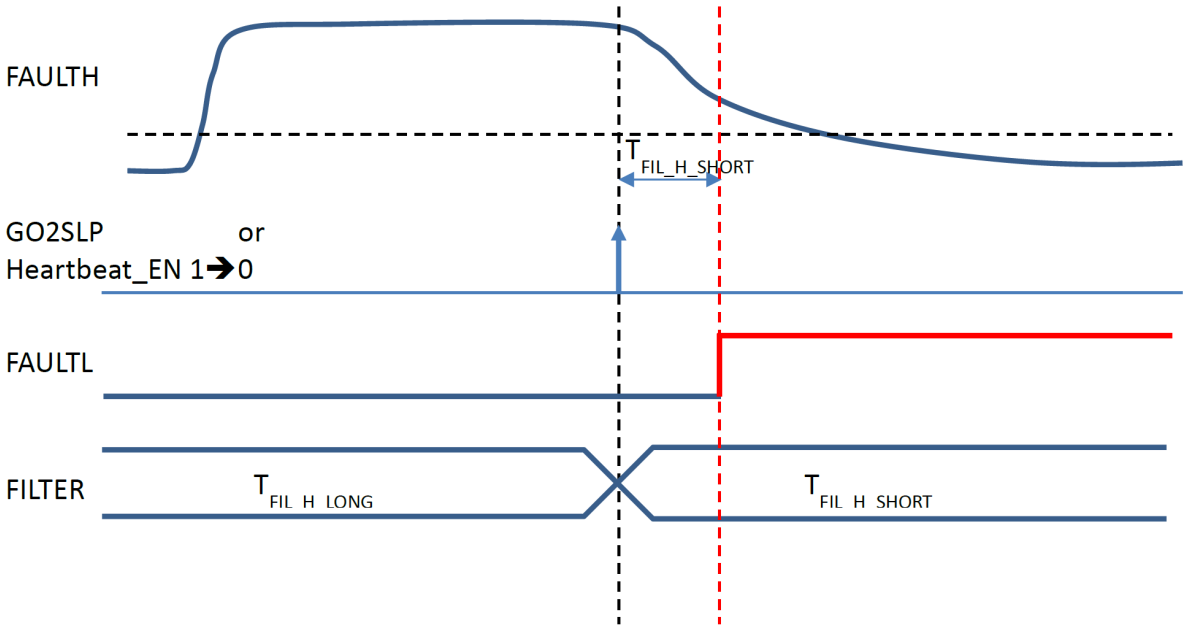
FaultH_EN	HeartBeat_En	Farthest_Unit	L9963E behavior	Optimized for
0	0	0	FAULTH receiver disabled. The FAULTH line pin is considered Low whatever its value is. FAULTL operates in static logic mode and can be set static high by **internal** fault **only**	Topmost unit of the chain in static logic value configuration
0	0	1		
0	1	0		
0	1	1	FAULTH receiver disabled. The FAULTH line pin is considered Low whatever its value is. FAULTL operates in heartbeat mode and can be set static high by **internal** fault **only**	Topmost unit of the chain in heartbeat configuration
1	0	0	FAULTH receiver enabled with short filter ($T_{FIL\_H\_SHORT}$) because HeartBeat signal is **not** possible. FAULTL operates in static logic mode and can be set static high by **both** external and internal fault	Unit in the middle of the chain or transceiver, in static logic value configuration
1	0	1	FAULTH receiver disabled. The FAULTH line pin is considered Low whatever its value is, because the Farthest Unit considers FaultH_EN = 0 whatever FaultH_EN value is. FAULTL operates in static logic mode and can be set static high by **internal** fault **only**	Topmost unit of the chain in static logic value configuration
1	1	0	FAULTH receiver enabled with long filter ($T_{FIL\_H\_LONG}$) because HeartBeat signal **is** possible FAULTL operates in heartbeat mode and can be set static high by **both** external and internal fault	Unit in the middle of the chain or transceiver, in heartbeat configuration
1	1	1	FAULTH receiver disabled. The FAULTH line pin is considered Low whatever its value is because the Farthest Unit always considers FaultH_EN = 0 whatever FaultH_EN value is. FAULTL operates in heartbeat mode and can be set static high by **internal** fault **only**	Topmost unit of the chain in heartbeat configuration

When disabling heartbeat mode (**HeartBeat_En 1 è 0**) or when moving to a low power state (**GO2SLP**), L9963E switches immediately from $T_{FIL\_H\_LONG}$ to $T_{FIL\_H\_SHORT}$. It is MCU responsibility to handle this transition correctly, avoiding false FAULTH detection (see Figure 15 as an example).

Follow this procedure:

1. Send a broadcast frame with **FaultH_EN = 0** and **HeartBeat_En = 0** in order to disable both heartbeat and fault receiver;
2. Wait for $T_{HB\_CYCLE\_000}$ (4 ms);
3. Send a broadcast frame with **FaultH_EN = 1** to re-enable the fault receiver;
4. (Optional) Send the GO2SLP command.

Figure 15. False failure detection due to sudden heartbeat disable during the duty phase



4.3.4 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V ; -40 °C < Tambient < 105 °C

Table 37. Heart beat electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{HB_PULSE}	High level HeartBeat Pulse duration when HeartBeat function is enabled	Tested by SCAN	-	500	-	µs
T_{HB_CYCLE}	Programmable HeartBeat cycle duration	Tested by SCAN HeartBeatCycle = 000	-	4	-	ms
		Tested by SCAN HeartBeatCycle = 001	-	8	-	ms
		Tested by SCAN HeartBeatCycle = 010	-	32	-	ms
		Tested by SCAN HeartBeatCycle = 011	-	128	-	ms
$T_{FIL\_H\_SHORT}$		Tested by SCAN	-	300	-	µs
$T_{FIL\_H\_LONG}$		Tested by SCAN	-	3.5	-	ms

4.4 Cell voltage measurement

A level shifter is able to report the cell voltage at the input of the low voltage cell ADC.

All cells are acquired in parallel, with no desynchronization between samples. Immunity to differential noise can be increased by tuning the acquisition window $T_{CYCLEADC}$.

The user may program the voltage acquisition window $T_{CYCLEADC}$ among 8 different values:

- The whole option set is available for both **ADC_FILTER_SOC** and **ADC_FILTER_CYCLE**. These parameters apply respectively to **On-Demand Conversions** and **Cyclic Conversions**
- The first 4 rows are available for **ADC_FILTER_SLEEP** configuration. This parameter applies to **Cyclic Conversions** performed in **Cyclic Wakeup**

For further information, refer to Section 4.12 Voltage conversion routine.

Table 38. Selection of the ADC filter values

Parameter	Code	Window amplitude (typ)	Recommended wait time T_{DATA_READY}	Minimum sample time achievable T_{SAMPLE_MIN}
$T_{CYCLEADC\_000}$	000	290 µs	380 µs	760 µs
$T_{CYCLEADC\_001}$	001	1.16 ms	1.34 ms	2.68 ms
$T_{CYCLEADC\_010}$	010	2.32 ms	2.61 ms	5.22 ms
$T_{CYCLEADC\_011}$	011	9.28 ms	10.27 ms	20.54 ms
$T_{CYCLEADC\_100}$	100	18.56 ms	20.48 ms	40.96 ms
$T_{CYCLEADC\_101}$	101	37.12 ms	40.89 ms	81.78 ms
$T_{CYCLEADC\_110}$	110	74.24 ms	81.72 ms	163.44 ms
$T_{CYCLEADC\_111}$	111	148.48 ms	163.4 ms	326.8 ms

Cell measurement results are stored in **Vcellx** registers and are 16-bit wide. To obtain the result, apply the following formula:

Cell voltage measurement

$$V_{CELL} = BINARY\_CODE \times V_{CELLRES} \quad (2)$$

After launching a cell conversion, the MCU should wait at least for the recommended wait time T_{DATA_READY} before retrieving the cell data. This allows L9963E to perform sample interpolation and calibration.

The data readiness is confirmed by the assertion of:

- **d_rdy_Vcellx** bit for **VCELLx** registers
- **d_rdy_gpiox** bit for **GPIOx_MEAS** registers
- **d_rdy_vtref** bit for **VTREF** register
- **data_ready_vbattdiv** for **VBATT_DIV** register
- **data_ready_vsum** for **vsum_batt19_0** register

Polling the data ready bit is possible but not recommended, since it causes a higher consumption from the battery stack due to communication.

*Note: If **Coulomb Counting Routine** is activated, MCU should add $T_{CYCLEADC\_CUR}$ to the T_{DATA_READY} wait time in order to account for the maximum synchronization delay between voltage and current samples. For further information refer to Section 4.13.1 Coulomb counting.*

Before launching another conversion, MCU should wait at least for the recommended minimum T_{SAMPLE} in order to avoid conflict with previous conversions. In case this happens, the new request will be discarded.

Hence, given a differential signal with bandwidth **BW**:

- The MCU should sample it using at least $T_{SAMPLE} = 1 / 2BW$, in order to fulfill Nyquist criterion
  - All the $T_{CYCLEADC\_XXX}$ values in Table 38, whose T_{SAMPLE_MIN} is lower than T_{SAMPLE} can be exploited in application;

- The best performances in terms of differential noise attenuation can be achieved by choosing the longest $T_{CYCLEADC\_XXX}$ among the valid ones.

4.4.1 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C; Shift between AGND, DGND, CGND, GNDREF below +/-100 mV

Table 39. Cell voltage ADC electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CELL}	Cell Voltage Input Measurement Range	Design info C(n), n=1-14	0.1		5	V
$V_{CELLRES}$	Cell Voltage Measurement Resolution	Design info		89		µV
I_{CELL_LEAK}	Cn leakage current	C(n), n=1-14 |C(n) – C(n-1)| < 6V			300	nA
$V_{CELLERR0}$	Accuracy VBAT = C14 C0 = GND	0.1V ≤ V_{CELL} < 0.3 V -40 °C < TJ < 125 °C	-10		10	mV
$V_{CELLERR1}$		0.3 V ≤ V_{CELL} < 0.5 V -40 °C < TJ < 125 °C	-5		5	mV
$V_{CELLERR2}$		0.5 V ≤ V_{CELL} ≤ 5 V 105 °C < TJ < -125 °C	-6		6	mV
$V_{CELLERR3}$		0.5 V ≤ V_{CELL} < 3.2 V -40 °C < TJ < 105 °C	-1		1	mV
$V_{CELLERR4}$		3.2 V ≤ V_{CELL} ≤ 4.3 V -40 °C < TJ < 105 °C	-1.4		1.4	mV
$V_{CELLERR5}$		4.3 V ≤ V_{CELL} ≤ 4.7 V -40 °C < TJ < 105 °C	-1.6		1.6	mV
$V_{CELLERR6}$		4.7 V ≤ V_{CELL} ≤ 5 V -40 °C < TJ < 105 °C	-5		5	mV
$V_{CELLERR0}$	Accuracy + Drift[1] VBAT = C14 C0 = GND	0.1V ≤ V_{CELL} < 0.3 V -40 °C < TJ < 125 °C	-10		10	mV
$V_{CELLERR1}$		0.3 V ≤ V_{CELL} < 0.5 V -40 °C < TJ < 125 °C	-5		5	mV
$V_{CELLERR2}$		0.5 V ≤ V_{CELL} ≤ 5 V 105 °C < TJ < -125 °C	-7		7	mV
$V_{CELLERR3}$		0.5 V ≤ V_{CELL} < 3.2 V -40 °C < TJ < 105 °C	-1.4		1.4	mV
$V_{CELLERR4}$		3.2 V ≤ V_{CELL} ≤ 4.3 V -40 °C < TJ < 105 °C	-2		2	mV
$V_{CELLERR5}$		4.3 V ≤ V_{CELL} ≤ 4.7 V -40 °C < TJ < 105 °C	-2.6		2.6	mV
$V_{CELLERR6}$		4.7 V ≤ V_{CELL} ≤ 5 V -40 °C < TJ < 105 °C	-6.5		6.5	mV

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CELL_NOISE1}	$T_{CYCLEADC} = T_{CYCLEADC\_000}$	0.1 V ≤ V_{CELL} ≤ 5 V -40 °C < TJ < 125 °C			600	µVrms
V_{CELL_NOISE2}	$T_{CYCLEADC} = T_{CYCLEADC\_001}$	0.1 V ≤ V_{CELL} ≤ 5 V -40 °C < TJ < 125 °C			400	µVrms
V_{CELL_NOISE3}	$T_{CYCLEADC} = T_{CYCLEADC\_010}$	0.1 V ≤ V_{CELL} ≤ 5 V -40 °C < TJ < 125 °C			200	µVrms
V_{CELL_NOISE4}	$T_{CYCLEADC} = T_{CYCLEADC\_011}$, $T_{CYCLEADC\_100}$, $T_{CYCLEADC\_101}$, $T_{CYCLEADC\_111}$	0.1 V ≤ V_{CELL} ≤ 5 V -40 °C < TJ < 125 °C			150	µVrms
$T_{CYCLEADC\_000}$	Conversion Time to Measure all cells	Tested by SCAN		290		µs
$T_{CYCLEADC\_001}$		Tested by SCAN		1.16		ms
$T_{CYCLEADC\_010}$		Tested by SCAN		2.32		ms
$T_{CYCLEADC\_011}$		Tested by SCAN		9.28		ms
$T_{CYCLEADC\_100}$		Tested by SCAN		18.56		ms
$T_{CYCLEADC\_101}$		Tested by SCAN		37.12		ms
$T_{CYCLEADC\_110}$		Tested by SCAN		74.24		ms
$T_{CYCLEADC\_111}$		Tested by SCAN		148.48		ms
V_{CELL_OV}	Cell Over-voltage Fault Threshold **threshVcellOV**	Application info, tested by SCAN	0		5.80992	V
$V_{CELL\_OV\_RES}$	Cell Over-voltage Fault Threshold Resolution	Design info		22.784		mV
V_{CELL_UV}	Cell Under-voltage Fault Threshold **threshVcellUV**	Application info, tested by SCAN	0		5.80992	V
$V_{CELL\_UV\_RES}$	Cell Under-voltage Fault Threshold Resolution	Design info		22.784		mV
$V_{CELL\_BAL\_UV\_\Delta}$	Cell Balance Under-voltage Fault Threshold **Vcell_bal_UV_delta_thr**	Application info, Tested by SCAN	0		5	V
$V_{CELL\_BAL\_UV\_RES}$	Cell Balance Under-voltage Fault Threshold Resolution	Design info		22.784		mV
R_{LPF_OPEN}	Equivalent open resistance in series to Cn pin	Application info		4		KΩ
V_{CxOPEN}	Cx open threshold for series resistor	Application info. Maximum voltage drop on the series resistor. To prevent excessive leakage from differential filtering capacitor Tested by SCAN		200		mV
$I_{OPEN\_DIAG\_CX}$	Pulldown current used for cell open load detection	For C1..14	40	50	60	µA
$I_{OPEN\_DIAG\_C0}$		For C0	-60	-50	-40	µA
$V_{ADC\_CROSS\_FAIL}$	Critical mismatch between ADC results causing cross-check failure	Tested by SCAN		20		mV
T_{CxOPEN_SET}	Settling time for cell open diagnostics	Tested by SCAN		0.7		ms

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{CELL\_SET\_01}$	Settling time in respect to the first step of the **Voltage Conversion Routine** for balancing auto pause and VTREF dynamic enable	Tested by SCAN		175		µs
$T_{CELL\_SET\_10}$	Settling time in respect to the first step of the **Voltage Conversion Routine** for balancing auto pause and VTREF dynamic enable	Tested by SCAN		350		µs
$T_{CELL\_SET\_11}$	Settling time in respect to the first step of the **Voltage Conversion Routine** for balancing auto pause and VTREF dynamic enable	Tested by SCAN		700		µs

1. *The drift in spec accounts for the effects of both soldering and ageing. Post-soldering drift is provided on "as is" basis for information only and it has been evaluated on a limited population of 30 samples, hence subject to potential deviations. HTOL ageing was evaluated according to automotive qualification flow.*

4.5 VBAT voltage measurement

4.5.1 Total battery voltage measurement

A measurement of the total stack voltage is implemented in two ways:

- By summing the single cell voltage during the **Cell Conversion**, thus obtaining VBATT_SUM, stored in **Vsum_batt(19:0)**
- Directly converting the VBAT pin during **VBAT Conversion**, thus obtaining VBATT_MONITOR, stored in **VBAT_DIV**

Both results can be read as:

Stack voltage decoding

$$\begin{cases} V_{BATT\_SUM} = BINARY\_CODE \times V_{BATRES} \\ V_{BATTT\_MONITOR} = BINARY\_CODE \times V_{BATRES} \end{cases} \quad (3)$$

Besides that, an independent analog comparator monitors the VBAT pin for fast UV/OV detection.

Refer to Section 4.11.2 Total battery VBAT diagnostic for further information about diagnostics.

4.5.2 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C; Shift between AGND, DGND, CGND, GNDREF below +/-100 mV

Table 40. Stack voltage measurement electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BATRES}	VBAT Voltage Measurement Resolution(1)	Design info 70 V full scale input, obtained by sum of all cell voltages		89		µV
$V_{BAT\_OV\_SUM}$	VBAT Over-voltage Fault Threshold(2) VBATT_SUM_OV_TH	Tested by SCAN Related to sum of ADC (V_{BATT_SUM})		70.35		V
$V_{BAT\_UV\_SUM}$	VBAT Under-voltage Fault Threshold(2) VBATT_SUM_UV_TH	Tested by SCAN Related to sum of ADC (V_{BATT_SUM})		10		V
$V_{BAT\_SUM\_RES}$	Stack voltage UV/OV resolution for Sum Of Cells	Tested by SCAN		364.544		mV

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BAT\_DIV\_RES}$	VBAT Voltage Measurement Resolution Related to ADC + divider ($V_{BATT\_MONITOR}$)	Design info 70 V full scale input, Related to ADC + divider ($V_{BATT\_MONITOR}$)		1.33		mV
$V_{BAT\_SUM\_ERR\_1}$	VBAT = C14 C0 = GND Sum of cells accuracy + drift Noise contribution of each single cell is given in Table 39	0.1 V ≤ V_{CELL} < 0.3 V -40 °C < T_J < 125 °C	-140		140	mV
$V_{BAT\_SUM\_ERR\_2}$		0.3 V ≤ V_{CELL} < 0.5 V -40 °C < T_J < 125 °C	-70		70	mV
$V_{BAT\_SUM\_ERR\_3}$		0.5 V ≤ V_{CELL} < 0.5 V 105 °C < T_J < -125 °C	-56		56	mV
$V_{BAT\_SUM\_ERR\_4}$		0.5 V ≤ V_{CELL} < 3.2 V -40 °C < T_J < 105 °C	-20		20	mV
$V_{BAT\_SUM\_ERR\_5}$		3.2 V ≤ V_{CELL} < 4.3 V -40 °C < T_J < 105 °C	-28		28	mV
$V_{BAT\_SUM\_ERR\_6}$		4.3 V ≤ V_{CELL} < 5 V -40 °C < T_J < 105 °C	-36.5		36.5	mV
V_{BATERR}	VBAT Voltage Measurement Error	Related to ADC + divider ($V_{BATT\_MONITOR}$) Tested by SCAN			±0.5%	VBAT
$V_{BAT\_CRITICAL\_OV\_TH}$	VBAT Over-voltage Fault Threshold	Related to ADC + divider ($V_{BATT\_MONITOR}$) Tested by SCAN	70	70.35	70.7	V
$V_{BAT\_OVHYS\ (ADC)}$	VBAT Over-voltage Hysteresis Voltage	Related to ADC + divider ($V_{BATT\_MONITOR}$) Tested by SCAN		200		mV
$V_{BAT\_CRITICAL\_UV\_TH}$	VBAT Under-voltage Fault Threshold	Related to ADC + divider ($V_{BATT\_MONITOR}$) Tested by SCAN	9.6	9.95	10.3	V
V_{BAT_UVHYS}	VBAT Under-voltage Hysteresis Voltage	Related to ADC + divider (VBATT_MONITOR) Tested by SCAN		200		mV
$V_{BAT\_OV\_WARNING\ (COMP)}$	VBAT warning OV Threshold	Analog comparator related to VBAT	64	67	70	V
$V_{BAT\_OV\_WARN\_HYS\ (COMP)}$	VBAT warning OV Hysteresis Voltage	Analog comparator related to VBAT	2.2	2.5	2.8	V
$V_{BAT\_UV\_WARNING\ (COMP)}$	VBAT warning UV Threshold	Analog comparator related to VBAT	10	11	12	V
$V_{BAT\_UV\_WARN\_HYS\ (COMP)}$	VBAT warning UV Hysteresis Voltage	Analog comparator related to VBAT	230	300	370	mV
T_{VBAT_FILT}	UV/OV digital filter time	Tested in SCAN		300		µs

1. *The total voltage measurement is used for detecting the OV/UV of the chip inputs. Moreover, it also provides a redundant check for functional integrity and measurement accuracy of the cell voltage. It is realized by summing the voltage of all cell ADC.*
2. *The OV/UV thresholds of VBAT can be set by user.*

4.6 Cell current measurement

The current flowing into the external shunt resistance RSENSE is measured through a differential amplifier stage (connected between ISENSEP/ISENSEM pins) feeding a 18 bits ADC.

The current conversion chain can be enabled through the **CoulombCounter_en** bit and runs in background to perform the **Coulomb Counting Routine**.

Moreover, L9963E also allows to synchronize the **Voltage Conversion Routine** and the **Coulomb Counting Routine** for a precise State Of Charge estimation. Everytime an on-demand voltage conversion is requested by setting **SOC = 1**, the actual conversion start is delayed until the first useful current conversion takes place. This might result in a maximum delay of TCYCLEADC_CUR, that must be taken into account by user SW only in case current ADC is enabled.

Synchronized current sample is available into the **CUR_INST_Synch**.

4.6.1 Cell current ADC

In the typical application, the current measurement is performed by detecting the voltage drop on a shunt resistor RSENSE with a value of 0.1 mΩ, with a current range of +/-1500 A. By changing the value of the shunt resistance, it is possible to cover different current ranges.

The architecture includes an ADC that converts ISENSEP-ISENSEM voltage information into a digital value.

The input range of current measurement is set from -1500 A to +1500 A. In the range of [-600 A, +600 A], a constant error value of ±3 A (which is 600 A × ±5‰) is set to avoid the unlimited small error near the zero current. In the range of [-1500 A, -600 A) and (+600 A, +1500 A], the accuracy of ±5‰ is chosen.

Converted value is available in **CUR_INST_calib** register and follows 2's complement notation. Cell current can be calculated according to the following formula:

Cell current measurement

$$\begin{cases} V_{ISENSE} = BINARY\_CODE|_{2's\ complement} \times V_{ISENSE\_RES} \\ I_{CELL} = \dfrac{V_{ISENSE}}{R_{SHUNT}} \end{cases} \quad (4)$$

4.6.2 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C; Shift between AGND,DGND,CGND,GNDREF below +/-100 mV

Table 41. Current measurement electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$Freq_{CURR\_MEAS}$	Frequency of input voltage	Not tested, design info			1	kHz
$T_{CYCLEADC\_CUR}$	Conversion Time for Cyclic Wakeup state operation	Not tested, design info		328.25		µs
I_{CELL}	Current Input Measurement Range	Application only, not to be tested (R_{shunt} = 0.1 mΩ)	-1500		1500	A
$I_{ISENSEP}$	ISENSEP input current	ISENSEP = 0 mV	-140	-70	-30	µA
$I_{ISENSEM}$	ISENSEM input current	ISENSEM = 0 mV	-140	-70	-30	µA
I_{ISENSE_DIF}	ISENSE differential current		-1		1	µA
$I_{ISENSEP\_LEAK}$	ISENSEP input leakage current	ISENSEP = 3.3V			300	nA
$I_{ISENSEM\_LEAK}$	ISENSEM input leakage current	ISENSEM = 3.3V			300	nA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CUR_SENSE}	Input voltage for ADC conversion	Application info. Absolute voltage on ISENSEP/M pins. Same as operating range	-300		+300	mV
$V_{DIFF\_CUR\_SENSE}$	Differential input voltage. ISENSEP- ISENSEM range	Design info	-150		+150	mV
$I_{CELLRES}$	Current Measurement Resolution	±1750 A full scale input assuming 18-bit signed data output and an R_{shunt} = 0.1 mΩ Not tested, application info		13.33		mA
V_{ISENSE_RES}	Voltage Measurement Resolution	±175 mV full scale input assuming 18-bit signed data output Design info		1.33		µV
$I_{CELLERR}$	Current Measurement Error V_{DIFF_SENSE} = V(ISENSE+) - V(ISENSE-)	-150 mV ≤ $V_{DIFF\_CUR\_SENSE}$ < -60 mV, -40 °C < T_J < 125 °C	-0.5		0.5	%
$I_{CELLERR2}$		-60 mV ≤ $V_{DIFF\_CUR\_SENSE}$ ≤ 60 mV -40 °C < T_J < 125 °C	-0.3		0.3	mV
$I_{CELLERR3}$		60 mV < $V_{DIFF\_CUR\_SENSE}$ ≤ 15 0 mV, -40 °C < T_J < 125 °C	-0.5		0.5	%
$I_{CURR\_SENSE\_OC\_SLEEP}$	ISENSE Over-current Fault Threshold in Cyclic Wakeup	Tested in SCAN (76.8A with R_{shunt} = 0.1 mΩ)	0		10.55488	mV
$I_{CURR\_SENSE\_OC\_NORM}$	ISENSE Over-current Fault Threshold in Normal		0		175	mV
$I_{CELL\_OC\_SLP\_RES}$	ISENSE Over-current Fault Threshold Resolution in Cyclic Wakeup	Application info (+/-3.4048A with R_{shunt} = 0.1 mΩ)		340.48		µV
$I_{CELL\_OC\_NORM\_RES}$	ISENSE Over-current Fault Threshold Resolution in Normal	Application info (+/-13.3 mA with R_{shunt} = 0.1 mΩ)		1.33		µV
$V_{ISENSE\_OPEN\_thr}$	ISENSE pins open threshold voltage		1.5	1.7	1.9	V
$T_{CURR\_SENSE\_OPEN\_filter}$	Open digital filter time	Tested in SCAN		60		µs

4.7 Cell balancing

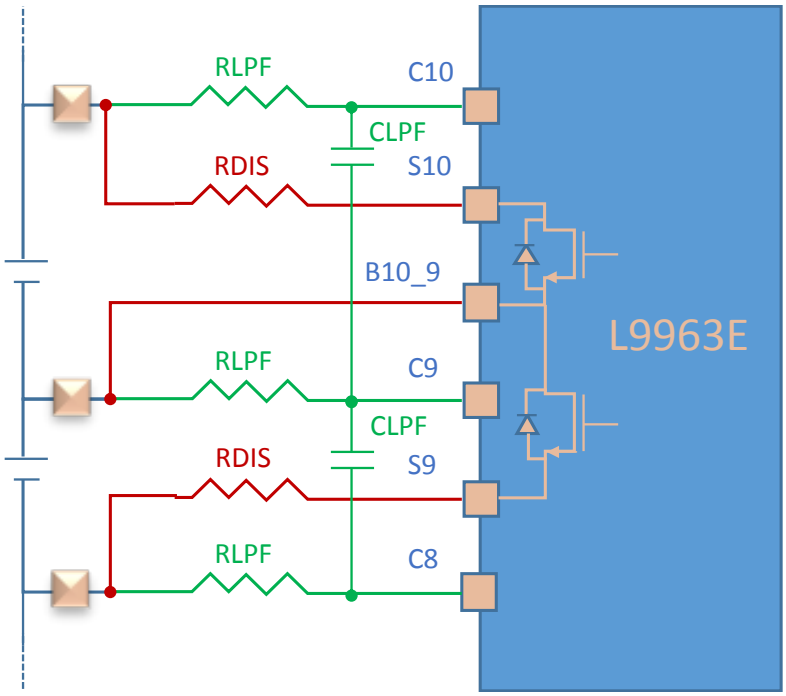
The Sx and Bx_x-1 pins are used to balance the charge of the cells by discharging the ones with a higher SOC (State Of Charge). Balancing can be performed either with external or internal MOSFETs.

Cell balance drivers are powered by VBAT stack voltage. Hence, balancing is theoretically possible even at low cell voltages, with an exception for cell 14. In case V_{CELL14} < $V_{CELL14\_BAL\_MIN}$, the correspondent balancing circuitry will not operate properly and false overcurrent detection may occur.

4.7.1 Passive cell balancing with internal MOSFETs

The internal balancing requires only on-board resistors, and the MOSFETs which are embedded in the chip.

Figure 16. **Cell monitoring with Internal balancing**



- Force lines used for balancing. Connect them as close as possible to the cell connector. This improves cell voltage sensing while balancing is ongoing, by minimizing the voltage drop on the sense lines while current is being sunk
- Sense lines used for cell voltage measurement. Keep away from noisy lines. Recommended PCB layout strategy is to route them over the first layer and shield them using the second layer as GND plane

The on-chip MOSFETs are switched on to sink a current from the cell, thus dissipating charge on RDIS. The affordable balancing current is restricted by the thermal relief on the current source circuits.

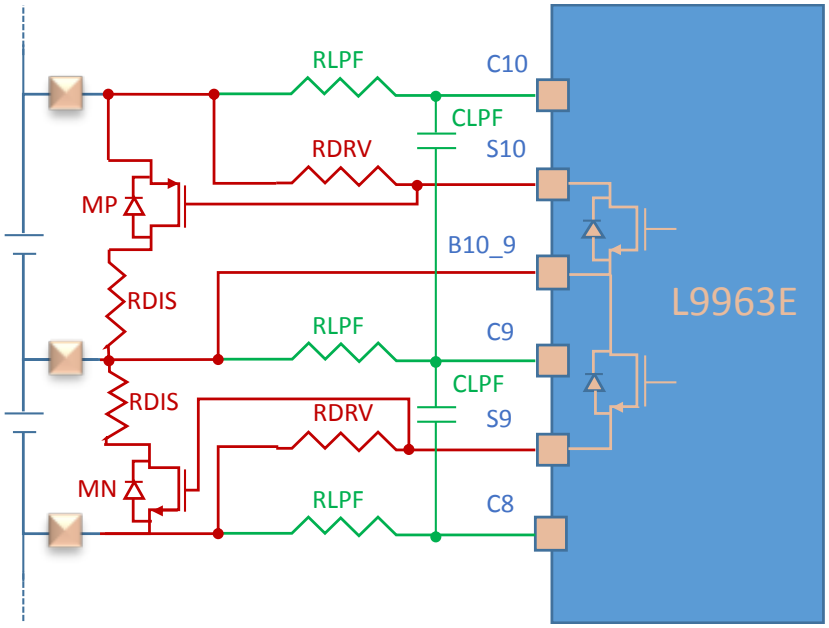
The maximum balance current on each cell is 200 mA. All cells can be balanced simultaneously, provided that junction temperature doesn't exceed the maximum operating defined in Table 5. To prevent thermal overstress, the **Die temperature diagnostic and over temperature** protections are implemented.

For further information, refer to Section 6.6.1 Cell balancing with internal MOSFETs.

4.7.2 Passive cell balancing with external MOSFETs

The external balancing includes the on-board power resistors and MOSFETs driven by the Sx pins.

Figure 17. **Cell monitoring with external balancing with the mixed NMOS and PMOS transistors**



- Force lines used for balancing. Connect them as close as possible to the cell connector. This improves cell voltage sensing while balancing is ongoing, by minimizing the voltage drop on the sense lines while current is being sunk
- Sense lines used for cell voltage measurement. Keep away from noisy lines. Recommended PCB layout strategy is to route them over the first layer and shield them using the second layer as GND plane

The schematic of the external balancing is shown in the figure above.

The cell stack can be divided into adjacent couples and, for each couple, the even cell is balanced by a PMOS, while the odd cell is balanced by an NMOS.

For further information refer to Section 6.6.2 Cell balancing with external MOSFETs.

4.7.3 Balancing modes

In order to allow maximum flexibility, the cell balancing process can be performed both in **Manual Balancing mode** and **Timed Balancing mode**. The configuration can be selected by acting on **Balmode** bit.

In case balancing is interrupted by **Voltage Conversion Routine**, any unfinished balancing state will be saved, and will resume once the measurement is done.

It is started writing **bal_start = 1** and **bal_stop = 0**, while it can be stopped by writing the opposite code (**bal_start = 0** and **bal_stop = 1**). Writing other codes will not alter the status of balancing. Switching from ***Manual Balancing mode*** to ***Timed Balancing mode*** will immediately apply the new settings. Balancing will not be interrupted, unless **ThrTimedBalCell**xx is set to '0' for a specific cell, causing the immediate end of balancing on it.

The **bal_on** and **eof_bal** flags indicate the status of the balancing FSM. Once a balancing task is over MCU must program **bal_start = 0** and **bal_stop = 1** in order to reset the FSM to the idle state.

Table 42. Balancing FSM

bal_on	eof_bal	Balancing Status
0	0	Idle
0	1	Balancing Over
1	0	Ongoing
1	1	Impossible

Note that balancing is performed only on enabled cells (**VCELLx_EN = 1**). Once balance is started, any change to **VCELLx_EN** or **BALx** will not disable the balancing function on the related cell. To disable balancing, **bal_start = 0** and **bal_stop = 1** must be programmed.

4.7.3.1 *Manual balancing mode*

The MCU directly controls the output state of Sn (n=1…14) individually. The start and end time of the balancing are controlled by **bal_start** and **bal_stop**.

To operate manual balancing, follow these steps:

1. Set **Balmode = 01** in the **Bal_2** register to configure manual balancing
2. Set **BALxx = 10** in the **BalCell14_7act** and **BalCell6_1act** registers to enable balancing on the selected cells
3. Set **bal_start = 1** and **bal_stop = 0** in the **Bal_1** register to start balancing

To prevent cell overdischarge due to misconfiguration, Manual Balancing does not support the **Silent Balancing** state. Any GO2SLP command or communication timeout will halt the operation and move L9963E to the **Sleep** mode, even if **slp_bal_conf** flag is set. Balancing will not be resumed once the device is woken up.

In order to prevent cells over-discharge, a watchdog timer **WDTimedBalTimer**, whose timeout is $T_{BAL\_TIMEOUT}$, is always started at the beginning of each manual balancing start command. In case the timeout expires, the balancing is stopped and the **EoBtimeerror** latch is set. FAULT line will also be triggered.

4.7.3.2 *Timed balancing mode*

The device is able to balance at the same time up to 14 cells. The balancing procedure is the following:

1. Set **Balmode = 10** in the **Bal_2** register to configure timed balancing;
2. The MCU can program up to 14 registers (**ThrTimedBalCell**xx) to assign each cell with its own balancing time duration, based on the estimation of the charge to be subtracted;
3. Set **BALxx = 10** in the **BalCell14_7act** and **BalCell6_1act** registers to enable balancing on the selected cells;
4. Set **bal_start = 1** and **bal_stop = 0** in the **Bal_1** register to start balancing.

The global **TimedBalTimer** is started and the balancing operation begins. The watchdog timer **WDTimedBalTimer** starts along with the primary one. When one of the two counters reaches the threshold designated for a cell, balancing is stopped on the involved cell.

While they start balancing at the same time, each balancing driver stops when its own time-threshold elapses. When all the balancing tasks are done, the **TimedBalTimer** is reset and the eof_bal latch is set.

The balancing timer resolution can be programmed according to the **TimedBalacc** bit:

- **TimedBalacc = 0** selects the coarse resolution: 8 min 32 sec
- **TimedBalacc = 1** selects the fine resolution: 4 sec

Table 43 lists all the available configurations for the balancing thresholds (**ThrTimedBalCell**xx).

In case GO2SLP command is received or communication timeout occurs, the behavior depends on **slp_bal_conf**:

- **slp_bal_conf = 0** means that balancing will be stopped when L9963E moves to a low power state (**Sleep** or **Cyclic Wakeup**)
- **slp_bal_conf = 1** means that L9963E moves to **Silent Balancing** state and balancing will continue.

Balancing is always stopped when moving from a low power state to **Normal**.

Table 43. Balancing threshold configuration

		TimedBalacc = 0 (coarse)	TimedBalacc = 1 (fine)
ThrTimedBalCellxx [dec]	ThrTimedBalCellxx [bin]	Threshold [hh:mm:ss]	Threshold [hh:mm:ss]
0	0000000	0:0:0	0:0:0
1	0000001	0:8:32	0:0:4
2	0000010	0:17:4	0:0:8
3	0000011	0:25:36	0:0:12
4	0000100	0:34:8	0:0:16
5	0000101	0:42:40	0:0:20
6	0000110	0:51:12	0:0:24
7	0000111	0:59:44	0:0:28
8	0001000	1:8:16	0:0:32
9	0001001	1:16:48	0:0:36
10	0001010	1:25:20	0:0:40
11	0001011	1:33:52	0:0:44
12	0001100	1:42:24	0:0:48
13	0001101	1:50:56	0:0:52
14	0001110	1:59:28	0:0:56
15	0001111	2:8:0	0:1:0
16	0010000	2:16:32	0:1:4
17	0010001	2:25:4	0:1:8
18	0010010	2:33:36	0:1:12
19	0010011	2:42:8	0:1:16
20	0010100	2:50:40	0:1:20
21	0010101	2:59:12	0:1:24
22	0010110	3:7:44	0:1:28
23	0010111	3:16:16	0:1:32
24	0011000	3:24:48	0:1:36

		TimedBalacc = 0 (coarse)	TimedBalacc = 1 (fine)
ThrTimedBalCellxx [dec]	ThrTimedBalCellxx [bin]	Threshold [hh:mm:ss]	Threshold [hh:mm:ss]
25	0011001	3:33:20	0:1:40
26	0011010	3:41:52	0:1:44
27	0011011	3:50:24	0:1:48
28	0011100	3:58:56	0:1:52
29	0011101	4:7:28	0:1:56
30	0011110	4:16:0	0:2:0
31	0011111	4:24:32	0:2:4
32	0100000	4:33:4	0:2:8
33	0100001	4:41:36	0:2:12
34	0100010	4:50:8	0:2:16
35	0100011	4:58:40	0:2:20
36	0100100	5:7:12	0:2:24
37	0100101	5:15:44	0:2:28
38	0100110	5:24:16	0:2:32
39	0100111	5:32:48	0:2:36
40	0101000	5:41:20	0:2:40
41	0101001	5:49:52	0:2:44
42	0101010	5:58:24	0:2:48
43	0101011	6:6:56	0:2:52
44	0101100	6:15:28	0:2:56
45	0101101	6:24:0	0:3:0
46	0101110	6:32:32	0:3:4
47	0101111	6:41:4	0:3:8
48	0110000	6:49:36	0:3:12
49	0110001	6:58:8	0:3:16
50	0110010	7:6:40	0:3:20
51	0110011	7:15:12	0:3:24
52	0110100	7:23:44	0:3:28
53	0110101	7:32:16	0:3:32
54	0110110	7:40:48	0:3:36
55	0110111	7:49:20	0:3:40
56	0111000	7:57:52	0:3:44
57	0111001	8:6:24	0:3:48
58	0111010	8:14:56	0:3:52
59	0111011	8:23:28	0:3:56
60	0111100	8:32:0	0:4:0
61	0111101	8:40:32	0:4:4
62	0111110	8:49:4	0:4:8
63	0111111	8:57:36	0:4:12
64	1000000	9:6:8	0:4:16

		TimedBalacc = 0 (coarse)	TimedBalacc = 1 (fine)
ThrTimedBalCellxx [dec]	ThrTimedBalCellxx [bin]	Threshold [hh:mm:ss]	Threshold [hh:mm:ss]
65	1000001	9:14:40	0:4:20
66	1000010	9:23:12	0:4:24
67	1000011	9:31:44	0:4:28
68	1000100	9:40:16	0:4:32
69	1000101	9:48:48	0:4:36
70	1000110	9:57:20	0:4:40
71	1000111	10:5:52	0:4:44
72	1001000	10:14:24	0:4:48
73	1001001	10:22:56	0:4:52
74	1001010	10:31:28	0:4:56
75	1001011	10:40:0	0:5:0
76	1001100	10:48:32	0:5:4
77	1001101	10:57:4	0:5:8
78	1001110	11:5:36	0:5:12
79	1001111	11:14:8	0:5:16
80	1010000	11:22:40	0:5:20
81	1010001	11:31:12	0:5:24
82	1010010	11:39:44	0:5:28
83	1010011	11:48:16	0:5:32
84	1010100	11:56:48	0:5:36
85	1010101	12:5:20	0:5:40
86	1010110	12:13:52	0:5:44
87	1010111	12:22:24	0:5:48
88	1011000	12:30:56	0:5:52
89	1011001	12:39:28	0:5:56
90	1011010	12:48:0	0:6:0
91	1011011	12:56:32	0:6:4
92	1011100	13:5:4	0:6:8
93	1011101	13:13:36	0:6:12
94	1011110	13:22:8	0:6:16
95	1011111	13:30:40	0:6:20
96	1100000	13:39:12	0:6:24
97	1100001	13:47:44	0:6:28
98	1100010	13:56:16	0:6:32
99	1100011	14:4:48	0:6:36
100	1100100	14:13:20	0:6:40
101	1100101	14:21:52	0:6:44
102	1100110	14:30:24	0:6:48
103	1100111	14:38:56	0:6:52
104	1101000	14:47:28	0:6:56

		TimedBalacc = 0 (coarse)	TimedBalacc = 1 (fine)
ThrTimedBalCellxx [dec]	ThrTimedBalCellxx [bin]	Threshold [hh:mm:ss]	Threshold [hh:mm:ss]
105	1101001	14:56:0	0:7:0
106	1101010	15:4:32	0:7:4
107	1101011	15:13:4	0:7:8
108	1101100	15:21:36	0:7:12
109	1101101	15:30:8	0:7:16
110	1101110	15:38:40	0:7:20
111	1101111	15:47:12	0:7:24
112	1110000	15:55:44	0:7:28
113	1110001	16:4:16	0:7:32
114	1110010	16:12:48	0:7:36
115	1110011	16:21:20	0:7:40
116	1110100	16:29:52	0:7:44
117	1110101	16:38:24	0:7:48
118	1110110	16:46:56	0:7:52
119	1110111	16:55:28	0:7:56
120	1111000	17:4:0	0:8:0
121	1111001	17:12:32	0:8:4
122	1111010	17:21:4	0:8:8
123	1111011	17:29:36	0:8:12
124	1111100	17:38:8	0:8:16
125	1111101	17:46:40	0:8:20
126	1111110	17:55:12	0:8:24
127	1111111	18:3:44	0:8:28

4.7.4 Balancing state transition

When the chip is in the NORMAL mode, the sleep conditions (communication timeout or GO2SLP command) will demand the chip entering the SLEEP or SILENT BALANCING state depending on the **slp_bal_conf**. Silent balancing is only available for **Timed Balancing mode** (**Balmode = 10** and **slp_bal_conf = 1**), while **Manual Balancing mode** (**Balmode = 01**) will be interrupted and the state transition is forced to SLEEP, regardless of **slp_bal_conf**.

If the **slp_bal_conf = 0**, whatever kind of balancing is currently being operated, it will be stopped, and then the chip will turn to the SLEEP mode.

4.7.5 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Table 44. Balancing electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BAL_OPEN}	Open load Fault Detection Voltage Threshold	Balance Power OFF (Open Load), voltage ramp on Power Drain	0.3	0.55	0.74	V
I_{PD_CB}	Output OFF Open Load Detection Pull-down Current	VDS = 5 V	100		300	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		Balance Power OFF Open Load Detect Enabled				
$I_{OUT(LKG)}$	Output Leakage Current	VDS = 5 V Balance Driver disabled (current on Sn Bn,n-1) Open Load Detect Disabled			1	µA
$I_{OUT(BAL\_OFF)}$	Output Driver Current	VDS = 5 V Balance Driver enabled but Power OFF (current on Sn, Bn,n-1) Open Load Detect Disabled	-35		5	µA
R_{DS_ON}	Drain-to-Source On Resistance	I_{OUT} = 200 mA -40 °C < T_J < 125 °C 1.8 V < Vcell(1..12) < 5 V			0.8	Ω
		I_{OUT} = 200 mA -40 °C < T_J < 125 °C 3.2 V < Vcell(13..14) < 5 V			0.8	Ω
		I_{OUT} = 200 mA 40 °C < T_J < 80 °C (production test at room) 1.8 V < Vcell(13..14) < 3.2 V			1.3	Ω
		I_{OUT} = 200 mA 80 °C < T_J < 125 °C (production test at 125 °C) 1.8 V < Vcell(13..14) < 3.2 V			1.5	Ω
I_{BAL_OC}	Over Current Short detection Current flowing through the PowerMOS when BALx_SHORT = 1	Vcell(1..14) = 5 V, Power MOS ON, current ramp on Power Drain	250			mA
V_{BAL_CLAMP}	Static clamp	I_{forced} = 300 mA	10		13	V
$V_{CELL14\_BAL\_MIN}$	Minimum voltage on cell 14 that guarantees correct operation of the balance driver	Application info			1.7	V
T_{ON_BAL}	Cell Balance Driver Turn On Time	R_L = 40 Ω (that gives a 130 mA balancing current when Vcell = 5 V) from internal command to 10% of VDS	0.5	1.8	5	µs
T_{OFF_BAL}	Cell Balance Driver Turn Off Time	R_L = 40 Ω (that gives a 130 mA balancing current when Vcell = 5 V) from internal command to 90% of VDS	0.5	4.7	15	µs
T_{BAL_OL}	Open load digital filter time	Tested by SCAN		11		ms
$T_{BAL\_OL\_HWSC}$	Digital Filter time for HWSC	Tested by SCAN		4		µs
$T_{BAL\_OVC\_DEGLITCH}$	Short Detect Glitch Filter	Tested by SCAN		61		µs
$T_{BAL\_TIMEOUT}$	Secondary Balancing Timer Timeout in Manual Mode	Tested by SCAN		600		min

4.8 Device regulators

All the internal blocks of the device are supplied by VBAT or VREG pin.

In order to optimize the power dissipation, to provide a suitable voltage for different functions or to decouple sensible from noisy blocks, different regulators are available.

4.8.1 Linear regulators

VREG

This is a linear regulator that exploits an external MOS in order to decrease the power dissipation inside L9963E. It acts as pre-regulator supplying all other internal regulatos (VANA, VCOM, VTREF and VDIG). It is switched OFF in low power modes (Sleep, Silent Balancing, OFF phase of Cyclic Wakeup). The source of the MOS is connected to VREG pin, while the gate is connected to NPNDRV pin and the drain to VBAT. VREG regulator has to be intended for L9963E use only. For the regulator external components, refer to Table 73.

VREG regulator has a dedicated UV/OV diagnostic:

- if VREG voltage goes below V_{VREG_UV} threshold for a time longer than T_{VREG_FILT} a VREG undervoltage condition is latched into **VREG_UV** flag and the bootstrap is disabled;
- if VREG voltage goes over V_{VREG_OV} threshold for a time longer than T_{VREG_FILT} a VREG overvoltage condition is latched into **VREG_OV** flag.

VANA

This low drop regulator supplies all the ADC, comparators, monitors, main bandgap, current generator and other analogic blocks. An external stabilization capacitance placed close to the pin is needed (see Table 73). VANA regulator has to be intended for L9963E use only.

VANA regulator has a dedicated UV/OV diagnostic:

- if VANA voltage goes below V_{VANA_UV} threshold for a time longer than T_{POR_FILT} a POR condition is triggered;
- if VANA voltage goes over V_{VANA_OV} threshold for a time longer than $T_{VANA\_OV\_FILT}$ a VANA overvoltage condition is latched into **VANA_OV** flag.

VANA regulator has an internal current limitation, its value is $I_{VANA\_curr\_lim}$.

VCOM

The isolated communication receiver/transmitter and the GPIO output buffers are supplied by this low drop regulator. An external stabilization capacitance placed close to the pin is needed (see Table 73).

VCOM regulator can also be used to supply external loads with I_{VCOM_ext} max. current budget.

VCOM regulator has a dedicated UV/OV diagnostic:

- if VCOM voltage goes below V_{VCOM_UV} threshold for a time longer than T_{VCOM_FILT} a VCOM undervoltage condition is latched into **VCOM_UV** flag;
- if VCOM voltage goes over V_{VCOM_OV} threshold for a time longer than T_{VCOM_FILT} a VCOM overvoltage condition is latched into **VCOM_OV** flag.

VCOM regulator has an internal current limitation, its value is $I_{VCOM\_curr\_lim}$.

VTREF

This low drop regulator is used as precise voltage reference to supply external components such as NTCs for temperature sensing. An external stabilization capacitance placed close to the pin is needed (see Table 73).

VTREF regulator has IVTREF_ext max. current budget. The recommended application circuit in **NTC Analog Front End** guarantees that each NTC channel sinks no more than 500 µA.

VTREF regulator has a dedicated UV/OV diagnostic:

- if VTREF voltage goes below V_{VTREF_UV} threshold for a time longer than T_{VTREF_FILT} a VTREF undervoltage condition is latched into **VTREF_UV** flag;
- if VTREF voltage goes over V_{VTREF_OV} threshold for a time longer than T_{VTREF_FILT} a VTREF overvoltage condition is latched into **VTREF_OV** flag.

VTREF regulator has an internal current limitation, its value is $I_{VTREF\_curr\_lim}$.

VTREF regulator is disabled by default. Its operation can be controlled via SPI according to Table 55.

VDIG

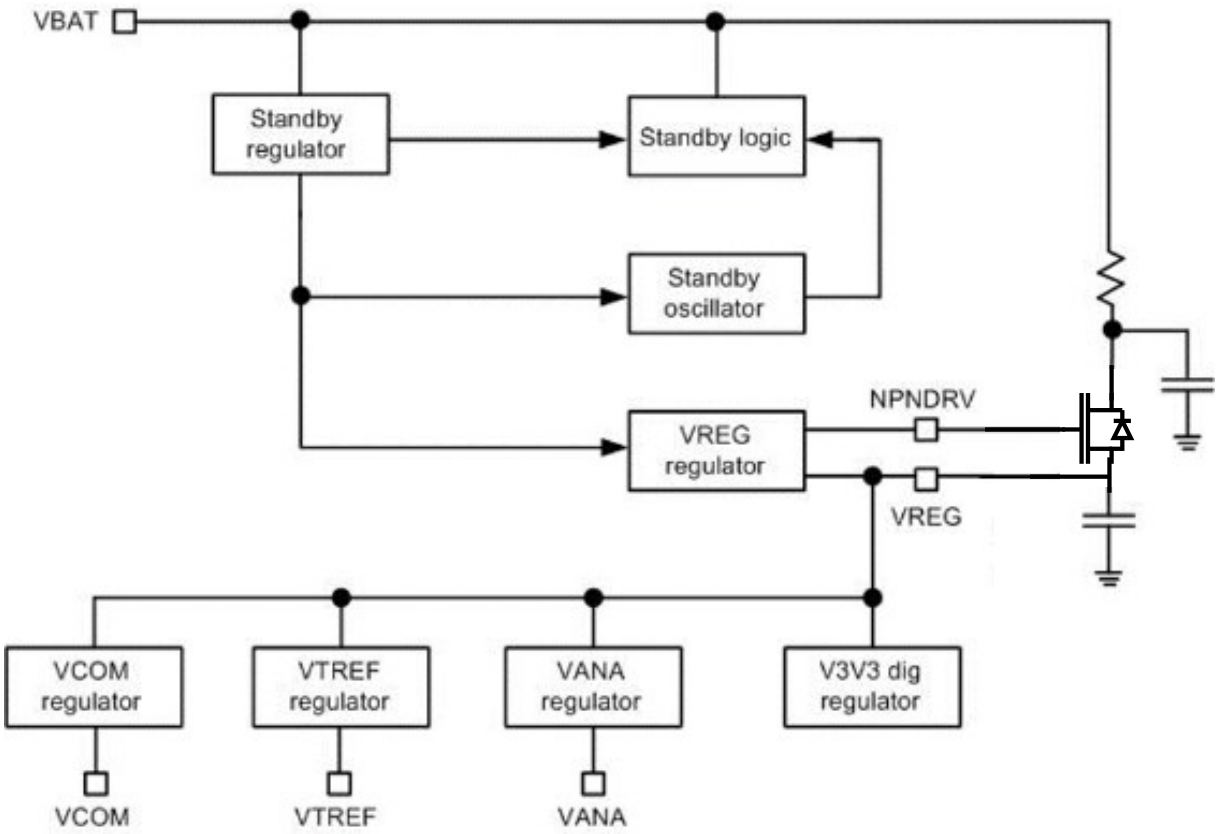
VDIG regulator has a dedicated UV/OV diagnostic:

- if VDIG voltage goes below V_{VDIG_UV} threshold for a time longer than T_{POR_FILT} a POR condition is triggered;
- if VDIG voltage goes over V_{VDIG_OV} threshold for a time longer than T_{VDIG_FILT} a VDIG overvoltage condition is latched into **VDIG_OV** flag.

For all regulators the slew rate at the power up can be evaluated considering corresponding current limitation applied on capacitance connected to related pin. The equation below estimates the startup time considering a 20% tolerance on the external stabilization capacitance (refer to Table 73). The VREG regulator implements a soft start strategy and its startup time is $T_{VREG\_SOFT\_START}$.

$$\begin{cases} T_{VCOMstart} = \frac{V_{VCOM} \times C_{VCOM}}{I_{VCOM\_curr\_lim}} = [85 - 275]\,\mu s \\ T_{VTREFstart} = \frac{V_{VTREF} \times C_{VTREF}}{I_{VTREF\_curr\_lim}} = [85 - 270]\,\mu s \\ T_{VANAstart} = \frac{V_{VANA} \times C_{VANA}}{I_{VANA\_curr\_lim}} = [65 - 260]\,\mu s \end{cases} \quad (5)$$

Figure 18. Regular scheme



4.8.2 Bootstrap

In order to provide a supply higher than VBAT to the level shifters of the ADC, a Bootstrap solution has been implemented. The Bootstrap is automatically enabled in NORMAL mode. The bootstrap works with an external capacitance C_{CB}.

Bootstrap works in 2 phases:

- during phase 1 capacitance CCB is charged between 0 V and VREG for a time long T_{RELOAD_PHASE}.
- during phase 2 the same capacitance is bootstrapped, connecting its negative terminal to VBAT. This phase longs T_{BOOT_PHASE}.

A VREG OV condition turns off bootstrap circuit.

4.8.3 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Table 45. Regulators electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{VREG}	Regulated voltage	Tested with external Iload = 10 mA/120 mA 9.6 V < VBAT < 70 V	6	6.5	7	V
$VREG_{LOAD\_TRAN}$	Transient load regulation	VBAT = 9.6/80 I = 10 mA → 120 mA	-120		120	mV
R_{PD_NPNDRV}	Pulldown resistor on NPNDRV pin	VREG regulator OFF		1		MΩ
V_{VREG_ovs}	Overshoot at power on	IVREG = 10 mA CVREG = 4.7 µF			6.8	V
$T_{VREG\_SOFT\_START}$	Soft start time	IVREG = 10 mA CVREG = 4.7 µF	100	300	500	µs
V_{VREG_UV}	Under voltage monitor		5	5.5	6	V
$V_{VREG\_UV\_HYS}$	Under voltage monitor hysteresis		100		250	mV
V_{VREG_OV}	Over voltage monitor		7	7.5	8	V
$V_{VREG\_OV\_HYS}$	Over voltage monitor hysteresis		100		250	mV
T_{VREG_FILT}	UV/OV digital filter time	Tested in SCAN	17	20	23	µs
V_{VCOM}	Regulated voltage	Tested with external Iload = 0, 10 mA 5.8 V < VREG < 7.2 V	4.8	5	5.2	V
$I_{VCOM\_curr\_lim}$	Current limitation	Measured with VCOM = 0 V	50	75	100	mA
I_{VCOM_ext}	Current budget for supplying external components	Application info			25	mA
V_{VCOM_UV}	Under voltage monitor		4.25	4.5	4.75	V
$V_{VCOM\_UV\_HYS}$	Under voltage monitor hysteresis		100		250	mV
V_{VCOM_OV}	Over voltage monitor		5.25	5.5	5.75	V
$V_{VCOM\_OV\_HYS}$	Over voltage monitor hysteresis		100		250	mV
T_{VCOM_FILT}	UV/OV filter	Tested in SCAN	17	20	23	µs
V_{VTREF}	Regulated voltage	Tested with external Iload = 0, 10 mA 5.8 V < VREG < 7.2 V	4.8	4.958	5.1	V
$V_{VTREF\_TEMP\_SPREAD}$	Maximum negative variation of VTREF in respect to the room temperature value	Tested with external Iload = 0 5.8 V < VREG < 7.2 V Guarantee by design	-12			mV
$I_{VTREF\_curr\_lim}$	Current limitation	Measured with VTREF = 0 V	50	75	100	mA
I_{VTREF_ext}	Current budget for supplying external components	Application info			50	mA
V_{VTREF_UV}	Under voltage monitor		4.25	4.5	4.75	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{VTREF\_UV\_HYS}$	Under voltage monitor hysteresis		100		250	mV
V_{VTREF_OV}	Over voltage monitor		5.25	5.5	5.75	V
$V_{VTREF\_OV\_HYS}$	Under voltage monitor hysteresis		100		250	mV
T_{VTREF_FILT}	UV/OV filter	Tested in SCAN	17	20	23	µs
V_{ANA}	Regulated voltage	Tested with external Iload = 0, 10 mA 5.8 V < VREG < 7.2 V	3.15	3.3	3.45	V
$I_{VANA\_curr\_lim}$	Current limitation	Measured with VANA = 2.5 V	35	60	85	mA
V_{VANA_UV}	Under voltage monitor		2.6	2.75	2.9	V
$V_{VANA\_UV\_HYS}$	Under voltage monitor hysteresis		50		150	mV
V_{VANA_OV}	Over voltage monitor		3.6		4	V
$V_{VANA\_OV\_HYS}$	Over voltage monitor hysteresis		50		200	mV
$T_{VANA\_OV\_FILT}$	VANA Over voltage filter time	Tested in SCAN	17	20	23	µs
$V_{VANA\_POR\_LH}$	Power on reset going out of POR		2.7	2.85	3	V
$V_{VANA\_POR\_HL}$	Power on reset going into POR		2.6	2.75	2.9	V
$V_{VANA\_POR\_HYS}$	POR monitor hysteresis		50		150	mV
V_{DIG}	Regulated voltage	Tested with external Iload = 0 5.8 V < VREG < 7.2 V	3.15	3.3	3.45	V
V_{VDIG_UV}	Under voltage monitor		2.6	2.75	2.9	V
$V_{VDIG\_UV\_HYS}$	Under voltage monitor hysteresis		50		150	mV
V_{VDIG_OV}	Over voltage monitor		3.6		4	V
$V_{VDIG\_OV\_HYS}$	Under voltage monitor hysteresis		50		200	mV
T_{VDIG_FILT}	UV/OV filter	Tested in SCAN	17	20	23	µs
T_{POR_FILT}	Power on reset filter		4		16	µs
$T_{POR\_FILT\_LH}$			2.5		7.5	µs
V_{BOOT}	CAP2 voltage during bootstrap phase		VBAT+2.5 V + 840 mV (840 mV = 6.5 mA*128 µs/1 µF) Design info			V
T_{BOOT_PHASE}	Bootstrap phase duration	Tested in SCAN		128		µs
T_{RELOAD_PHASE}	Bootstrap reload phase duration	Tested in SCAN		17		µs
I_{VBOOT_CURR}	Bootstrap charge current for external cap	Bootstrap charge phase, CAP1 = 2 V, measured sinked current between CAP1 and GND	30	65	100	mA
C_{CB}	External capacitance between CAP1 and CAP2 pins	Application info	0.7	1	1.3	µF
$T_{GND\_LOSS\_filter}$	GND loss digital filter time	Tested in SCAN		300		µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
GND_LOSS_THR	GND loss analog threshold		100	300	450	mV

4.9 General purpose I/O: GPIOs

L9963E provides 9 GPIOs which can be individually configured as digital I/Os or analog I/Os according to the following configuration:

Table 46. GPIO port configuration

GPIO port	Digital				Analog
	Std. GPIO	SPI	Wake up	FAULT	Absolute input
1	X			X	
2	X			X	
3	X				X
4	X				X
5	X				X
6	X				X
7	X		X		X
8	X	X			X
9	X	X			X

Note: 'X' means the option is available.

GPIO default configuration depends on the device operating mode:

Table 47. GPIO default configuration

GPIO	Type	SPIEN = 1	SPIEN = 0
GPIO1_FAULTH	Read Only	Digital Input(1)	
GPIO2_FAULTL	Read Only	Digital Output(1)	
GPIO3	Read/Write	Analog Input	
GPIO4	Read/Write	Analog Input	
GPIO5	Read/Write	Analog Input	
GPIO6	Read/Write	Analog Input	
GPIO7_WAKEUP	Read/Write	Digital Input	
GPIO8_SCK	Read/Write conditioned	Digital Input(1)	Analog Input
GPIO9_SDO	Read/Write conditioned	Digital Output(1)	Analog Input

1. *Configuration is locked and cannot be changed by MCU.*

4.9.1 GPIO3-9: absolute analog inputs

Seven GPIOs (from GPIO3 to GPIO9) can be used as analog inputs. They can be converted during the **Voltage conversion routine**.

This configuration is usually implemented in order to monitor external Negative Temperature Coefficient (NTCs). Refer to Section 6.9 NTC analog front end for the application circuit.

The buffered regulator output VTREF is used to bias up to 7 NTC probes.

Depending on the measurement strategy selected via **ratio_abs_x_sel** bit, two decoding formulas apply:

GPIO measurement formula

$$\begin{cases} V_{GPIO} = BINARY\_CODE * V_{GPIO\_ABS\_RES}, & if\ ratio\_abs\_x\_sel = 0 \\ \frac{V_{GPIO}}{V_{TREF}} = BINARY\_CODE * V_{GPIO\_RATIO\_RES}, & if\ ratio\_abs\_x\_sel = 1 \end{cases} \quad (6)$$

ADCs integrity is checked by **Cell open with ADC_CROSS_CHECK = 1** and **Voltage ADC BIST**.

To cover latent failures, MCU can check if the divider is working properly by toggling the **ratio_abs_x_sel** bit:

1. MCU performs a GPIO conversion with **ratio_abs_x_sel = 0** (absolute measurement)
2. MCU manually evaluates the quantity **GPIOx_MEAS / VTREF_MEAS**
3. MCU switches to **ratio_abs_x_sel = 1** (ratiometric measurement)
4. MCU reads the ratiometric quantity in the **GPIOx_MEAS** registers and verifies that it matches the one evaluated at point 2.

Note: When toggling ratio_abs_x_sel bit, OT/UT and fast charge OT thresholds are not automatically updated, since they are supposed to be written by the MCU. Hence, unwanted failures might be flagged. For this reason, it is recommended to perform the divider integrity check at system startup.

4.9.2 GPIO1-9: standard digital I/O

The GPIO can be used in a standard digital input (Schmitt trigger) or digital Output buffer configuration, depending on the configuration defined by dedicated register.

4.9.3 GPIO8-9: SPI commands

When the L9963E is connected to the micro (bottom device of the chain, SPIEN pin connected to the 5 V LDO of the microcontroller), these two of the GPIO pins are used as SPI digital pins (the other 2 pins needed for SPI communication are ISOLP/M pins):

- ISOLM:CS (chip select) INPUT
- ISOLP: SDI (serial data in) INPUT
- GPIO8: SCLK (serial clock) INPUT
- GPIO9: SDO (serial data out) BUFFERED OUTPUT

4.9.4 GPIO7: wake up feature

To enable GPIO7 as wakeup source, it must be configured as digital input (**GPIO7_CONFIG = 10**) and the **GPIO7_WUP_EN** bit must be set to '1':

- Driving GPIO7 high for longer than TGPIO7_WAKEUP moves L9963E from a low power state to normal mode.
- A high logic value on GPIO7 pin keeps the device awake, also in case a GO2SLP command is received or communication timeout expires.
- In order to move the device to a low power state, the GPIO7 must be driven low and either a GO2SLP command must be issued or the communication timeout has to expire.

4.9.5 GPIO1-2: FAULT feature

The fault information is transmitted in the chain by optocouplers connected to GPIO pins. The L9963E senses the FAULT signal incoming from an upper device on **GPIO1_FAULTH** pin: external components must guarantee that the voltage on the FAULTH pin lays inside the operating range. The L9963E transmits the fault signal to the bottom of the chain through **GPIO2_FAULTL** pin that drives the optocoupler. External components must limit the current coming out from GPIO2 pin when a logic '1' is passed.

The FAULTL pin of the device at the bottom of the stack can be directly connected to the MCU digital input to connect a fault interrupt.

For further information about FAULT line, refer to Section 4.3 FAULT line.

Refer to Section 6.7 FAULT line circuit for the application circuit.

4.9.6 Electrial parameters

4.9.6.1 Analog input

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Table 48. GPIO electrical parameters for analog input configuration

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{GPIOAN}	GPIO Analog Voltage Input Measurement Range(1)	Design info Valid for GPIO3-9	0.1		5	V
$V_{GPIO\_ABS\_RES}$	GPIO Analog Voltage Input Measurement Resolution, when **ratio_abs_x_sel = 0**	Application Info, same as $V_{CELLRES}$		89		µV
$V_{GPIO\_RATIO\_RES}$	GPIO Analog Voltage Input Measurement Resolution, when **ratio_abs_x_sel = 1**	Application Info		2^{-16}		-
I_{OUT_HIZ}	Analog Input leakage current	Output buffer in tristate 0 < V_{GPIO} < VCOM – 0.5 V	-0.5		0.5	µA
$V_{GPIOANERR0}$	Accuracy VBAT = C14 C0 = GND	0.1 V ≤ V_{CELL} < 0.3 V -40 °C < T_J < 125 °C	-10		10	mV
$V_{GPIOANERR1}$		0.3 V ≤ V_{CELL} < 0.5 V -40 °C < T_J < 125 °C	-5		5	mV
$V_{GPIOANERR2}$		0.5 V ≤ V_{CELL} ≤ 5 V 105 °C < T_J < -125 °C	-7		7	mV
$V_{GPIOANERR3}$		0.5 V ≤ V_{CELL} < 3.2 V -40 °C < T_J < 105 °C	-2		2	mV
$V_{GPIOANERR4}$		3.2 V ≤ V_{CELL} ≤ 4.3 V -40 °C < T_J < 105 °C	-2.4		2.4	mV
$V_{GPIOANERR5}$		4.3 V ≤ V_{CELL} ≤ 4.7 V -40 °C < T_J < 105 °C	-2.6		2.6	mV
$V_{GPIOANERR6}$		4.7 V ≤ V_{CELL} ≤ 5 V -40 °C < T_J < 105 °C	-6		6	mV
$V_{GPIOANERR0}$	Accuracy + Drift VBAT = C14 C0 = GND Noise contribution is V_{CELL_NOISE1}	0.1 V ≤ V_{GPIO} < 0.3 V -40 °C < T_J < 125 °C	-10		10	mV
$V_{GPIOANERR1}$		0.3 V ≤ V_{GPIO} < 0.5 V -40 °C < T_J < 125 °C	-5		5	mV
$V_{GPIOANERR2}$		0.5 V ≤ V_{GPIO} ≤ 5 V 105 °C < T_J < -125 °C	-8		8	mV

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{GPIOANERR3}$	Accuracy + Drift VBAT = C14 C0 = GND Noise contribution is V_{CELL_NOISE1}	0.5 V ≤ V_{GPIO} < 3.2 V -40 °C < T_J < 105 °C	-2.4		2.4	mV
$V_{GPIOANERR4}$		3.2 V ≤ V_{GPIO} ≤ 4.3 V -40 °C < T_J < 105 °C	-3		3	mV
$V_{GPIOANERR5}$		4.3 V ≤ V_{GPIO} ≤ 4.7 V -40 °C < T_J < 105 °C	-3.6		3.6	mV
$V_{GPIOANERR5}$		4.7 V ≤ V_{GPIO} ≤ 5 V -40 °C < T_J < 105 °C	-7		7	mV
V_{GPIOAN_UT}	GPIO Analog Input Over-voltage Fault Threshold(2) **GPIO_UT_TH**	Application info Used for NTC UT failure detection on GPIO3-9 Tested by SCAN	0.1		5	V
$V_{GPIOAN\_UT\_RES}$	GPIO Analog Voltage Input Over-voltage Fault Threshold Resolution(2) Valid when **ratio_abs_x_sel = 0**	Design info Valid for GPIO3-9		11.392		mV
$V_{GPIOAN\_UT\_RATIO\_RES}$	GPIO Analog Voltage Input Over-voltage Fault Threshold Resolution(2) Valid when **ratio_abs_x_sel = 1**	Application info, valid for GPIO3-9		2^{-9}		-
V_{GPIOAN_OT}	GPIO Analog Input Under-voltage Fault Threshold(2) **GPIO_OT_TH**	Application info Used for NTC OT failure detection on GPIO3-9 Tested by SCAN	0.1		5	V
$V_{GPIOAN\_OT\_RES}$	GPIO Analog Voltage Input Under-voltage Fault Threshold Resolution(2) Valid when **ratio_abs_x_sel = 0**	Design info Valid for GPIO3-9		11.392		mV
$V_{GPIOAN\_OT\_RATIO\_RES}$	GPIO Analog Voltage Input Under-voltage Fault Threshold Resolution(2) Valid when **ratio_abs_x_sel = 1**	Application info, valid for GPIO3-9		2_{-9}		-
$V_{GPIO\_FASTCH\_OT\_DELTA}$	GPIO Analog Input Fast charge Fault Threshold **Gpio_fastchg_OT_delta_thr**	Design info, tested by SCAN Valid for GPIO3-9	0		5	V
$V_{GPIO\_FASTCH\_OT\_DELTA\_RES}$	GPIO Analog Voltage Input Fast Charge Under-voltage Fault Threshold Resolution(2) Valid when **ratio_abs_x_sel = 0**	Design info, tested by SCAN Valid for GPIO3-9		22.784		mV
$V_{GPIO\_FASTCH\_OT\_DELTA\_RATIO\_RES}$	GPIO Analog Voltage Input Fast Charge Under-voltage Fault Threshold Resolution(2) Valid when **ratio_abs_x_sel = 1**	Application info, tested by SCAN Valid for GPIO3-9		2^{-8}		-
V_{GPIO_OL}	Open load voltage threshold	Covered by SCAN Valid for GPIO3-9		200		mV
$I_{GPIO\_PD\_OPEN}$	Open load pulldown current		10		40	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{GPIO\_OPEN\_SET}$	Open load diagnostics settling time	Tested in SCAN		0.7		ms

1. *The measurement range and accuracy are the same of these for cell voltage.The GPIO readout is done in a time frame non-overlapping with the readout of Cell voltage.*
2. *When the GPIO ports are used for temperature measurement, the OV/UV detection can be used for OT/UT (under voltage → over-temperature, over voltage → under-temperature).*

4.9.6.2 *Digital input*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Table 49. Electrical parameters for GPIOs as digital inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN_L}	Low input level	Slow rising ramp on GPIO	0		1.4	V
V_{IN_H}	High input level	Slow falling ramp on GPIO	1.3		VCOM	V
V_{IN_HYS}	Input hysteresis	Calculation VIN_H-VIN_L	0.15		0.4	V

4.9.6.3 *Digital output*

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

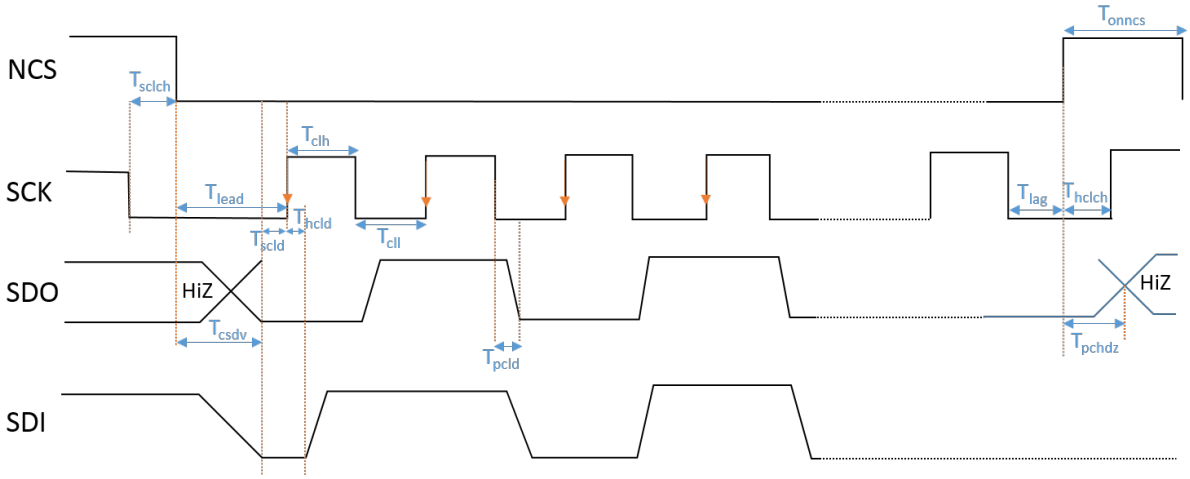
Table 50. GPIO digital output electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OUT_L}	GPIO1..9 Low output level	IGPIO = 2 mA	0		0.4	V
V_{OUT_H}	GPIO1..9 High output level	IGPIO = -2 mA	VCOM-0.4		VCOM	V
T_{OUT_trans9}	GPIO9 Rise and Fall time	Cload=120pF 20-80% on rising edge of VGPIO 80-20% on falling edge of VGPIO	5		35	ns
T_{OUT_trans}	GPIO1..8 Rise and Fall time	Cload = 120 pF 20-80% on rising edge of VGPIO 80-20% on falling edge of VGPIO	5		400	ns
$T_{FILT\_GPIO\_ECHO}$	GPIO1..9 short fault digital filter time	Tested in SCAN		2		µs

4.9.6.4 *SPI specification*

L9963E implements an SPI slave with the following timing requirements:

Figure 19. **SPI timing diagram**



All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Table 51. **SPI electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{cll}	Minimum time CLK = LOW	Application info	75			ns
T_{clh}	Minimum time CLK = HIGH	Application info	75			ns
T_{pcld}	Propagation delay (SCLK to data at SDO active)	Cload = 30 pF Valid for GPIO9			50	ns
T_{lead}	CLK change L/H after NCS = low	Application info	75			ns
T_{scld}	SDI input setup time (CLK change H/L after SDI data valid)	Application info	15			ns
T_{hcld}	SDI input hold time (SDI data hold after CLK change H/L)	Application info	15			ns
T_{sclch}	CLK low before NCS low	Application info	75			ns
T_{lag}	CLK low before NCS high	Application info	100			ns
T_{hclch}	CLK high after NCS high	Application info	100			ns
T_{onncs}	NCS min high time	Application info	300			ns
T_{pchdz}	NCS L/H to SDO @ high impedance	Cload = 30 pF Valid for GPIO9			75	ns
T_{csdv}	NCS H/L to SDO active	Cload = 30 pF Valid for GPIO9			90	ns
F_{CLK_SPI}	CLK frequency (50% duty cycle)	Application info	0.5		5	MHz
T_{SPI_ERR}		Tested by SCAN		5		ms
$R_{PULLDOWN\_SPIEN}$	Pulldown resistance on SPIEN pin		50		150	kΩ

4.10 Internal Non Volatile Memory (NVM)

L9963E offers the possibility to store pack ID and other sensitive data in the internal NVM, up to NNVM_SIZE bit. Three operations are available:

- **NVM Read**: this operation downloads the NVM content into RAM. This function populates **NVM_RD_x** and **NVM_CNTR** registers with the NVM content. Also trimming and calibration data will be re-downloaded.
- **NVM Write**: this operation pushes the RAM content into NVM. This function writes the NVM internal sub-sectors fetching the data from **NVM_WR_x** and **NVM_CNTR** registers. Such a procedure does not involve trimming and calibration data sectors. Since write operation is only capable of writing 'ones' and it cannot write 'zeroes', before executing a Write operation, the NVM must be erased first. A maximum of NNVM_MAX_WRITE write cycles is allowed.
- **NVM Erase**: this operation erases the NVM content, resetting all sub-sectors corresponding to **NVM_RD_x** and **NVM_CNTR** registers to '0x0'. Such a procedure does not involve trimming and calibration data sectors. After an Erase operation, only the Write operation is allowed.

The NVM must be operated in the following way: first Erase, then Write, then Read.

4.10.1 NVM read

To read the updated NVM content, simply re-trigger the NVM download performing the following procedure:

1. Set **trimming_retrigger = '1'**
2. Wait for $\mathbf{T_{NVM\_OP}}$
3. Set **trimming_retrigger = '0'**

NVM_RD_x and **NVM_CNTR** registers are now populated with the updated data downloaded from NVM. The whole NVM content, including user data, is checked against CRC upon download. In case of errors in the user sectors, the **EEPROM_CRC_ERR_CAL_RAM** flag will be set.

*Note: NVM_WR_BUSY flag is not set during read operation. Do not perform Read operation after Erase (refer to **NVM Erase**).*

4.10.2 NVM erase

To erase the NVM content corresponding to **NVM_RD_x** registers, follow this procedure:

1. Program **NVM_OPER = 10** and **NVM_PROGRAM = 1** to set Erase mode
2. Write first unlock key **NVM_UNLOCK_START = 0x1572F**
3. Write second unlock key **NVM_UNLOCK_START = 0x1602F**
4. Wait **TNVM_OP** (during wait time, the flag **NVM_WR_BUSY = 1**)
5. Check **NVM_WR_BUSY = 0**, indicating the operation has been successfully accomplished
6. Set **NVM_PROGRAM = 0**

After an erase, it is mandatory to perform **NVM Write** operation in order to bring the internal NVM registers to a defined state.

*Note: Read operation after an Erase is strictly forbidden. It will result in populating the RAM with randomic values, including the **NVM_CNTR**. In case NVM_CNTR results greater than NNVM_MAX_WRITE, the memory will be locked and no further erase/write will be possible.*

4.10.3 NVM write

To update the NVM content corresponding to **NVM_RD_x** registers with new data, follow this procedure:

1. Write the desired data into **NVM_WR_x** registers (all registers have to be populated; it is not possible to write just a selected bunch of registers). Make sure the NVM_WR_x registers are populated with the desired data by reading back the answers incoming from L9963E
2. Program **NVM_OPER = 11** and **NVM_PROGRAM = 1** to set Write mode
3. Write first unlock key **NVM_UNLOCK_START = 0x1572F**
4. Write second unlock key **NVM_UNLOCK_START = 0x1602F**
5. Wait **TNVM_OP** (during wait time, the flag **NVM_WR_BUSY = 1**)
6. Check **NVM_WR_BUSY = 0**, indicating the operation has been successfully accomplished
7. Set **NVM_PROGRAM = 0**

*Note: Remember to perform **NVM Erase** before executing a Write operation. The Write operation actually writes only 'ones' and is not capable of writing 'zeroes'. To see the effects of Write, the **NVM_RD_x** and **NVM_CNTR** registers have to be refreshed by re-downloading the NVM content via **NVM Read** procedure.*

Each writing operation increments the **NVM_CNTR** counter by '1'. In case **NVM_CNTR** saturates to NNVM_MAX_WRITE, writing operations are inhibited. User software shall inhibit any further Erase action in order to avoid counter reset. Only reading operations are possible.

4.10.4 Electrical parameters

Table 52. NVM electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
N_{NVM_SIZE}	NVM size allocated for external use	Design info			112	bit
T_{NVM_OP}	Time interval required to perform each NVM operation.	Tested by SCAN			10	ms
$N_{NVM\_MAX\_WRITE}$	Maximum number of NVM writing operations allowed.	Design info			32	Write cycles

4.11 Safety and diagnostic features

L9963E provides an extended set of safety mechanisms to reach the required ASIL (Automotive Safety Integrity Level) standard. Several diagnostics and integrity checks have been implemented. Faults can be notified in a redundant way to the MCU: **Global Status Word (GSW)** allows failure notification over daisy chain communication lines, while **FAULT Line** exploits a second independent pair. Every detected failure is available in SPI registers.

4.11.1 Cell UV/OV diagnostic

It is possible to select the value for the Overvoltage threshold (VCELL_OV) as well as for the Undervoltage threshold (V_{CELL_UV}) of the cells.

It is also possible to specify an increment ($V_{CELL\_BAL\_UV\_\Delta}$) with respect to the undervoltage threshold V_{CELL_UV}. Such an increment will determine the position of the balance Undervoltage threshold ($V_{BAL\_UV\_TH}$). Such a failure can be masked through dedicated SPI bit. The actual balance undervoltage threshold will be placed according to the following formula:

$$V_{BAL\_UV\_TH} = V_{CELL\_UV} + V_{CELL\_BAL\_UV} \quad (7)$$

This diagnostic feature is completed by analyzing, inside the logic block, the digital information provided by the Voltage measurement ADCs. Measurements will be performed just on enabled cells.

In case of cell UV/OV ($V_{CELL\_OV/UV}$):

- Corresponding fault flag is set and latched into **VCELL_OV** / **VCELL_UV** register
- Fault is propagated through the **FAULT Line**
- Balance is stopped in case of UV event
  - A cell UV causes the balance activity to be stopped on the whole cell stack
  - A cell balance UV causes the balance activity to be stopped only on the affected cell
- Conversion routine goes into **Configuration Override**

Balance UV ($V_{BAL\_UV\_TH}$) fault can be masked via **VCELLx_BAL_UV_MSK** bit. When masking is activated:

- Fault is not propagated through the **FAULT Line**
- Conversion routine doesn't go into **Configuration Override**
- **VCELLx_BAL_UV** SPI flag is not set

4.11.2 Total battery VBAT diagnostic

The total stack voltage diagnostic is implemented through three different safety mechanisms:

- Arithmetic sum of the digital information of cell ADC (within the **Cell Conversion** step of the **Voltage Conversion Routine**): V_{BATT_SUM}, stored in **Vsum_batt(19:0)**. Such a value is then compared to the digital thresholds $V_{BAT\_OV\ (SUM)}$ or $V_{BAT\_UV\ (SUM)}$ (programmable via the **VBATT_SUM_OV_TH** and **VBATT_SUM_UV_TH** registers). This diagnostic is intended to catch stack undervoltage and overvoltage events with a high precision.

- Direct conversion of the voltage $V_{BATT\_MONITOR}$ at VBAT pin through internal resistive divider (within the **VBAT Conversion** step of the **Voltage Conversion Routine**). The result is compared to the $V_{BAT\_CRITICAL\_OV\_TH}$ or $V_{BAT\_CRITICAL\_UV\_TH}$ fixed thresholds. This diagnostic is mainly intended to protect the IC against AMR violation on VBAT pin. It can also be used as a redundant coherency check with the arithmetic sum of cells.
- Continuous sense of the VBAT pin voltage with a $V_{BAT\_UV/OV}$ comparator, featuring fixed thresholds ($V_{BAT\_OV\_WARNING\ (COMP)}$ and $V_{BAT\_UV\_WARNING\ (COMP)}$). It is used as an “over voltage warning” or an “under voltage warning”. This diagnostic is intended to provide a fast reaction against transient overvoltage and undervoltage events.

This UV/OV comparator is always enabled in order to guarantee a continuous safety check on VBAT voltage.

Refer to Table 40 for the electrical parameters.

4.11.2.1 *VBAT over-voltage*

The aim of this diagnostic is to detect a dangerous increase of battery voltage in order to protect the circuitry connected to VBAT.

If VBAT > $V_{BAT\_OV\_WARNING\ (COMP)}$ (for a time longer than T_{VBAT_FILT}) or V_{BATT_SUM} > $V_{BAT\_OV\ (SUM)}$ or $V_{BATT\_MONITOR}$ > $V_{BAT\_CRITICAL\_OV\_TH}$ the over-voltage fault is directly reported in registers and notified to the microcontroller with 3 dedicated flags, according to the Fault communication procedure.

In case of VBAT overvoltage detection during voltage conversion routine (violation of $V_{BAT\_OV\ (SUM)}$ or $V_{BAT\_CRITICAL\_OV\_TH}$):

- Corresponding fault flag is set and latched into register **VSUM_OV** or **VBATTCRIT_OV**
- Fault is propagated through the **FAULT Line**
- Voltage conversion routine goes into **Configuration Override**

In case of VBAT overvoltage detection through the analog comparator ($V_{BAT\_OV\_WARNING}$):

- Corresponding fault flag is set and latched into register **VBATT_WRN_OV**
- Fault is propagated through the **FAULT Line**
- Voltage conversion routine is not involved, since this diagnostic is not part of the routine steps

For further details see Section 4.12 Voltage conversion routine.

4.11.2.2 *VBAT under-voltage*

The aim of this diagnostic is to detect a decrease of battery voltage in order to notify this fault that may cause system malfunctions.

If VBAT < $V_{BAT\_UV\_WARNING\ (COMP)}$ (for a time longer than T_{VBAT_FILT}) or V_{BATT_SUM} < $V_{BAT\_UV\ (SUM)}$ or $V_{BATT\_MONITOR}$ < $V_{BAT\_CRITICAL\_UV\_TH}$ the under-voltage fault is reported in the register and notified to the microcontroller with 3 dedicated flags, according to the Fault communication procedure.

In case of VBAT undervoltage detection during voltage conversion routine (violation of $V_{BAT\_UV\ (SUM)}$ or $V_{BAT\_CRITICAL\_UV\_TH}$):

- Corresponding fault flag is set and latched into register **VSUM_UV** or **VBATTCRIT_UV**
- Fault is propagated through the **FAULT Line**
- Balance is stopped on the whole stack
- Voltage conversion routine goes into **Configuration Override**

In case of VBAT undervoltage detection through the analog comparator ($V_{BAT\_UV\_WARNING}$):

- Corresponding fault flag is set and latched into register **VBATT_WRN_UV**
- Fault is propagated through the **FAULT Line**
- Voltage conversion routine is not involved, since this diagnostic is not part of the routine steps

In case of VBAT pin loss, the internal resistive divider will pull-down VBAT to GND, thus causing VBAT UV failure and, eventually, POR.

For further details see Section 4.12 Voltage conversion routine.

4.11.3 Cell open wire diagnostic

The cell open detection can be performed through the **Voltage Conversion Routine** and it has been studied to address several safety issues. Diagnostic strategy depends on the **ADC_CROSS_CHECK** bit.

4.11.3.1 Cell open with ADC_CROSS_CHECK = 0

If the **Cell Terminal Diagnostics** step of the **Voltage Conversion Routine** is executed having programmed **ADC_CROSS_CHECK = 0**, then the diagnostic addresses the following failures:

- RLPF degradation: diagnostic has been implemented to guarantee that low pass filter resistor in series to the Cx pin is below the critical limit R_{LPF_OPEN}
  - On odd cells, RLPF degradation will cause the assertion of the corresponding CELLx_OPEN flag
  - On even cells, flag assertion depends on the RLPF degradation
    - A small degradation (RLPF < 24 kΩ typ. with 10 nF CLPF) will only cause the assertion of the corresponding CELLx_OPEN flag
    - A huge degradation (RLPF > 24 kΩ typ. with 10 nF CLPF) will cause the assertion of both the corresponding CELLx_OPEN flag and the lower odd cell CELLx-1_OPEN flag
- L9963E C1-C14 pin open
- L9963E C0 pin open or PCB connector open

Diagnostic is present just on enabled cells (**VCELLx_EN = 1**).

The mechanism used for this detection is based on a diagnostic pull down current ($I_{OPEN\_DIAG\_CX}$), which allows to measure the voltage drop generated on the external RLPF resistance connected in series to Cx pin. If such a voltage drop is higher than V_{CxOPEN} threshold a Cx open connection is detected.

C0 open diagnostic is performed with a pullup current ($I_{OPEN\_DIAG\_C0}$) instead of a pulldown. A dedicated comparator senses C0 pin voltage and compares it with V_{CxOPEN}. In case V(C0) > V_{CxOPEN}, open detection occurs.

In case of failure detection on an enabled cell:

- Corresponding fault flag is set and latched into **CELLx_OPEN** register;
- Fault is propagated through the **FAULT Line**;
- Voltage conversion routine goes into **Configuration Override**.

For further details see Section 4.12 Voltage conversion routine.

4.11.3.2 Cell open with ADC_CROSS_CHECK = 1

If the **Cell Terminal Diagnostics** step of the **Voltage Conversion Routine** is executed having programmed **ADC_CROSS_CHECK = 1**, then the diagnostic addresses the following issues:

- Failure in the filtering capacitor CLPF causing an excessive leakage from cell;
- ADC error due to bandgap shift or failure on the conversion path.

The mechanism used for this detection is the same as **Cell open with ADC_CROSS_CHECK = 0**, except that no pull-down current is sunk from Cx pin.

For each pair of consecutive cells, the two corresponding ADCs, each of whom is referenced to a different bandgap, are measuring the voltage drop on the external RLPF.

Since no pull-down current is applied while measurement is on going, the voltage drop on RLPF is expected to be null, and the two measurement results should match.

If one of the two ADCs is experiencing an issue, or an excessive leakage from the CLPF is causing a voltage drop on the RLPF, a mismatch in the results occurs. If such a mismatch is greater than $V_{ADC\_CROSS\_FAIL}$, failure is detected.

In case of failure detection on an enabled cell:

- The **CELLx_OPEN** fault latch will be set for both cells belonging to the pair that failed;
- Fault is propagated through the **FAULT Line**;
- Voltage conversion routine goes into **Configuration Override**.

For further details see Section 4.12 Voltage conversion routine.

4.11.4 ADC swap

Failures on the ADCs can be detected by the **HardWare Self-Check (HWSC)** step of the **Voltage Conversion Routine**.

L9963E provides the means to operate a limp home functionality. For each pair of cells, in case one of the two independent ADC fails, it is still possible to perform a swap of the input MUX, in order to allow the remaining ADC measuring both cells.

User FW may activate, by means of **CROSS_ODD_EVEN_CELL**, a swap between the two ADCs of a cell pair, in order to measure even cells through ADCs dedicated to the odd cells, and vice versa. For instance, if the ADC assigned to cell Cx (even) fails, the adjacent one assigned to cell Cx-1 (odd) can be exploited to implement the limp home functionality.

Since one ADC has failed, it is not possible to perform a complete scan of the cells in a single measurement cycle. User SW must switch to the limp home routine where each scan requires two **On-Demand Conversions**:

- The first iteration will be executed having set **CROSS_ODD_EVEN_CELL = 0** (default)
  - ADCx measures cell Cx → MCU must discard the result, since ADCx is broken
  - ADCx-1 measures cell Cx-1 → Result is good
- The second iteration will be executed having set **CROSS_ODD_EVEN_CELL = 1** (swap mode)
  - ADCx measures cell Cx-1 → MCU must discard the result, since ADCx is broken
  - ADCx-1 measures cell Cx → Result is good

MCU then merges the results of the first and second iteration to obtain a set of 14 reliable values, that can be used to:

- Detect an UV/OV on cells (comparison with threshold must be made by user FW)
- Get an accurate conversion of cells even if in case of fault on a ADC. This makes State Of Charge estimation still possible
- Perform total stack voltage measurement as the sum of cells

When in limp home mode, all the ADC based diagnostics are not guaranteed. Fault tolerant time requirements can still be met by doubling the sample rate (e.g. switching from 100 ms to 50 ms sample time).

4.11.5 PCB open diagnostic

To detect loss of cell wire at PCB connector, the following procedure must be executed:

1. Convert even cells with an on-demand conversion.
2. Enable the diagnostic current (I_{PD_CB}) on even cells by programming **PCB_open_en_even_curr = 1**.
3. Wait for a proper settling time T_{PCB_SET}, whose minimum value and the minimum settling time can be estimated according to the following equation:

$$T_{PCB\_SET} = \frac{\Delta V_{PCBmax}}{I_{PD\_CBmin}} \times 2C_{LPF} = (e.g. \quad (8)$$

$$)\frac{1V}{100\mu A} \times 2 \times 10nF = 200\mu s$$

   Choosing T_{PCB_SET} = **T_{CxOPEN_SET}** is enough if using **$T_{CYCLEADC\_000}$** filter option to convert cells at step 1. In general, the settling time T_{PCB_SET} should be longer than **T_{SAMPLE_MIN}** in Table 38.
4. Convert even cells with an on-demand conversion.
5. Disable the diagnostic current (I_{PD_CB}) on even cells by programming **PCB_open_en_even_curr = 0**.
6. For each cell, evaluate the difference between conversion at step 1 and step 4. If higher than a defined threshold V_{PCB_DIFF}, the PCB connection to the cell is degraded. The open resistance depends on V_{PCB_DIFF} according to the following equation:

   PCB open resistance evaluation

$$R_{PCB\_OPEN} = \frac{V_{PCB\_DIFF}}{I_{PD\_CB}} \quad (9)$$

   For instance, setting V_{PCB_DIFF} = 40 mV allows detecting R_{PCB_OPEN} in the [133-400] Ω range.
7. Repeat all the previous steps for odd cells, using **PCB_open_en_odd_curr** to manage the diagnostic current.

*Note: When performing PCB open diagnostic, other diagnostics such as **Cell UV/OV diagnostic** and **Balancing open load diagnostic** might also be triggered. They must be then discarded by user SW.*

4.11.6 Voltage ADC BIST

Besides **Cell open with ADC_CROSS_CHECK = 1**, the **HardWare Self-Check (HWSC)** step of the **Voltage Conversion Routine** covers all the additional conversion paths, such as VTREF, GPIOs configured as analog input and VBAT resistive divider. As a redundant mechanism, it also covers conversion paths involving Cx pins.

If BIST result is not aligned to expectations:

- Corresponding fault flag is set and latched into register **MUX_BIST_FAIL** or **OPEN_BIST_FAIL** or **GPIO_BIST_FAIL**
- Fault is propagated through the **FAULT Line**
- Balance is stopped
- Voltage conversion routine goes into **Configuration Override**

For further details see Section 4.12 Voltage conversion routine.

4.11.7 Die temperature diagnostic and over temperature

An internal temperature sensor continuously monitors the temperature of the chip: measurement result is available in the **TempChip** register and can be evaluated according to the following formula:

Temperature Measurement Formula

$$T_j = 1.3828 \times BINARY_{CODE} + 99.733 \quad (10)$$

T_J is in °C and the binary code is in 2's complement format.

The chip prevents over-heating through an over temperature threshold TSD (which includes a hysteresis TSD_HY). Once the die temperature reaches TSD, a thermal shutdown circuit will force the chip to reduce the consumption by stopping balancing. A fault is reported to the µC with a dedicated bit **OTchip** and propagated through the **FAULT Line**. When the temperature of the die returns to a normal level, L9963E can resume the normal operation. Balancing is released after the uC reads **OTchip** latch.

4.11.8 Balancing open load diagnostic

During Balancing open load diagnostic a pulldown current I_{PD_CB} is applied through the balancing path, including the discharge resistor. A voltage comparator is able to detect whether the voltage |Sn-Bn,n-1|, in Power balance OFF condition, falls below the open load threshold V_{BAL_OPEN}. If $T_{OPEN} - T_{NOT\_OPEN} > T_{BAL\_OL}/2$, the open load fault (**BALx_OPEN**) is latched.

Note: T_{OPEN} is the time interval where the comparator output is high (open fault present), while T_{NOT_OPEN} is the time interval where the comparator output is low (open fault not present).

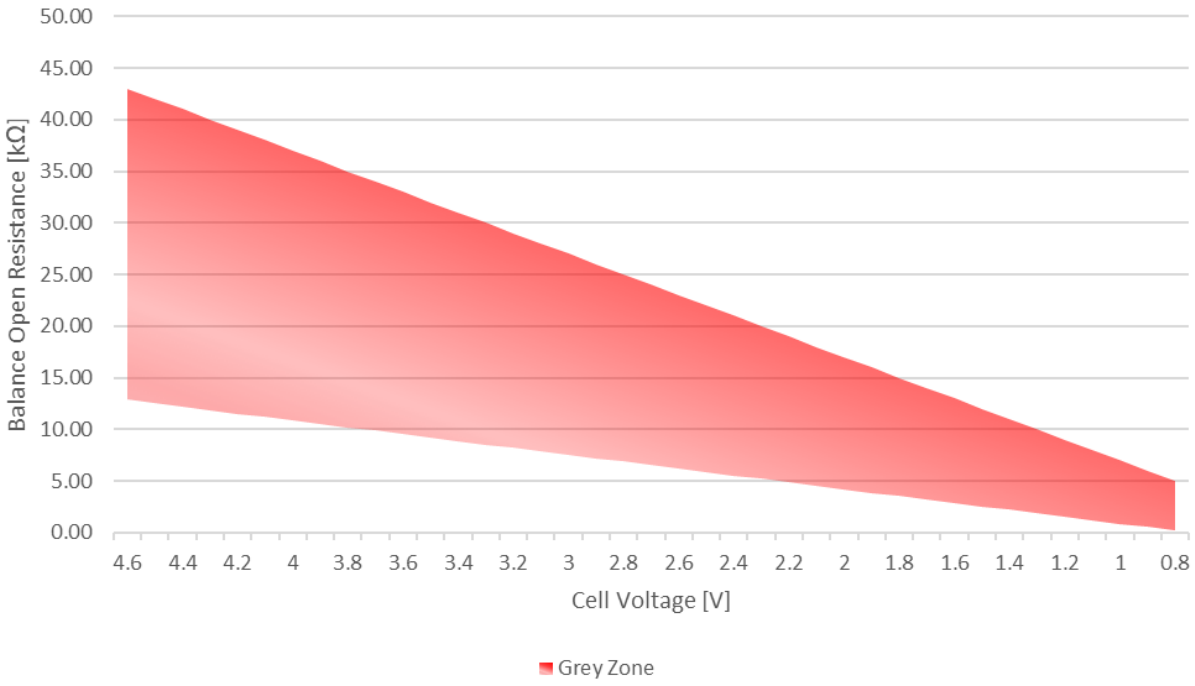
Balance comparator has a self test mechanism used to check internal integrity. In case BIST fails (**BIST_BAL_COMP_HS_FAIL** or **BIST_BAL_COMP_LS_FAIL**), balancing is stopped.

The equivalent open load resistance in series to the balancing path can be evaluated according to the following equation:

Equivalent balance open resistance estimation

$$R_{BAL_{OPEN}} = \frac{V_{CELL} - V_{BAL\_OPEN}}{I_{PD\_CB}} \quad (11)$$

Figure 20. **Equivalent open resistance vs.cell voltage**



In case of balance open detection on an enabled cell:

- Corresponding fault flag is set and latched into **BALX_OPEN** register
- Fault is propagated through the **FAULT Line**
- Voltage conversion routine goes into **Configuration Override**

For further details see Section 4.12 Voltage conversion routine.

This safety mechanism is also able to detect loss of cell PCB connector. In fact, if Celln positive terminal is disconnected from PCB, both BALn_OPEN and BALn+1_OPEN failures will be flagged. Two exceptions:

- If PCB connector to cell14 positive terminal (C14) is lost, only BAL14_OPEN flag will be set
- If PCB connector to cell1 negative terminal (C0), CELL0_OPEN flag will be set

4.11.9 Balancing short load diagnostic

The detection of the short load is implemented through the detection of overcurrent: if the balance current exceeds the overcurrent threshold I_{BAL_OC} for a time longer than $T_{BAL\_OVC\_DEGLITCH}$ a diagnostic short fault is reported. Such a diagnostic is active during Power balance ON condition.

Balance comparator has a self test mechanism used to check internal integrity. In case BIST fails (**BIST_BAL_COMP_HS_FAIL** or **BIST_BAL_COMP_LS_FAIL**), balancing is stopped.

In case of short detection:

- Corresponding fault flag is set and latched into register **BALx_SHORT**
- Fault is propagated through the **FAULT Line**
- Balance is stopped on the involved cell

Balance short detection is always active, even in low power modes (Silent Balancing, Cyclic Wakeup). When a failure is detected in low power states, balancing will be immediately stopped; however, the device will not wake up. **FAULT Line** and related fault latch will be triggered once the device has moved to **Normal**, following a wake up condition.

4.11.10 Balancing secondary timing

Secondary balancing timer is used to avoid over-discharge when manual balancing stop command communication failure or primary balancing timer function disorder happens.

4.11.11 Oscillator main clock monitoring

The oscillator used for the main logic functionalities and digital timings is monitored with a redundant oscillator that is electrically independent from the main one. Redundant oscillator is used just for safety purpose, in order to check a possible stuck condition. It can be activated by setting **clk_mon_en = 1**, and the confirmation of its activation can be read back via the **clk_mon_init_done** bit.

If a frequency difference greater than **Freq_diff** occurs between the two redundant clocks, the **OSCFail** flag is set.

4.11.11.1 Electrical parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:

9.6 V < VBAT < 64 V; -40 °C < Tambient < 105 °C

Main Oscillator Electrical parameters

Table 53. Main oscillator electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
FMAIN_OSC	Internal MAIN Oscillator frequency		15	16	17	MHz
FAUX_OSC	Internal redundant Oscillator frequency		15	16	17	MHz
Freq_diff	Delta oscillator check			15		%

4.11.12 Stand-by oscillator main clock monitoring

The Stand-by oscillator is used in both **Normal** operation and low power modes. It keeps alive all the standby functionalities, including wakeup circuitries, during **Sleep**, **Silent Balancing** and **Cyclic Wakeup**. It is also responsible for clocking the balancing activity during **Normal, Cyclic Wakeup** and **Silent Balancing** operation.

Thanks to this oscillator, balancing drivers can be continuously protected against a sudden short event, even in low power modes. In order to guarantee a maximum coverage against latent failures that could prevent from balancing short detection, such oscillator is monitored with a redundant oscillator that is electrically independent from the main one. Redundant oscillator is always available and is used just for safety purposes, in order to check a possible stuck condition of the main one. In case the main oscillator gets stuck, the Balancing Drivers are automatically switched off. This guarantees a fail safe operation, preventing infinite balancing duration.

If the failure happens while the device is in Normal mode, the communication with L9963E will still be functional.

If the failure occurs while the device is in a Low Power mode, L9963E will fail safely, but it will be impossible to wake up.

4.11.13 Regulator UV/OV diagnostic

VTREF, VCOM, VREG regulators have dedicated UV/OV diagnostic implementation. If one of these regulated voltages goes lower than the corresponding UV threshold or higher than the corresponding OV threshold for a time longer than the corresponding digital filter, the related fault flag is latched. Failure is then propagated through the **FAULT Line**.

In case of UV/OV detection:

- Corresponding fault flag is set and latched into **Faults1** register
- Fault is propagated through the **FAULT Line**
- In the specific case of VREG OV, Bootstrap and Balance functions are disabled
- In the specific case of VREG UV, Balance is disabled

4.11.14 Regulator self test

All power supplies are provided with a dedicate undervoltage or overvoltage test.

An analog self test on UV/OV comparators is implemented in order to guarantee high robustness safety requirements. Such a BIST can be requested via **Voltage Conversion Routine**:

- VTREF
- VCOM
- VREG

In case of wrong self test detection:

- Corresponding fault flag is set and latched into **BIST_COMP** register
- Fault is propagated through the **FAULT Line**
- Voltage conversion routine goes into **Configuration Override**

4.11.15 Regulator current limitation

Regulators VANA, VTREF, VCOM have dedicated current limitation features (refer to Table 45).

4.11.16 GPIO short FAULT

When GPIO are configured as digital outputs, they are short-protected. GPIO output value is monitored via the input Schmitt Trigger. If it differs from the programmed **GPOxOn** for a time interval longer than $T_{FILT\_GPIO\_ECHO}$, the short fault is detected.

In case of short detection:

- Corresponding fault flag is set and latched into **GPOxshort** register;
- Fault is propagated through the **FAULT Line**;
- Corresponding output buffer is put in HiZ.

The output re-engagement strategy is:

1. Toggle **GPOxOn** bit;
2. Clear **GPOxshort** latch via SPI read;
3. Reprogram **GPOxOn** bit to the desired value.

GPIO short detection is not available for GPIO9 when configured as SDO in SPI mode.

4.11.17 GPIO open fault (GPIO3-9)

When GPIO are used as analog inputs, it is possible to detect if an open wire has occurred between the pin and the R_{NTC} resistances on the board. To do this, a pulldown current $I_{GPIO\_PD\_OPEN}$ is turned on and, after $T_{GPIO\_OPEN\_SET}$, GPIO voltage is converted with $T_{CYCLEADC\_000}$; if converted voltage is lower than a threshold V_{GPIO_OL}, the open load detection occurs. This diagnostics is available just for GPIO3-9, if configured as analog input.

In case of open detection (with GPIO configured as analog input):

- Corresponding fault flag is set and latched into **GPIOX_OPEN** register;
- Fault is propagated through the **FAULT Line**;
- Voltage conversion routine goes into **Configuration Override**.

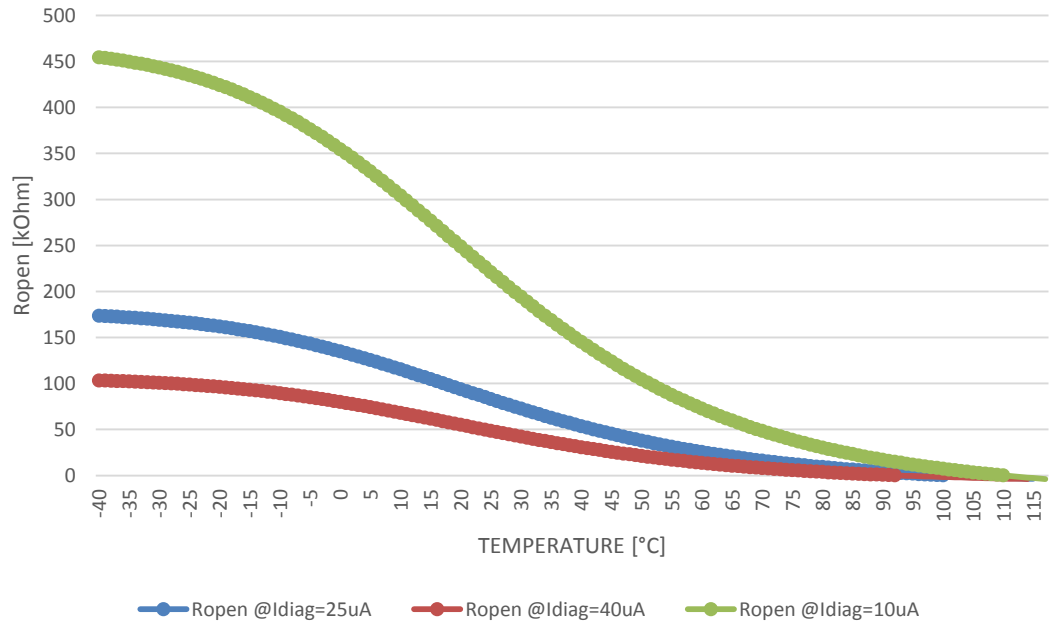
In case connection to the external NTC is lost at the PCB connector, the GPIO is pulled up to VTREF, thus causing OV/UT failure when the GPIO is converted. MCU is responsible for programming an OV/UT threshold below VTREF, in order to catch such event.

Figure 21 shows the equivalent series open resistance vs. temperature. The estimation has been made considering an NTC with $R_{25°C}$ and B = 3984 K. The calculation already accounts for the presence of the series filtering resistor and the BOM recommended in Table 83.

Estimation of the GPIO open resistance in the NTC analog front end

$$R_{OPEN} = \frac{V_{TREF}{}^{*}\frac{R_{NTC}(T)}{R_{NTC}(T)+R_{PU}}}{I_{GPIO\_PD\_OPEN}} - \frac{R_{PU}{}^{*}R_{NTC}(T)}{R_{PU}+R_{NTC}(T)} - R_{FIL} - \frac{V_{GPIO\_OL}}{I_{GPIO\_PD\_OPEN}} \quad (12)$$

Figure 21. **GPIO open resistance vs. temperature**



The proposed solution works fine in the whole cell operating temperature range. For very high and abnormal cell temperatures (greater than 90°C), a GPIOx_OPEN failure could be triggered when performing GPIO open diagnostic.

For further details see Section 4.12 Voltage conversion routine.

4.11.18 GPIO OT/UT (UV/OV) and fast charge OT diagnostic (GPIO3-9)

It is possible to select the value for the Overvoltage threshold (V_{GPIOAN_UT}) as well as for the Undervoltage threshold (V_{GPIOAN_OT}) of the analog voltages applied on GPIO pins. These diagnostics are available for GPIO3-9, if configured as analog input.

Dedicated OV/UT (**GPIOx_UT_TH**) and UV/OT (**GPIOx_OT_TH**) thresholds are available for each GPIO3-9. Individual OT/UT failures can be masked via dedicated **Gpiox_OT_UT_MSK** mask bit.

It is also possible to specify an increment ($V_{GPIO\_FASTCH\_OT\_DELTA}$) of the undervoltage threshold V_{GPIOAN_OT}. This increment, programmable via **Gpio_fastchg_OT_delta_thr** bit, will determine the position of the Fast Charge Undervoltage threshold ($V_{FASTCHG\_OT\_TH}$). Purpose of this diagnostic is providing an additional OT threshold to help MCU understanding when switching from fast charge (high DC current) to low power charge, thus preventing excessive overheating during the battery charging process.

The failure can be masked through the **Gpiox_fastchg_OT_MSK** bit. The actual fast charge undervoltage threshold will be placed according to the following formula:

$$V_{FASTCHG\_OT\_TH} = V_{GPIOAN\_OT} + V_{GPIO\_FASTCH\_OT\_DELTA} \quad (13)$$

This diagnostic can be used in application to monitor Overtemperature/Undertemperature events on external NTCs: UV is related to Overtemperature while OV is related to Undertemperature.

If voltage (measured using $T_{CYCLEADC\_000}$) is higher than the V_{GPIOAN_UT} threshold or lower than V_{GPIOAN_OT} threshold:

- Corresponding fault flag is set and latched into **VGPIO_OT_UT** register;
- Fault is propagated through the **FAULT Line**;
- Conversion routine goes into **Configuration Override**.

GPIO UT/OT failures can be masked via **Gpiox_OT_UT_MSK** bit. When masking is activated:

- Fault is not propagated through the **FAULT Line**;
- Conversion routine doesn't go into **Configuration Override**;
- **GPIOx_UT** and **GPIOx_OT** SPI flags are not set.

Masking OT/UT failure is useful when using analog inputs to measure sensors different than cell NTCs.

If voltage (measured using $T_{CYCLEADC\_000}$) is lower than $V_{FASTCHG\_OT\_TH}$ threshold:

- Corresponding Fast charge OT fault flag is set and latched into **GPIO_fastchg_OT** register;
- Fault is propagated through the **FAULT Line**;
- Conversion routine goes into **Configuration Override**.

$V_{GPIO\_FASTCH\_OT\_DELTA}$ has to be intended as a delta increase to be added to V_{GPIOAN_OT} threshold, as total Fast charge threshold must be always higher than V_{GPIO_UV}.

Fast charge stop fault can be masked via **Gpiox_fastchg_OT_MSK** bit. When masking is activated:

- Fault is not propagated through the **FAULT Line**;
- Conversion routine doesn't go into **Configuration Override**;
- **GPIOx_fastchg_OT** SPI flag is not set.

For further details refer to Section 4.12 Voltage conversion routine.

4.11.19 Current sense overcurrent

Current sense circuitry includes an overcurrent diagnostic active while the Coulomb Counter is enabled and the device is in **Cyclic Wakeup**. The diagnostic compares each sample of the current sense conversion with a digital threshold ($I_{CURR\_SENSE\_OC\_SLEEP}$). If the converted value is higher than $I_{CURR\_SENSE\_OC\_SLEEP}$, overcurrent detection occurs.

In case of curr sense OVC detection:

- Corresponding fault flag is set and latched into **curr_sense_ovc_sleep** register
- Fault is propagated through the **FAULT Line**
- Normal mode is entered

Failure can be masked by setting **ovc_sleep_msk = 1**.

Current sense circuitry includes also an overcurrent diagnostic active while the Coulomb Counter is enabled and the device is in **Normal**. The diagnostic compares each sample of the current sense conversion with a digital threshold ($I_{CURR\_SENSE\_OC\_NORM}$). If the converted value is higher than $I_{CURR\_SENSE\_OC\_NORM}$, overcurrent detection occurs.

In case of curr sense OVC detection:

- Corresponding fault flag is set and latched into **curr_sense_ovc_norm** register
- Fault is propagated through the **FAULT Line**

Failure can be masked by setting **ovc_norm_msk = 1**.

4.11.20 Current sense open diagnostic

Curr sense performs open diagnostic using internal $I_{ISENSEP}$ and $I_{ISENSEM}$ currents. If I_{SENSEP} or I_{SENSEM} pin voltages are higher than $V_{ISENSEP\_OPEN\_th}$ or $V_{ISENSEM\_OPEN\_th}$ threshold for a time longer than digital filter $T_{CURR\_SENSE\_OPEN\_filter}$, current sense open detection occurs.

In case of curr sense open detection, which occurs only if coulomb counter is enabled (**CoulombCounter_en = 1**):

- Corresponding fault flag is set and latched into **sense_plus_open** or **sense_minus_open** register. Because the CSA is choppering the inputs, both latches could be alternatively set
- Fault is propagated through the **FAULT Line**

4.11.21 Reference voltage monitor

Two BG references are used in order to guarantee independency between monitor functions. For each pair of cells, the two corresponding ADCs are referenced to different bandgaps. This guarantees results independency when performing **Cell open with ADC_CROSS_CHECK = 1** diagnostic.

4.11.22 Communication integrity

The communication frame is checked and verified to ensure the information is valid.

A Cyclic Redundancy Check (CRC) is used to ensure the serial data read from L9963E is valid and has not been corrupted even in application environments of high noise. For further information, refer to Section 4.2.4.6 CRC calculation.

4.11.23 Communication loss detection

In case no valid communication frame is received for t > t_SLEEP (programmable via **CommTimeout** bit), the **Comm_timeout_flt** latch is set and the device moves to **Sleep** or **Silent Balancing** state, depending on the **slp_bal_conf** bit.

In a vertical interface arrangement, any command addressing a slave unit will pass through the whole chain, thus serving the communication timeout for all the units. On the contrary, polling the Master unit is not a good strategy to refresh the communication timeout.

Communication timeout is enabled by default, but can be disabled by programming **comm_timeout_dis = '1'**.

For further information about Master and Slaves, refer to Section 4.2.1 Communication interface selection.

4.11.24 Rolling counter

To improve fault coverage on unintended message repetition, a rolling counter functionality has been implemented. MCU can send a MOSI frame setting a certain value for the Rolling Counter bit (LSB of the **Global Status Word (GSW)**). L9963E will answer setting the same Rolling Counter value in the next communication iteration (protocol is out of frame). So that this safety mechanism to be effective, MCU should continuously toggle the rolling counter bit each MOSI frame.

4.11.25 Trimming and calibration data integrity check

This safety mechanism checks:

- The trimming and calibration data stored in internal EEPROM. This is done everytime the NVM is downloaded (**EEPROM_DWNLD_DONE 0 → 1**). In case one of the EEPROM sectors is corrupted, the following error bit will be set:
  - **EEPROM_CRC_ERR_SECT_0** covers the trimming data
  - **EEPROM_CRC_ERR_CAL_RAM** covers the calibration data used by the **Voltage Conversion Routine**
  - **EEPROM_CRC_ERR_CAL_FF** covers the calibration data used by the **Coulomb Counting Routine**
- The data loaded into RAM, everytime it is requested by the **Voltage Conversion Routine** and **Coulomb Counting Routine**. In case of error, the following bit will be set:
  - **RAM_CRC_ERR** covers the data stored in RAM
  - The RAM correct functionality is guaranteed by BIST

NVM is downloaded upon first power up. Manual connection of battery cells might cause first power up failure due to slow stack voltage increase. In such a case, NVM first download might fail. Once the device has been correctly woken up, MCU shall check all the NVM error bit and, in case of data corruption, trimming data re-download can be triggered by attaining to the following procedure:

1. Set **trimming_retrigger = '1'**;
2. Wait for **Inter-frame Delay**;
3. Set **trimming_retrigger = '0'**;
4. Check all NVM error bit to confirm trimming and calibration data integrity;
5. Wait for at least **timeout_VCOM_UP_first** before executing any conversion.

4.11.26 FAULT heart beat

The heart beat functionality of the fault line guarantees continuous fault line integrity monitoring. Moreover, it acts as a windowed watchdog, where every stacked device monitors its upper companion. Refer to Section 4.3 FAULT line for further information.

4.11.27 GND loss detection

The device is able to check a possible AGND or DGND or CGND loss detection. If one of these ground pins has a voltage level higher than GND_LOSS_THR for a time longer than digital filter $T_{GND\_LOSS\_filter}$ the fault is confirmed and latched into one among **loss_agnd**, **loss_dgnd** or **loss_cgnd** bit.

4.11.28 Safety mechanisms summary

Table 54. Safety mechanisms summary

Category	Diagnostic name	Condition	Available in	Availability type	Actions	SPI related fields name	SPI related fields description	Masking	Masking condition
Cells	Cell UV	$V_{CELL} < V_{CELL\_UV}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Stop balance on involved cell •Configuration override	VCellx	Measurement Result	YES	VCELLx_EN = 0
						VCELLx_UV	Fault Latch		
						threshVcellUV	UV threshold		
Cells	Cell Balance UV	$V_{CELL} < V_{BAL\_UV\_TH}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Stop balance on involved cell •Configuration override	VCellx	Measurement Result	YES	VCELLx_EN = 0 OR VCELLx_BAL_UV_MSK = 1
						VCELLx_BAL_UV	Fault Latch		
						Vcell_bal_UV_delta_thr	Increment in respect to threshVcellUV		
Cells	Cell OV	$V_{CELL} > V_{CELL\_OV}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Configuration override	VCellx	Measurement Result	YES	VCELLx_EN = 0
						VCELLx_OV	Fault Latch		
						threshVcellOV	OV threshold		
Battery Stack	Sum Of Cells UV	$V_{BATT\_SUM} < V_{BATT\_UV\_SUM}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Stop balance on whole stack •Configuration override	vsum_batt1_0	Measurement Result LSB	NO	
						vsum_batt19_2	Measurement Result MSB		
						VSUM_UV	Fault Latch		
						VBATT_SUM_UV_TH	UV threshold		
Battery Stack	Sum Of Cells OV	$V_{BATT\_SUM} > V_{BATT\_OV\_SUM}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Configuration override	vsum_batt1_0	Measurement Result LSB	NO	
						vsum_batt19_2	Measurement Result MSB		

Category	Diagnostic name	Condition	Available in	Availability type	Actions	SPI related fields name	SPI related fields description	Masking	Masking condition
Battery Stack	Sum Of Cells OV	$V_{BATT\_SUM} > V_{BATT\_OV\_SUM}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Configuration override	VSUM_OV VBATT_SUM_OV_TH	Fault Latch OV threshold	NO	
Battery Stack	VBAT Critical UV	$V_{BATT\_MONITOR} < V_{BATT\_CRITICAL\_UV\_TH}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Stop balance on whole stack •Configuration override	VBATTCRIT_UV	Fault Latch	NO	
Battery Stack	VBAT Critical OV	$V_{BATT\_MONITOR} > V_{BATT\_CRITICAL\_OV\_TH}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Configuration override	VBATTCRIT_OV	Fault Latch	NO	
Battery Stack	VBAT UV Warning	$V_{BAT} < V_{BAT\_UV\_WARNING}$ for t > T_{VBAT_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	VBATT_WRN_UV	Fault Latch	NO	
BIST	VBAT UV Comparator BIST failure	VBAT Undervoltage Analog Comparator BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL	VBAT_COMP_BIST_FAIL	Fault Latch	NO	
Battery Stack	VBAT OV Warning	$V_{BAT} > V_{BAT\_OV\_WARNING}$ for t > T_{VBAT_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	VBATT_WRN_OV	Fault Latch	NO	
BIST	VBAT OV Comparator BIST failure	VBAT Overvoltage Analog Comparator BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL	VBAT_COMP_BIST_FAIL	Fault Latch	NO	
Cells	Cell Open	$V_{Cx\_SERIES\_DROP} > V_{CxOPEN}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Configuration override	CELLx_OPEN	Fault Latch	YES	VCELLx_EN = 0

Category	Diagnostic name	Condition	Available in	Availability type	Actions	SPI related fields name	SPI related fields description	Masking	Masking condition
BIST	ADCV BIST Fail	Failure converting internal reference connected to each input of the MUX	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Stop balance on whole stack •Configuration override	MUX_BIST_FAIL	Cx pin measurement failure	NO	
						OPEN_BIST_FAIL	Sx and Bx_x-1 pin failure		
						GPIO_BIST_FAIL	GPIOx measurement failure		
						VTREF_BIST_FAIL	Failure converting VTREF pin		
						VBAT_DIV_BIST_FAIL	Failure converting VBAT pin		
BIST	ADCV Cross Check Fail	$\|V_{ADCn} - V_{ADCn+1}\| > V_{ADC\_CROSS\_FAIL}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Configuration override	CELLn_OPEN	Fault Latch	YES	VCELLx_EN = 0
						CELLn+1_OPEN			
Junction Temperature	IC Overtemperature	$T_j > T_{SD}$	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL •Stop balance on whole stack	Otchip	Fault Latch	NO	
						TempChip	Measurement Result		
Balance	Balance Open	$T_{OPEN} - T_{NOT\_OPEN} > T_{BAL\_OL}/2$ refer to **Balancing open load diagnostic**	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Configuration override	BALx_OPEN	Fault Latch	YES	VCELLx_EN = 0
Balance	Balance Short	$I_{BAL} > I_{BAL\_OC}$ for $t > T_{BAL\_OVC\_DEGLITCH}$	Normal, Cyclic Wakeup, Silent Balancing	Always ON when balance is active	•Set Latch •Raise FAULTL •Stop balance on involved cell	BALx_SHORT	Fault Latch	YES	VCELLx_EN = 0
Balance	Balancing Secondary Timer Timeout	Balancing active for $t > T_{BAL\_TIMEOUT}$	Normal, Cyclic Wakeup	Always ON when balance is active	•Set Latch •Raise FAULTL •Stop balance on whole stack	EoBtimeerror	Fault Latch	NO	
BIST	Balance Open/Short Comparator BIST failure	Analog Comparator monitoring PowerMOS VDS BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL •Stop balance on involved cell	BIST_BAL_COMP_HS_FAIL	Fault Latch for Even Cells	YES	VCELLx_EN = 0
						BIST_BAL_COMP_LS_FAIL	Fault Latch for Odd Cells		

Category	Diagnostic name	Condition	Available in	Availability type	Actions	SPI related fields name	SPI related fields description	Masking	Masking condition
BIST	Main Oscillator Monitor Failure	Frequency mismatch between the two oscillators	Normal, Cyclic Wakeup	Always ON, when enabled	•Raise FAULTL •Set latch	clk_mon_en	Enable Bit	YES	clk_mon_en = 0
						OSCFail	Fault Status Bit		
						clk_mon_init_done	Enable Status Bit		
BIST	Standby Oscillator Monitor Failure	Frequency mismatch between the two oscillators	Normal, Cyclic Wakeup, Silent Balancing, Sleep	Always ON, when enabled	•Stop balance on whole stack			NO	
Regulators	VREG UV	$V_{VREG} < V_{VREG\_UV}$ for t > T_{VREG_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL •Stop balance on whole stack	VREG_UV	Fault Latch	NO	
BIST	VREG UV Comparator BIST failure	VREG Undervoltage Analog Comparator BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL	VREG_COMP_BIST_FAIL	Fault Latch	NO	
Regulators	VREG OV	$V_{VREG} > V_{VREG\_OV}$ for t > T_{VREG_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL •Stop balance on whole stack •Disable bootstrap	VREG_OV	Fault Latch	NO	
Regulators	VANA OV	$V_{VANA} > V_{VANA\_OV}$ for t > $T_{VANA\_OV\_FILT}$	Normal, Cyclic Wakeup	Always ON	•Set Latch	VANA_OV	Fault Latch	NO	
Regulators	VANA UV	$V_{VANA} < V_{VANA\_UV}$ for t > T_{POR_FILT}	All states	Always ON	•POR			NO	
Regulators	VDIG OV	$V_{VDIG} > V_{VDIG\_OV}$ for t > T_{VDIG_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch	VDIG_OV	Fault Latch	NO	
Regulators	VDIG UV	$V_{VDIG} < V_{VDIG\_UV}$ for t > T_{POR_FILT}	All states	Always ON	•POR			NO	

Category	Diagnostic name	Condition	Available in	Availability type	Actions	SPI related fields name	SPI related fields description	Masking	Masking condition
BIST	VREG OV Comparator BIST failure	VREG Overvoltage Analog Comparator BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL	VREG_COMP_BIST_FAIL	Fault Latch	NO	
Regulators	VTREF UV	$V_{VTREF} < V_{VTREF\_UV}$ for t > T_{VTREF_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	VTREF_UV VTREF_MEAS	Fault Latch Measurement Result	NO	
BIST	VTREF UV Comparator BIST failure	VTREF Undervoltage Analog Comparator BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL	VTREF_COMP_BIST_FAIL	Fault Latch	NO	
Regulators	VTREF OV	$V_{VTREF} > V_{VTREF\_OV}$ for t > T_{VTREF_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	VTREF_OV VTREF_MEAS	Fault Latch Measurement Result	NO	
BIST	VTREF OV Comparator BIST failure	VTREF Overvoltage Analog Comparator BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL	VTREF_COMP_BIST_FAIL	Fault Latch	NO	
Regulators	VCOM UV	$V_{VCOM} < V_{VCOM\_UV}$ for t > T_{VCOM_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	VCOM_UV	Fault Latch	NO	
BIST	VCOM UV Comparator BIST failure	VCOM Undervoltage Analog Comparator BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL	VCOM_COMP_BIST_FAIL	Fault Latch	NO	
Regulators	VCOM OV	$V_{VCOM} > V_{VCOM\_OV}$ for t > T_{VCOM_FILT}	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	VCOM_OV	Fault Latch	NO	
BIST	VCOM OV Comparator BIST failure	VCOM Overvoltage Analog Comparator BIST Fail	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine	•Set Latch •Raise FAULTL	VCOM_COMP_BIST_FAIL	Fault Latch	NO	
GPIO	GPIO Short	GPOxon != GPIx for t > $T_{FILT\_GPIO\_ECHO}$	Normal, Cyclic Wakeup	Always ON, when GPIO configured as Digital Output	•Set Latch •Raise FAULTL •Put GPIO in HiZ	GPOxshort	Fault Latch	YES	GPIOx_CONFIG != 11

Category	Diagnostic name	Condition	Available in	Availability type	Actions	SPI related fields name	SPI related fields description	Masking	Masking condition
GPIO	GPIO Open	V_{GPIO} < V_{GPIO_OL}	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine Only for GPIO3-9	•Set Latch •Raise FAULTL •Configuration override	GPIOx_OPEN	Fault Latch	YES	GPIOx_CONFIG != 00
GPIO	GPIO OT	V_{GPIO} < V_{GPIOAN_OT}	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine Only for GPIO3-9	•Set Latch •Raise FAULTL •Configuration override	GPIO_OT_TH	OT threshold	YES	GPIOx_CONFIG != 00 OR Gpiox_OT_UT_MSK = 1
						GPIOx_OT	Fault Latch		
						GPIOx_MEAS	Measurement Result		
GPIO	GPIO Fast Charge OT	V_{GPIO} < $V_{FASTCHG\_OT\_TH}$	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine Only for GPIO3-9	•Set Latch •Raise FAULTL •Configuration override	Gpio_fastchg_OT_delta_thr	Increment in respect to GPIO_OT_TH	YES	GPIOx_CONFIG != 00 OR Gpiox_fastchg_OT_MSK = 1
						GPIOx_fastchg_OT	Fault Latch		
						GPIOx_MEAS	Measurement Result		
GPIO	GPIO UT	V_{GPIO} > V_{GPIOAN_UT}	Normal, Cyclic Wakeup	Periodic or On-Demand Voltage Conversion Routine Only for GPIO3-9	•Set Latch •Raise FAULTL •Configuration override	GPIO_UT_TH	UT threshold	YES	GPIOx_CONFIG != 00 OR Gpiox_OT_UT_MSK = 1
						GPIOx_UT	Fault Latch		
						GPIOx_MEAS	Measurement Result		
GPIO	Incoming Fault	FAULTH = 1 for t > $T_{FIL\_H\_LONG}$	Normal, Cyclic Wakeup, Silent Balancing, Sleep	Always ON	•Set Latch •Raise FAULTL	FaultHline_fault	Fault Latch	YES	HeartBeat_En = 0 OR FaultH_EN = 0
		FAULTH = 1 for t > $T_{FIL\_H\_SHORT}$							FaultH_EN = 0
GPIO	Absence Of Heartbeat	FAULTH = 0 for t > 1.2*T_{HB_CYCLE}	Normal	Always ON	•Set Latch •Raise FAULTL	HeartBeat_fault	Fault Latch	YES	HeartBeat_En = 0 OR FaultH_EN = 0

Category	Diagnostic name	Condition	Available in	Availability type	Actions	SPI related fields name	SPI related fields description	Masking	Masking condition
Coulomb Counter	CSA Open	$V^{ISENSEP}$ > $V_{ISENSEP\_OPEN\_TH}$ for t > $T_{CURR\_SENSE\_OPEN\_FILTER}$ OR $V_{ISENSEM}$ > $V_{ISENSEM\_OPEN\_TH}$ for t > $T_{CURR\_SENSE\_OPEN\_FILTER}$	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	sense_plus_open	Fault Latch	YES	CoulombCounter_en = 0
						sense_minus_open	Fault Latch		
Coulomb Counter	OC Sleep	I_{SENSE} > $I_{CURR\_SENSE\_OC\_SLEEP}$	Cyclic Wakeup	Always ON in the duty phase	•Set Latch •Raise FAULTL	curr_sense_ovc_sleep	Fault Latch	YES	CoulombCounter_en = 0 OR ovc_sleep_msk = 1
						CUR_INST_calib	Measurement Result		
						adc_ovc_curr_threshold_sleep	OC Threshold		
Coulomb Counter	OC Normal	I_{SENSE} > $I_{CURR\_SENSE\_OC\_NORM}$	Normal	Always ON	•Set Latch •Raise FAULTL	curr_sense_ovc_norm	Fault Latch	YES	CoulombCounter_en = 0 OR ovc_norm_msk = 1
						CUR_INST_calib	Measurement Result		
						adc_ovc_curr_threshold_norm	OC Threshold		
Coulomb Counter	Sample Counter or Accumulator Overflow	CoulombCntTime overflows OR CoulombCounter_msb overflows	Normal	Always ON	•Set Latch •Raise FAULTL	CoCouOvF	Fault Latch	NO	
BIST	Bandgap Monitor Fail	One Bandgap Reference shifts too much in respect to the other	Normal, Cyclic Wakeup	Always ON	•POR			NO	
BIST	EEPROM Checksum Failure	An unwanted change in EEPROM data occurred	Trimming, Normal	Upon EEPROM Download	•Set Latch •Stop balance on whole stack	EEPROM_CRC_ERR_SECT_0	Fault Latch	YES	EEPROM_CRC_ERR MSK_SECT_0 = 1
						EEPROM_CRC_ERR_CAL_RAM	Fault Latch		

Category	Diagnostic name	Condition	Available in	Availability type	Actions	SPI related fields name	SPI related fields description	Masking	Masking condition
BIST	EEPROM Checksum Failure	An unwanted change in EEPROM data occurred	Trimming, Normal	Upon EEPROM Download	•Set Latch •Stop balance on whole stack	EEPROM_CRC_ERR_CAL_FF	Fault Latch	YES	EEPROM_CRC_ERRMSK_CAL_RAM = 1 EEPROM_CRC_ERRMSK_CAL_FF = 1
BIST	RAM Checksum Failure	An unwanted change in RAM data occurred	Normal, Cyclic Wakeup	Always ON	•Set Latch •Stop balance on whole stack	RAM_CRC_ERR	Fault Latch	YES	RAM_CRC_ERRMSK = 1
BIST	AGND and GNDREF Loss	Loss of both AGND and GNDREF in respect to DGND, lasting more than TGND_LOSS_FILTER	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	loss_agnd	Fault Latch	NO	
BIST	DGND / CGND Loss	A ground shift among AGND, and DGND, or AGND and CGND, lasts more than TGND_LOSS_FILTER	Normal, Cyclic Wakeup	Always ON	•Set Latch •Raise FAULTL	loss_dgnd loss_cgnd	Fault Latch Fault Latch	NO	

4.12 Voltage conversion routine

L9963E implements a flexible voltage conversion routine, whose main goals are:

- Providing on-demand information about the cells voltage, the stack voltage and the cell temperature;
- Providing on-demand diagnostic information about the device functionality;
- Periodically monitoring the cells and the stack status, along with the device functionality;
- Limit the power consumption by activating only the necessary resources;
- Automatically validate any eventual failure detected during the routine execution.

The following parameters play a key role in the definition of the voltage routine behavior:

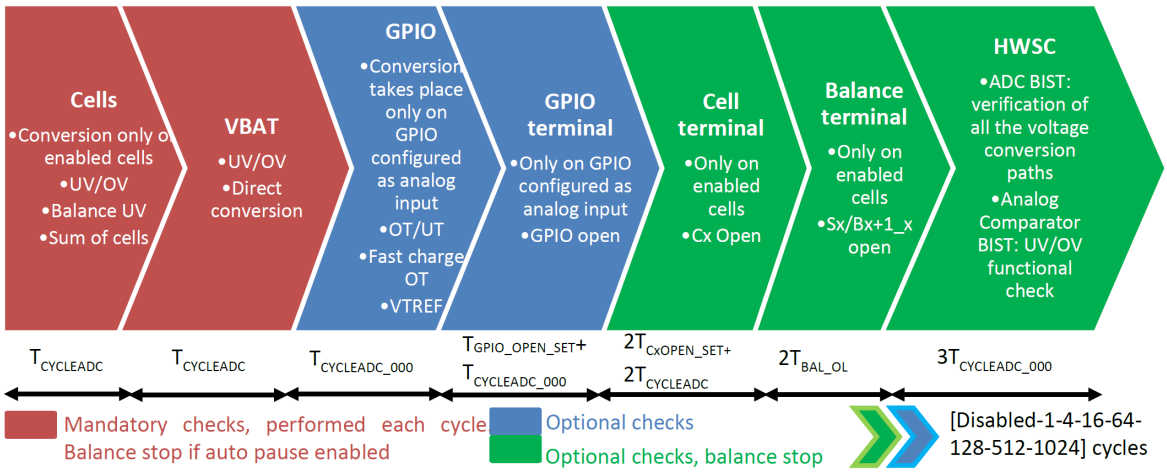
- $T_{CYCLEADC}$ refers to the duration of a voltage conversion step. It can be programmed via the **ADC_FILTER_SOC** (for **On-Demand Conversions** in **Normal**st ate) and **ADC_FILTER_CYCLE** (for cyclic operation in both **Normal** and **Cyclic Wakeup** states) bit fields. Available values are listed in Table 38:
  - $T_{CYCLEADC\_XXX}$ refers to a fixed option of $T_{CYCLEADC}$, thus implying a fixed duration for the voltage conversion;

- **TCYCLE** refers to the internal counter determining the routine period (sum of active and idle phases). It can be programmed via the **TCYCLE** (for operation in **Normal** state) and **TCYCLE_SLEEP** (for operation in **Cyclic Wakeup** state) bit fields. Available values are listed in Table 68:
  - $\mathbf{T_{ROUTINE}}$ refers to the duration of the active phase. It's a variable time interval depending on how many steps have been scheduled for execution and their duration;
  - **DUTY_ON** is a flag set during the active phase, that is during $\mathbf{T_{ROUTINE}}$, independently of the routine execution mode;
  - The idle phase lasts **TCYCLE** - $\mathbf{T_{ROUTINE}}$. Hence the routine duty-cycle is represented by the ratio $\mathbf{T_{ROUTINE}}$ / **TCYCLE**;
  - **TCYCLE_OVF** is a latch set when $\mathbf{T_{ROUTINE}}$ > **TCYCLE**. This anomalous situation is often referred to an **overflow** because it leads to duty-cycle saturation (100%);
- **NCYCLE** refers to the internal counter that is incremented by one every time a routine period ends. It is useful for scheduling optional step execution every X cycles.
  - **NCYCLE_X** refers to a threshold specifying the X-th step periodicity. It can be programmed independently of each step via SPI (e.g. **NCYCLE_GPIO = '010'** specifies that GPIO conversion must take place every 4 cycles). Refer to Section 4.12.4 Operations periodicity for all the available options.

4.12.1 Routine structure

The voltage conversion routine is structured as follows:

Figure 22. Voltage conversion routine



The steps are organized as follows:

- Mandatory checks: they are fixed and cannot be excluded. They perform main operations such as Cells and VBAT measurement;
  - Balance is paused if **BAL_AUTO_PAUSE = 1**.
- Optional checks: they can be excluded or periodically executed. Each step periodicity can be configured independently via its **NCYCLE_X** bit field (e.g. the **NCYCLE_GPIO** field programs the cyclic execution of the GPIO conversion);
  - Steps involving the GPIOs do not affect balancing.
  - Steps involving Cell Terminal, Balance Terminal and HWSC require balance to be stopped independently of the **BAL_AUTO_PAUSE** value.

In case balance is paused during a step, balance timer is frozen if **BAL_TIM_AUTO_PAUSE = 1**, otherwise it keeps running even if balance operation is temporarily interrupted. Refer to Figure 25 in order to understand the functionality of **BAL_AUTO_PAUSE** and **BAL_TIM_AUTO_PAUSE** bit.

Refer to Figure 25 for a graphic example of the **BAL_AUTO_PAUSE** and **BAL_TIM_AUTO_PAUSE** bit.

Depending on the wire length of the cell wires connected to the PCB, some inductive spikes might be seen when interrupting the balancing, prior to “Cells” step of the **Voltage Conversion Routine**. These spikes can be a source of inaccuracy, especially if Cx pins are filtered using high values for RLPF (e.g. 3 kΩ), requiring a relatively high settling time. It is possible to specify a settling time T_{CELL_SET} by programming the **T_CELL_SET** SPI field. Upon Start Of Conversion (SOC) event, L9963E will wait for **T_CELL_SET** before starting the **Voltage Conversion Routine**. Such a settling time is only enabled if **BAL_AUTO_PAUSE = 1**. In order to keep synchronization with the **Coulomb Counting Routine**, the Cells step might be additionally delayed in order to align with the first useful current sample. In the worst case, the total delay is **T_CELL_SET** + $T_{CYCLEADC\_CUR}$.

The VTREF regulator is normally used for temperature sensing applications, involving the GPIO steps of the routine. To save current, it can be dynamically enabled only when needed, according to the following table:

Table 55. VTREF operating modes

VTREF_EN	VTREF_DYN_EN	VTREF Regulator behavior
0	0	(Default). VTREF regulator disabled
0	1	VTREF regulator disabled
1	0	VTREF regulator permanently enabled
1	1	VTREF regulator dynamically enabled. The regulator is normally OFF. It is enabled at each Start Of Conversion (SOC) event (either on-demand or cyclic), with a settling time T_{CELL_SET} in respect to the Cells step of the **Voltage Conversion Routine**. The regulator is kept enabled until the last step of the routine (HWSC) has been performed.

Due to flexibility, routine execution time **TROUTINE** is not fixed. It depends on the programmed voltage acquisition window (either **ADC_FILTER_SOC** or **ADC_FILTER_CYCLE** depending on the conversion type) and the number of steps scheduled for execution (see Section 4.12.4 Operations periodicity).

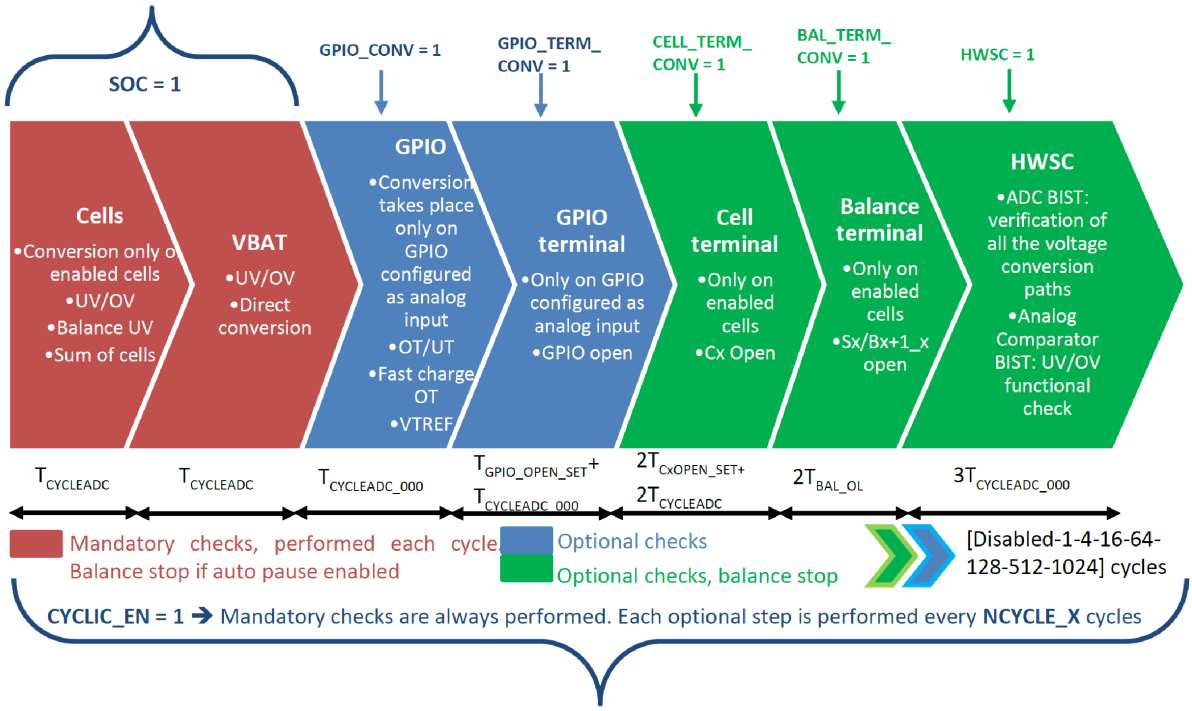
Voltage conversion routine duration

$$\begin{cases} T_{ROUTINE_{MIN}} = 2T_{CYCLEADC}, \text{ when only mandatory checks are executed} \\ T_{ROUTINE_{MAX}} = 4T_{CYCLEADC} + 5T_{CYCLEADC\_000} + 2T_{BAL\_OL} + 2T_{CxOPEN\_SET} + T_{GPIO\_OPEN\_SET}, \text{ when all checks are executed} \end{cases} \quad (14)$$

4.12.2 Routine execution modes

The voltage conversion routine can be executed in three different ways according to microcontroller commands. The different modes are mutually exclusive: only one routine execution at a time is allowed and multiple threads are not supported.

Figure 23. Routine execution modes: on-demand and cyclic executions



The execution modes follow a priority concept:

- **Configuration Override** has high priority, since its purpose is to perform diagnostics upon failure detection in order to validate the catch. It can interrupt any ongoing activity and, once done, Voltage conversion routine is moved to **Idle** state, waiting for the microcontroller to interpret the diagnostic data.
- **On-Demand Conversions** have low priority. They are meant to allow microcontroller performing measurements or diagnostics at specific time instants. They cannot co-exist with **Cyclic Conversions**: to run an on-demand conversion, cyclic conversions have to be disabled and MCU has to wait for their termination (monitor the **DUTY_ON** flag). On the other hand **On-Demand Conversions** cannot interrupt themselves, nor a **Configuration Override**.
- **Cyclic Conversions** have low priority. Their purpose is mainly to monitor battery pack and L9963E status. However, they can also be used to periodically retrieve measurement data. They can be interrupted by **Configuration Override**. They cannot co-exist with **On-Demand Conversions***:* before enabling cyclic conversions, MCU must wait for any ongoing on-demand conversion to end first (monitor the **DUTY_ON** flag).

In general, microcontroller is able to determine L9963E activity by performing a read operation on the **ADCV_CONV** register and observing the following bit:

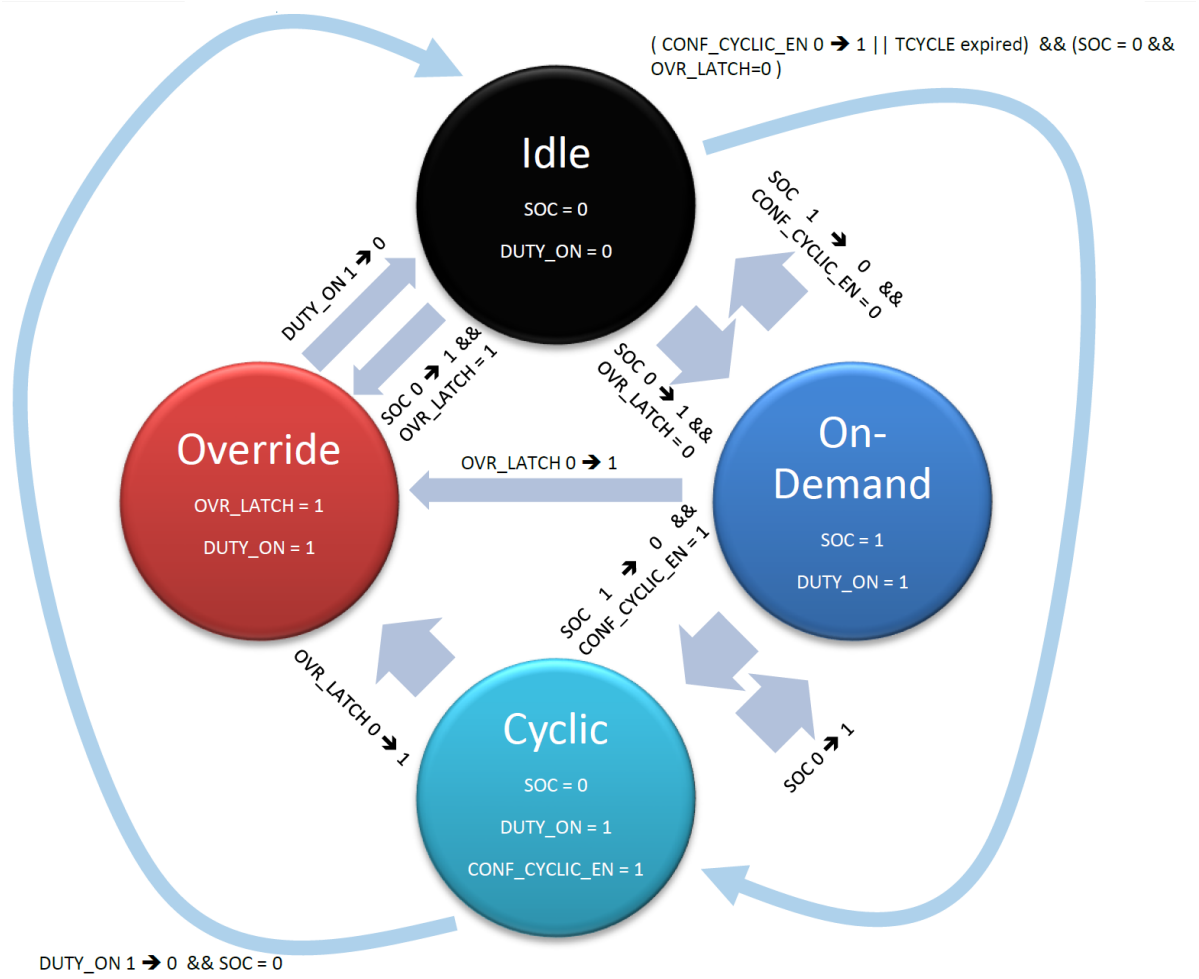
Table 56. Voltage conversion routine status

SOC (status upon readback)	OVR_LATCH	CONF_CYCLIC_EN	DUTY_ON	Device status
0	0	0	0	Idle
0	0	0	1	Not possible

SOC (status upon readback)	OVR_LATCH	CONF_CYCLIC_EN	DUTY_ON	Device status
0	0	1	0	Cyclic activity, (idle phase)
0	0	1	1	Cyclic activity, (duty phase)
0	1	0	0	Idle (last execution set the override latch)
0	1	0	1	Not possible
0	1	1	0	Cyclic activity locked in idle phase after the end of override: MCU must set CONF_CYCLIC_EN = 0 and then run a SOC
0	1	1	1	Fault detected during cyclic activity with override still ongoing
1	0	0	0	Not possible
1	0	0	1	On-demand conversion
1	0	1	0	Not possible
1	0	1	1	On-demand conversion interrupting a cyclic one (must be avoided since results may not be reliable)
1	1	0	0	Not possible
1	1	0	1	On-demand conversion after a fault was detected
1	1	1	0	Not possible
1	1	1	1	On-demand conversion interrupting a cyclic one. Failure detected during the on-demand conversion (must be avoided since results may not be reliable)

The following FSM describes the functionality and the transitions among the different operating modes of the voltage conversion routine.

Figure 24. **Equivalent FSM behavior of the voltage conversion routine**



4.12.2.1 *On-Demand conversions*

To start **On-Demand Conversions**, the user must set **SOC = 1** in the **ADCV_CONV** register: in case the **Coulomb Counting Routine** is enabled, everytime an on-demand voltage conversion is requested by setting **SOC = 1**, the actual conversion start is delayed until the first useful current conversion takes place. This allows a perfect synchronization between voltage and current samples, but might result in a maximum delay of $T_{CYCLEADC\_CUR}$, that must be taken into account by user SW and added to the recommended T_{DATA_READY} in Table 38.

- **Cell Conversion** and **VBAT Conversion** step are always executed
- **GPIO Conversion** is executed only if **GPIO_CONV = 1** in the same SPI frame
- **GPIO Terminal Diagnostics** is executed only if **GPIO_TERM_CONV = 1** in the same SPI frame
- **Cell Terminal Diagnostics** is executed only if **CELL_TERM_CONV = 1** in the same SPI frame
- **Balance Terminal Diagnostics** is executed only if **BAL_TERM_CONV = 1** in the same SPI frame
- **HardWare Self-Check (HWSC)** is executed only if **HWSC = 1** in the same SPI frame

Once set, **SOC** stays high until the conversion routine ends (refer to for the routine duration $T_{ROUTINE}$), then it is internally reset. While **SOC** is high, any attempt to perform an on-demand conversion will be discarded. A feedback on the on-demand conversion status can be retrieved via the **DUTY_ON** flag. Setting any of the optional bit without setting **SOC** in the same SPI frame has no effect: conversion will not be started.

The user can select the desired voltage acquisition window ($T_{CYCLEADC}$) by programming the **ADC_FILTER_SOC** fielding the **ADCV_CONV** register.

Registers containing measurement results are updated as soon as the related conversion step is over, so they are available before $T_{ROUTINE}$ ends. Each measurement register contains a **d_rdy_xx** (data ready) bit, which is set when a new measurement incomes and is reset upon a data read operation.

Upon an on-demand conversion (SOC), the first step of the voltage conversion routine (cell measurement) is delayed until the first available current conversion start pulse comes. Hence, the cell measurement will start synchronously with the current sample acquisition. This technique is effective only by choosing the shortest filter option for voltage conversion routines ($T_{CYCLEADC\_000}$).

On-Demand Conversions have lower priority than **Configuration Override**. When **SOC 0 → 1**:

- If a **Configuration Override** is ongoing, it won't be affected by **SOC** command. Therefore **SOC**, **GPIO_CONV** and **DIAG** bit will be discarded and kept **'0'**.

4.12.2.2 *Cyclic conversions*

To start **Cyclic Conversions**, the user must set **CONF_CYCLIC_EN = 1** in the **ADCV_CONV** register. The **ADC_FILTER_CYCLE** determines the duration of the routine steps. **Cyclic Conversions** activity can be used for both diagnostic and measurement purposes:

- In case the routine is only intended for diagnostic purposes, the user may program **CYCLIC_UPDATE = 0**. This setting will cause any conversion result to be used only for internal comparisons. Data will be subsequently discarded and registers containing measurement results won't be updated.
- In case measurement results are important, the user may program **CYCLIC_UPDATE = 1**, thus causing measurement registers update upon each step completion, as for **On-Demand Conversions**. Be aware that results of a previous on-demand conversion might be overwritten by the ones of cyclic executions.

Two counters are implemented for driving the cyclic execution:

- **TCYCLE** is an SPI programmable timer accounting for cycle period. User can program the **TCYCLE** field in the **ADCV_CONV** register.
- **NCYCLE** is an internal counter, incremented by 1 every time **TCYCLE** expires: it counts the number of cycles executed. It works in conjunction with the **NCYCLE_X** parameters to determine the periodicity of each routine step (refer to Section 4.12.4 Operations periodicity). In general, each step is executed if its **NCYCLE_X** parameter is different than 0.

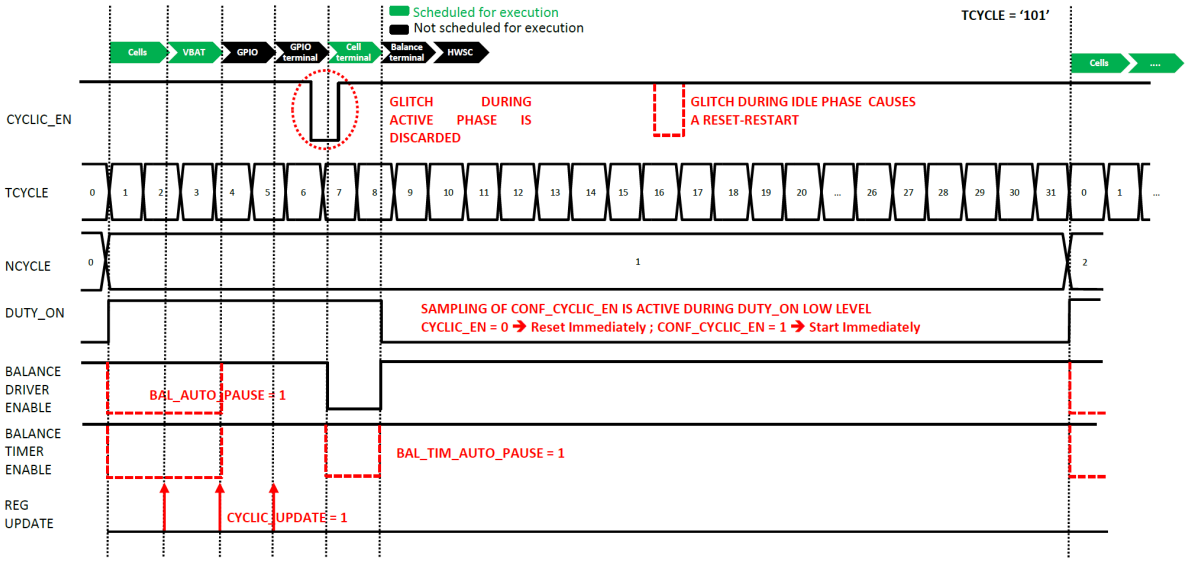
TCYCLE and **NCYCLE** shall not be updated while **Cyclic Conversions** are ongoing: routine must be first disabled by programming **CONF_CYCLIC_EN = 0** and then re-enabled once all configuration parameters have been updated.

Such counters are started/stopped upon FSM transitions. The following table summarizes all events involving the two timers:

Table 57. Summary of the NCYCLE and TCYCLE events

Event	NCYCLE	TCYCLE	Effect on routine
Routine active phase ($T_{ROUTINE}$)	Frozen	Counting	Steps are being performed
Routine idle phase	Frozen	Counting	No step is being performed
TCYCLE expiration	NCYCLE = NCYCLE + 1	Restarted from 0	Routine restarted from first step
CONF_CYCLIC_EN → 1	no action	Reset and start from 0	Routine initialized and started. See Table 58 for additional information
CONF_CYCLIC_EN 1 → 0	Wait for idle phase (DUTY_ON 1 → 0), then Stop and Reset	Wait for idle phase (DUTY_ON 1 → 0), then Stop and Reset	Routine disabled and reset after the active phase completion. See Table 58 for additional information

Figure 25. **Example of routine execution in normal mode**



During a **TCYCLE**, the **DUTY_ON** flag is set when the routine is in the active phase (during **TROUTINE**), while it is reset during the remaining idle time. It reflects the duty-cycle of the cyclic routine:

DUTY_ON flag duty-cycle during a cyclic execution

$$DUTY\_ON_{high\%} = \frac{T_{ROUTINE}}{T_{CYCLE}} \times 100 \quad (15)$$

Programming a $T_{ROUTINE}$ longer than **TCYCLE** is not recommended. Routine will behave in continuous mode, even if not explicitly set.

In order to program a continuous execution the user must set **CYCLIC_CONTINUOUS = 1** before enabling the cyclic mode (**CONF_CYCLIC_EN = 1**).

Table 58. **Focus on routine enable/disable and continuous mode activation/deactivation**

CONF_CYCLIC_EN	CYCLIC_CONTINUOUS	Effect on routine
1 → 0	0	Any ongoing routine is disabled once the active phase of the current cycle is completed (DUTY_ON 1 → 0). Setting-Resetting CONF_CYCLIC_EN while DUTY_ON = 1 is considered as a glitch and will be discarded. Refer to Figure 25.
1 → 0	1	The routine is disabled after the last enabled step of the cycle has been executed (upon $T_{ROUTINE}$ completion).
0 → 1	0	Routine is started with TCYCLE periodicity.
0 → 1	1	Routine is started in continuous mode. NCYCLE started.
0	X	Changing CYCLIC_CONTINUOUS while the routine is disabled has no effect.

While in continuous mode, **TCYCLE** is ignored and the periodicity will be given by **TROUTINE**. **NCYCLE** will be incremented upon each routine completion (every $T_{ROUTINE}$).

The following table lists sampling intervals for the configuration parameters related to the cyclic functionality. It is useful to understand when the new settings will be applied after they have been modified during an on-going activity.

Table 59. **Sampling intervals for the configuration parameters related to cyclic functionality**

Parameter	Normal mode	Continuous mode
CONF_CYCLIC_EN	Continuously sampled while DUTY_ON = 0	Every TROUTINE
ADC_FILTER_CYCLE	Every TCYCLE	Every TROUTINE
CYCLIC_CONTINUOUS	Every TCYCLE	Every TROUTINE
BAL_TIM_AUTO_PAUSE	Every TCYCLE	Every TROUTINE
BAL_AUTO_PAUSE	Every TCYCLE	Every TROUTINE
CYCLIC_UPDATE	Every TCYCLE	Every TROUTINE
NCYCLE_X	Every TCYCLE	Every TROUTINE

4.12.2.3 *Configuration override*

The **Configuration Override** is a special routine execution mode, which is internally triggered by failure assertion, independently of the conversion type. It is meant to simplify failure validation and it works according to the following algorithm.

If a failure is asserted at the x-th routine step, all the following steps will be performed, independently of their activation or periodicity. Any failure detected during these steps will be latched and available for the microcontroller to perform failure validation (refer to Figure 26).

- Finding the **OVR_LATCH** set means that override occurred:
  - The **OVR_LATCH** is set upon failure assertion during the routine execution.
  - The **OVR_LATCH** is released and can be cleared upon read in case the last on-demand execution has ended without any failure detected (even if failures detected by previous executions are still latched in diagnostic registers).
  - All fault latches related to measurement registers (e.g. CELLx_UV/OV, GPIO UT/OT, etc.) cannot be cleared until a new conversion is executed and the root cause fault has disappeared. To understand the fault status of the last routine execution the MCU SW should observe the OVR_LATCH.
- In case cyclic mode was activated, routine is not restarted after a **Configuration Override**. The **OVR_LATCH** masks the **CONF_CYCLIC_EN** configuration. This helps locking the routine status, allowing the MCU to intervene and observe the snapshot of the last execution.
- Once **Configuration Override** is over (**DUTY_ON 1 → 0**), the voltage conversion routine is kept in idle, waiting for microcontroller to read diagnostic registers and validate the failure.
- The following fault handling procedure must be executed once configuration override is over:
  1. MCU must access diagnostic latches and perform correct failure validation as recommended in Table 60.
  2. MCU must launch **On-Demand Conversions** (SOC = 1) in order to update measurement registers, while also disabling any cyclic execution by setting **CONF_CYCLIC_EN = 0** in the same SPI frame.
  3. MCU must wait for **On-Demand Conversions** to be over and evaluate routine result by reading the **ADCV_CONV** register. A read operation on such a register would reset the **OVR_LATCH** in case the execution launched at step 2 ended with no failure:
     - In case failure persists, the read operation will not reset the **OVR_LATCH**. Return to step 1.
     - In case failure disappeared, reading the **ADCV_CONV** register will also reset the **OVR_LATCH**. Proceed to step 4.
  4. Read all diagnostic latches in order to clear them.
  5. (Optional) Restart any cyclic execution by setting **CONF_CYCLIC_EN = 1**

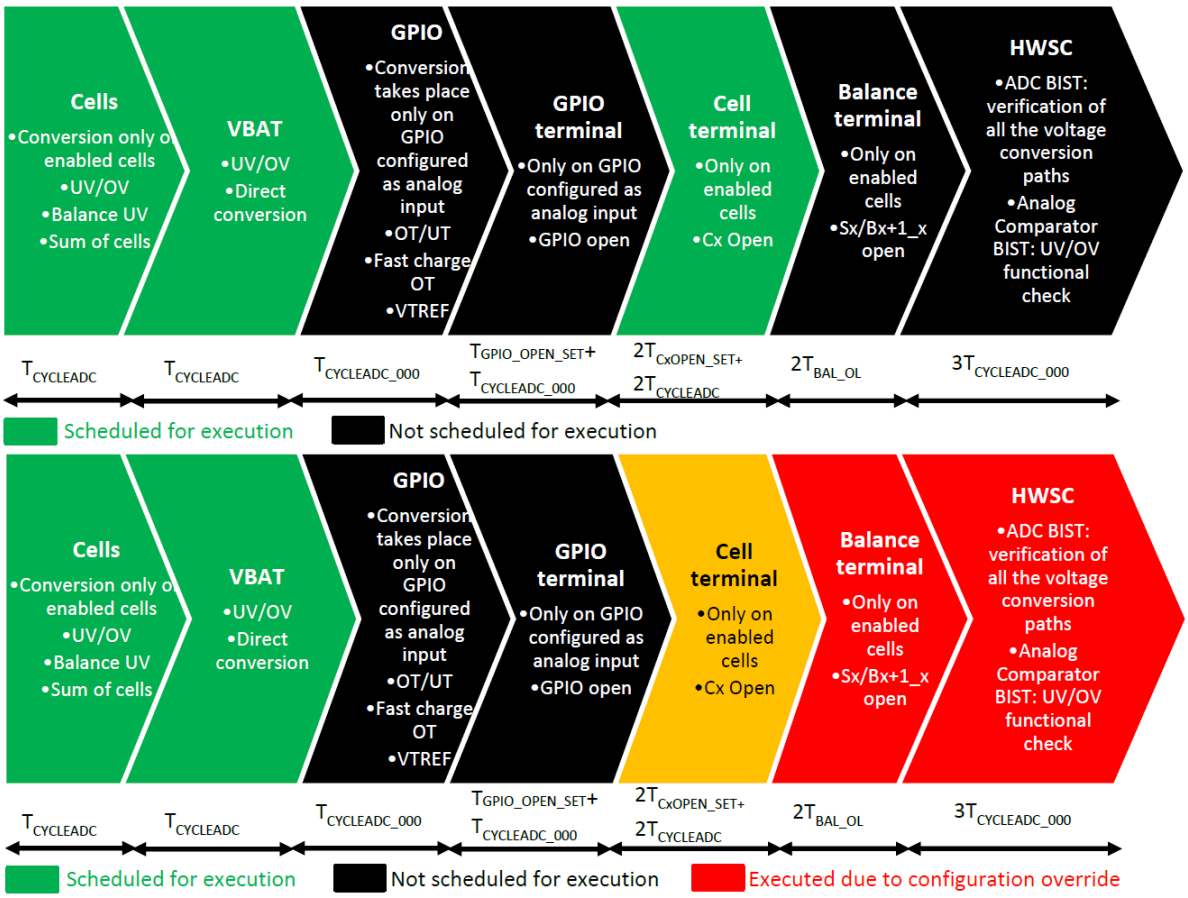
Writing **ADCV_CONV** and **NCYCLE_PROG_X** registers during a **Configuration Override** is strongly not recommended, since it might affect the failure validation. The configuration override is performed keeping the same ADC filter settings programmed for the execution mode that was being executed. For instance, if it occurs during **On-Demand Conversions**, the **ADC_FILTER_SOC** will be used; in case it interrupts ***Cyclic Conversions***, the **ADC_FILTER_CYCLE** or the **ADC_FILTER_SLEEP** will be used, depending on the device status. Microcontroller is able to detect the **Configuration Override** activity by polling the voltage conversion routine status as shown in Table 56.

The steps of the voltage conversion routine have been arranged in a fixed order, engineered to allow failure validation in every possible scenario thanks to the **Configuration Override** capability:

Table 60. Failure validation table

Failure type	What to check for validation	Reason
Cell UV/OV	Sum of cells	Is the sum of cells coherent with a cell UV/OV failure?
	Balance UV	If a cell UV is detected, then also balance UV should be flagged
	Cx Open	Not measuring actual cell voltage
	Balance open	PCB connector to a cell might have been lost
	HWSC	Is measurement reliable?
Sum of cells UV/OV	VBAT direct conversion	Is the VBAT direct conversion close to the sum of cells?
	Cell UV/OV	Is there at least one cell in UV/OV condition?
	Cx Open	Not measuring actual cell voltage
	HWSC	Is measurement reliable?
Balance UV	Cell UV	If a Cell UV is flagged, then it's much worse than simple balance UV
	Cx Open	Not measuring actual cell voltage
	Balance open	PCB connector to cell might have been lost
	HWSC	Is measurement reliable?
VBAT UV/OV	Cell UV/OV	If no cell is UV/OV, then it's not plausible
	Sum of Cells	Does the sum of cells confirm the UV/OV event?
	VBAT direct conversion and monitor	Is the conversion value actually reporting an OV/UV? Or is it just a transient OV/UV (as per VDA)?
	Cx Open	Summing wrong Cx contributions
	HWSC	Is measurement reliable?
GPIO UT/OT	GPIO open	Not measuring actual load voltage
	HWSC	Is measurement reliable?
	VTREF	Is the VTREF regulator working properly?
Fast Charge OT	GPIO open	Not measuring actual load voltage
	HWSC	Is measurement reliable?
	VTREF	Is the VTREF regulator working properly?
Cell open	HWSC	Is measurement reliable?
GPIO open	GPIO UT/OT	If connection to the external NTC is lost at the PCB connector, the GPIO will be pulled up to VTREF, thus causing GPIO UT detection. On the other hand, if the connection is lost at the device pin, the GPIO open internal diagnostic circuitry will detect it.
	HWSC	Is measurement reliable?
	VTREF	Is the VTREF regulator working properly?
Balance open	HWSC	Comparators must have correctly flagged open
PCB Connector open	Balance open	In case PCB connector to CELLx is open, then BALx and BALx+1 open failures will be flagged
HWSC	VREG UV/OV	BIST may have failed because supply is not in range. Checking VBAT and UV/OV comparators functionality is recommended.
	VBAT UV/OV	

Figure 26. **Example of configuration override: a failure detected during Cell Terminal diagnostics (yellow background) causes the following two steps (red background) to be executed**



4.12.3 Routine steps

The following paragraph will cover the functionality of each step embedded in the voltage conversion routine.

4.12.3.1 Cell conversion

Cell conversion is the first step of the voltage conversion routine. It is mandatory, meaning that it cannot be excluded from routine execution, neither in **On-Demand Conversions** nor in **Cyclic Conversions**.

During this step, all the enabled cells will be converted and their voltage will be added to obtain the total stack value.

Table 61. **Operations performed during cell conversion step**

Operation	Skip condition
C1-C0	VCELL1_EN = 0
C2-C1	VCELL2_EN = 0
C3-C2	VCELL3_EN = 0
C4-C3	VCELL4_EN = 0
C5-C4	VCELL5_EN = 0
C6-C5	VCELL6_EN = 0
C7-C6	VCELL7_EN = 0
C8-C7	VCELL8_EN = 0

Operation	Skip condition
C9-C8	VCELL9_EN = 0
C10-C9	VCELL10_EN = 0
C11-C10	VCELL11_EN = 0
C12-C11	VCELL12_EN = 0
C13-C12	VCELL13_EN = 0
C14-C13	VCELL14_EN = 0

The step duration is not fixed, since it lasts **TCYCLEADC**, thus depending on the value programmed in the **ADC_FILTER_SOC** or **ADC_FILTER_CYCLE** fields (refer to Table 38).

The following failures can be flagged during cell conversion step execution, thus causing **Configuration Override**:

- **VCELLX_UV**: if the voltage of the x-th cell is lower than the programmed UV threshold (V_{CELL_UV})
- **VCELLX_OV**: if the voltage of the x-th cell is higher than the programmed OV threshold (V_{CELL_OV})
- **VSUM_OV**: if summing all cells voltage the outcome is higher than the programmed OV threshold ($V_{BAT\_OV\ (SUM)}$)
- **VSUM_UV**: if summing all cells voltage the outcome is lower than the programmed UV threshold ($V_{BAT\_UV\ (SUM)}$)
- **VCELLX_BAL_UV (maskable)**: if the voltage of the x-th cell is lower than the programmed balance UV threshold (V_{CELL_UV} + $V_{CELL\_BAL\_UV\_\Delta}$)

4.12.3.2 *VBAT conversion*

VBAT pin conversion is the second step of the voltage conversion routine. It is mandatory, meaning that it cannot be excluded from routine execution, neither in **On-Demand Conversions** nor in **Cyclic Conversions**.

During this step, the voltage on VBAT pin will be converted.

The step duration is not fixed, since it lasts **TCYCLEADC**, thus depending on the value programmed in the **ADC_FILTER_SOC** or **ADC_FILTER_CYCLE** fields (refer to Table 38).

The following failures can be flagged during VBAT conversion step execution, thus causing **Configuration Override**:

- **VBATTCRIT_OV**: if the voltage converted is higher than the **$V_{BAT\_CRITICAL\_OV\_TH}$**.
- **VBATTCRIT_UV**: if the voltage converted is lower than the **$V_{BAT\_CRITICAL\_UV\_TH}$**.

4.12.3.3 *GPIO conversion*

GPIO conversion is the third step of the voltage conversion routine.

L9963E allows possible to provide either the absolute conversion or the ratiometric conversion with respect to **VTREF_MEAS**, based on GPIOx dedicated R/W SPI register bits **ratio_abs_x_sel**.

This step is optional:

- To include it in **On-Demand Conversions**, the **GPIO_CONV** bit must be set along with the **SOC** in the same SPI frame.
- To specify its periodicity in **Cyclic Conversions**, the **NCYCLE_GPIO** field must be programmed (refer to **Operations Periodicity**).

During this step, all the GPIO configured as analog inputs will be converted.

Table 62. Operations performed during GPIO conversion step

Operation	Skip condition
GPIO1	Always
GPIO2	Always
GPIO3	GPIO3_CONFIG != 00

Operation	Skip condition
GPIO4	GPIO4_CONFIG != 00
GPIO5	GPIO5_CONFIG != 00
GPIO6	GPIO6_CONFIG != 00
GPIO7	GPIO7_CONFIG != 00
GPIO8	GPIO8_CONFIG != 00
GPIO9	GPIO9_CONFIG != 00

The step duration is fixed: it lasts $T_{CYCLEADC\_000}$ (refer to Table 38).

The following failures can be flagged during GPIO conversion step execution, thus causing **Configuration Override**:

- **GPIOX_OT**: if the converted voltage is lower than the programmed UV/OT threshold (V_{GPIOAN_OT}).
- **GPIOX_UT**: if the converted voltage is higher than the programmed OV/UT threshold (V_{GPIOAN_UT}).
- **GPIOX_fastchg_OT**: if the converted voltage is lower than the programmed fast charge UV/OT threshold (V_{GPIOAN_OT} + $V_{GPIO\_FASTCH\_OT\_DELTA}$); this function can be masked with a dedicated bit (**Gpiox_fastchg_OT_MSK**).

4.12.3.4 *GPIO terminal diagnostics*

GPIO terminal diagnostics is the fourth step of the voltage conversion routine. It is optional:

- To include it in an **On-Demand Conversions**, the **GPIO_TERM_CONV** bit must be set along with the **SOC** in the same SPI frame.
- To specify its periodicity in **Cyclic Conversions**, the **NCYCLE_GPIO_TERM** field must be programmed (refer to Section 4.12.4 Operations periodicity).

During this step, the GPIO open diagnostic will be performed on all GPIOs configured as analog inputs.

Table 63. Operations performed during GPIO terminal diagnostics step

Operation	Skip condition
GPIO1 Open	Always
GPIO2 Open	Always
GPIO3 Open	GPIO3_CONFIG != 00
GPIO4 Open	GPIO4_CONFIG != 00
GPIO5 Open	GPIO5_CONFIG != 00
GPIO6 Open	GPIO6_CONFIG != 00
GPIO7 Open	GPIO7_CONFIG != 00
GPIO8 Open	GPIO8_CONFIG != 00
GPIO9 Open	GPIO9_CONFIG != 00

The step duration is fixed: it lasts $T_{GPIO\_OPEN\_SET}$ + $T_{CYCLEADC\_000}$ (refer to Table 38).

The following failure can be flagged during GPIO terminal diagnostics step execution, thus causing **Configuration Override**:

- **GPIOX_OPEN**: if $V_{GPIO} < V_{GPIO\_OL}$ while $I_{GPIO\_PD\_OPEN}$ is applied

4.12.3.5 *Cell terminal diagnostics*

Cell terminal diagnostics is the fifth step of the voltage conversion routine. It is optional and its execution mode depends on the **ADC_CROSS_CHECK** bit (refer to **Cell open wire diagnostic** for further information):

- To include it in **On-Demand Conversions**, the **CELL_TERM_CONV** bit must be set along with the **SOC** in the same SPI frame.

- To specify its periodicity in **Cyclic Conversions**, the **NCYCLE_CELL_TERM** field must be programmed (refer to Section 4.12.4 Operations periodicity).

During this step, the cell terminal open diagnostic will be performed on all enabled cells.

Table 64. Operations performed during cell terminal diagnostics step

Operation	Skip condition
C0 Open	VCELL1_EN = 0
C1 Open	VCELL1_EN = 0
C2 Open	VCELL2_EN = 0
C3 Open	VCELL3_EN = 0
C4 Open	VCELL4_EN = 0
C5 Open	VCELL5_EN = 0
C6 Open	VCELL6_EN = 0
C7 Open	VCELL7_EN = 0
C8 Open	VCELL8_EN = 0
C9 Open	VCELL9_EN = 0
C10 Open	VCELL10_EN = 0
C11 Open	VCELL11_EN = 0
C12 Open	VCELL12_EN = 0
C13 Open	VCELL13_EN = 0
C14 Open	VCELL14_EN = 0

The step duration is not fixed, since it lasts **2*(T_{CxOPEN_SET} + $T_{CYCLEADC}$)**, thus depending on the value programmed in the **ADC_FILTER_SOC** or **ADC_FILTER_CYCLE** fields (refer to Table 38).
The following failure can be flagged during cell terminal diagnostics step execution, thus causing **Configuration Override**:

- **CELLX_OPEN**: for all enabled cells, if the voltage drop on the path in series to the **Cx** pin becomes higher than **VCxOPEN**.

4.12.3.6 *Balance terminal diagnostics*

Balance terminal diagnostics is the sixth step of the voltage conversion routine. It is optional:

- To include it in **On-Demand Conversions**, the **BAL_TERM_CONV** bit must be set along with the **SOC** in the same SPI frame.
- To specify its periodicity in **Cyclic Conversions**, the **NCYCLE_BAL_TERM** field must be programmed (refer to Section 4.12.4 Operations periodicity).

During this step, the balance terminal open diagnostic will be performed on all the enabled cells.

Table 65. Operations performed during balance terminal diagnostics step

Operation	Skip condition
B2_1 – S1 Open / Short	VCELL1_EN = 0
S2 – B2_1 Open / Short	VCELL2_EN = 0
B4_3 – S3 Open / Short	VCELL3_EN = 0
S4 – B4_3 Open / Short	VCELL4_EN = 0
B6_5 – S5 Open / Short	VCELL5_EN = 0
S6 – B6_5 Open / Short	VCELL6_EN = 0

Operation	Skip condition
B8_7 – S7 Open / Short	VCELL7_EN = 0
S8 – B8_7 Open / Short	VCELL8_EN = 0
B10_9 – S9 Open / Short	VCELL9_EN = 0
S10 – B10_9 Open / Short	VCELL10_EN = 0
B12_11 – S11 Open / Short	VCELL11_EN = 0
S12 – B12_11 Open / Short	VCELL12_EN = 0
B14_13 – S13 Open / Short	VCELL13_EN = 0
S14 – B14_13 Open / Short	VCELL14_EN = 0

The step duration is fixed: it lasts **2*TBAL_OL**.

The following failure can be flagged during balance terminal diagnostics step execution, thus causing **Configuration Override**:

- **BALX_OPEN**: if the voltage drop on the V_{DS} of the balance power MOS becomes lower than $\mathbf{V_{BAL\_OPEN}}$.

4.12.3.7 *Hardware Self-Check (HWSC)*

HWSC is the seventh step of the voltage conversion routine. It is optional:

- To include it in **On-Demand Conversions**, the **HWSC** bit must be set along with the **SOC** in the same SPI frame.
- To specify its periodicity in **Cyclic Conversions**, the **NCYCLE_HWSC** field must be programmed (refer to Section 4.12.4 Operations periodicity).

During this step, a BIST will be executed on the enabled analog conversion paths to verify the functionality of the ADC chain. Analog comparators used for UV/OV detection and diagnostics will also be checked.

Table 66. Operations performed during HWSC step

Operation	Skip condition
CX to ADC	Never
GPIO3-9 to ADC	Never
VBAT UV/OV comparator	Never
VREG UV/OV comparator	Never
VCOM UV/OV comparator	Never
VTREF UV/OVcomparator	Never
Bx_x-1 to ADC	Never
Sx to ADC	Never
Bx_x-1/Sx-1 Open/Short comparator (even cells)	Never
Sx/Bx_x-1 Open/Short comparator (odd cells)	Never

The step duration is fixed: it lasts $\mathbf{3*T_{CYCLEADC\_000}}$ (refer to Table 38).

The following failures can be flagged during HWSC step execution, thus causing **Configuration Override**:

- **MUX_BIST_FAIL**: if a failure is found while converting the Cx paths connected to the analog MUX
- **OPEN_BIST_FAIL**: if a failure is found while converting the Sx/Bx_x-1 paths connected to the analog MUX
- **GPIO_BIST_FAIL**: if a failure is found while converting the GPIOx paths connected to the analog MUX
- **VBAT_COMP_BIST_FAIL**: if the BIST on the VBAT UV/OV comparator fails
- **VREG_COMP_BIST_FAIL**: if the BIST on the VREG UV/OV comparator fails
- **VCOM_COMP_BIST_FAIL**: if the BIST on the VCOM UV/OV comparator fails
- **VTREF_COMP_BIST_FAIL**: if the BIST on the VTREF UV/OV comparator fails

- **BIST_BAL_COMP_HS_FAIL**: if the BIST on the balance open/short comparator of the High Side switches fails (even cells)
- **BIST_BAL_COMP_LS_FAIL**: if the BIST on the balance open/short comparator of the Low Side switches fails (odd cells)

Once this step is over, the **HWSC_DONE** flag will be set in the SPI registers. It must be cleared upon read by MCU.

4.12.3.8 *Summary of the routine steps*

The following table summarizes all the actions performed during routine steps:

Table 67. Summary of the voltage conversion routine steps

Step	Optional	Actions	Duration	Skip based on	Failure
Cell Conversion	No	All enabled cells converted + Sum of Cells	$T_{CYCLEADC}$	VCELLX_EN	VCELLX_UV VCELLX_OV VSUM_UV VSUM_OV VCELLX_BAL_UV (maskable)
VBAT Conversion	No	VBAT pin direct conversion	$T_{CYCLEADC}$	VCELLX_EN	VBATTCRIT_OV VBATTCRIT_UV
GPIO Conversion	Yes	Conversion of all GPIOs configured as analog input	$T_{CYCLEADC\_000}$	GPIOX_CONFIG	GPIOX_OT GPIOX_UT GPIOX_fastchg_OT (maskable)
GPIO Terminal Diagnostics	Yes	Open diagnostic on all GPIOs configured as analog input	$T_{GPIO\_OPEN\_SET}$ + $T_{CYCLEADC\_000}$	GPIOX_CONFIG	GPIOX_OPEN
Cell Terminal Diagnostics	Yes	Open diagnostic on all terminals connected to enabled cells	$2(T_{CxOPEN\_SET}$ + $T_{CYCLEADC})$	VCELLX_EN	CELLX_OPEN
Balance Terminal Diagnostics	Yes	Open diagnostic on balance paths of enabled cells	$2T_{BAL\_OL}$	VCELLX_EN	BALX_OPEN
HardWare Self-Check (HWSC)	Yes	BIST on all enabled conversion paths + Analog comparators	$3T_{CYCLEADC\_000}$		MUX_BIST_FAIL OPEN_BIST_FAIL GPIO_BIST_FAIL VBAT_COMP_BIST_FAIL VREG_COMP_BIST_FAIL VCOM_COMP_BIST_FAIL VTREF_COMP_BIST_FAIL BIST_BAL_COMP_HS_FAIL BIST_BAL_COMP_LS_FAIL

4.12.4 Operations periodicity

While in cyclic execution (**CONF_CYCLIC_EN = 1**), each step periodicity can be programmed by acting on **TCYCLE** and **NCYCLE_X** fields:

In case of Cyclic Wake up, the wake up timer is set by **TCYCLE_SLEEP** instead of **TCYCLE**.

Table 68. TCYCLE and NCYCLE_X options

TCYCLE / TCYCLE_SLEEP	CYCLE PERIOD	NCYCLE_X	CYCLIC OCCURRENCE
000	100 ms	000	Excluded from voltage conversion routine
001	200 ms	001	Occurs every 1 cycle
010	400 ms	010	Occurs every 4 cycles
011	800 ms	011	Occurs every 16 cycles
100	1.6 s	100	Occurs every 64 cycles
101	3.2 s	101	Occurs every 128 cycles
110	6.4 s	110	Occurs every 512 cycles
111	12.8 s	111	Occurs every 1024 cycles

By combining the two fields, each step periodicity can be evaluated as follows:

Evaluation of a step periodicity

$$\begin{cases} T_{STEP} = N_{CYCLE_X} \times T_{CYCLE}, \text{ when not in continuous mode or overflow} \\ T_{STEP} = N_{CYCLE_X} \times T_{ROUTINE}, \text{ when in continuous mode or overflow} \end{cases} \quad (16)$$

The periodicity ranges from a minimum of 100 ms to a maximum of 3.64 hours (13107.2 s):

- Important functional checks such as HWSC might be executed with a high frequency
- Time consuming operations such as open load diagnostics might be performed with a low frequency

Table 69 lists all the available periodicity options, calculated according to Eq. (16) assuming L9963E is not in continuous mode or overflow:

Table 69. Steps periodicity options

	Tcycle							
Ncycle	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
000	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
001	100 ms	200 ms	400 ms	800 ms	1.6 s	3.2 s	6.4 s	12.8 s
010	400 ms	800 ms	1.6 s	3.2 s	6.4 s	12.8 s	25.6 s	51.2 s
011	1.6 s	3.2 s	6.4 s	12.8 s	25.6 s	51.2 s	102.4 s	204.8 s
100	6.4 s	12.8 s	25.6 s	51.2 s	102.4 s	204.8 s	409.6 s	819.2 s
101	12.8 s	25.6 s	51.2 s	102.4 s	204.8 s	409.6 s	819.2 s	1638.4 s
110	51.2 s	102.4 s	204.8 s	409.6 s	819.2 s	1638.4 s	3276.8 s	6553.6 s
111	102.4 s	204.8 s	409.6 s	819.2 s	1638.4 s	3276.8 s	6553.6 s	13107.2 s

Changing **NCYCLE_X** for a step while cyclic activity is enabled (**CONF_CYCLIC_EN = 1**) will cause the new setting to be applied at the first useful cycle (refer to Table 59).

Table 70. NCYCLE counter and optional step periodicity

		NCYCLE COUNTER (11 bit)										
		1024	512	256	128	64	32	16	8	4	2	1
		b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
STEP LIST	GPIO							X				
	GPIO Term					X						
	Cell Term		X									
	Bal Term							X				
	ADC BIST									X		
	Analog Comp	X										

The **NCYCLE** is an 11 bit counter. Optional steps can be configured (via their **NCYCLE_X**) to be executed every time a specific **bx** bit toggles. Once the counter reaches the saturation value (2047), it is designed to roll over. Hence, operation periodicity is not affected and may continue for an arbitrary number of cycles.

4.12.5 Transition between cyclic wake up and normal states

Any asynchronous event causing L9963E moving to low power states will have the following effect on the voltage conversion routine:

- If the **OVR_LATCH** is set, it means that a **Configuration Override** is ongoing or has occurred and the command is ignored. In fact, a **Configuration Override** cannot be interrupted. Moreover, L9963E is locked in **Normal** state upon failure detection. Hence, the microcontroller must clear the **OVR_LATCH** before transitioning to a different state. The microcontroller has a feedback that the command was discarded because:
  - The **FAULTL** line is risen in case of ***Configuration Override*** thus propagating the fault down to the micro.
  - The **Configuration Override** latch is set (**OVR_LATCH = 1**).
- However, if the MCU does not respond within the communication timeout, the device will move to sleep anyway.
- If no failure occurred, any ongoing conversion activity can be interrupted by a **GO2SLP** command. The device will immediately move to a low power state (**Sleep**, **Cyclic Wakeup** or **Silent Balance**).
- To determine the next state, the **CONF_CYCLIC_EN** bit will be evaluated:
  - In case **CONF_CYCLIC_EN = 1** L9963E will move to **Cyclic Wakeup** state, where the wakeup timer is **TCYCLE_SLEEP** and the voltage acquisition window ($T_{CYCLEADC}$) is **ADC_FILTER_SLEEP**. The **TCYCLE_OVF** failure is avoided by design, since the **ADC_FILTER_SLEEP** can be only programmed among the first 4 values listed in Table 38. This makes $T_{ROUTINE}$ **< TCYCLE_SLEEP** by design.
  - In case **CONF_CYCLIC_EN = 0** L9963E will move to **Sleep** or **Silent Bal** state depending on **slp_bal_conf**.

The dual case is represented by the **Cyclic Wakeup** → **Normal** transition. During cyclic wake up, a wake up condition may occur:

- If the wake up condition does not involve any **Configuration Override** (e.g. Microcontroller sent a wake up frame or **FAULTH** was interpreted ‘high’), then L9963E will move to **Normal** state and the cyclic activity will continue, since **CONF_CYCLIC_EN** is still ‘1’.
- In case an internal failure is detected during the routine execution, the internal wakeup condition will move L9963E to **Normal**, while **Configuration Override** takes place.

4.13 Coulomb counting routine

4.13.1 Coulomb counting

The Coulomb counting routine is performed to evaluate the charge injected / subtracted during vehicle operation. To enable it, the **CoulombCounter_en** bit must be set to **'1'**.

Disabling the Coulomb Counter by setting **CoulombCounter_en** to '**0**' doesn't reset the accumulator (**CoulombCounter_msb, CoulombCounter_lsb**) and sample counter (**CoulombCntTime**) registers. MCU is supposed to reset the Coulomb Counter, clearing any data previously stored, before enabling it.

This can be done by performing a burst read operation as explained below:

- When L9963E is in **Normal** state, current is continuously sampled: a new conversion starts as soon as the previous one has been completed. Each acquisition window lasts **TCYCLEADC_CUR**. Coulomb counter internal registers are accessible sending the **0x7B** command via SPI (refer to Table 23) and are updated at the end of each conversion.
  - To read the Coulomb Counter internal registers:
    - MCU sends the **0x7B** burst command (see Table 26).
    - At command receival, data is loaded from accumulator (**CoulombCounter_msb** and **CoulombCounter_lsb**) and sample counter (**CoulombCntTime**) registers and L9963E will answer with a burst containing also instantaneous current (**CUR_INST_calib**) and diagnostic data (**CoCouOvF**).
    - Meanwhile, both the accumulator and the sample counter are reset to zero.
    - MCU can then evaluate the charge variation ΔQ in the battery pack, by referring to a known previous state of charge Q(t0) and applying the following equation:

      Coulomb Counting algorithm

$$\begin{cases} Q(t_k) = Q_{t0} + \Delta Q = Q_{t0} + \Delta T \Sigma_{k=1}^{K} I_{CELL}(k) = Q_{t0} + \frac{\Delta T}{R_{SHUNT}} \Sigma_{k=1}^{K} V_{\mathrm{DIFF\_CUR\_SENSE}}(k) \\ \Delta T = T_{CYCLEADC\_CUR} \\ K = CoulombCntTime \\ \Sigma_{k=1}^{K} V_{\mathrm{DIFF\_CUR\_SENSE}}(k) = (\mathbf{CoulombCounter_{msb}} + \mathbf{CoulombCounter_{lsb}})|_{2's\ compl} * V_{ISENSE\_RES} \end{cases} \quad (17)$$

    - Then, the Q(tk) just evaluated becomes the Q(t0) for the next iteration
  - MCU must periodically read the Coulomb Counter in order to avoid accumulator or sample counter overflow (latched by **CoCouOvF** bit). In case a register overflows, it will saturate: **CoulombCntTime** saturates to 0xFFFF, while **CoulombCounter_msb/lsb** saturates either to the upper bound (0x7FFFFFFF) or to the lower bound (0x80000000). In case of saturation, activity will continue, but data will not be reliable. Recommended polling period is 1 s or less.
  - Reading the Coulomb Counter registers will not interrupt the Coulomb Counting Routine running in background.
  - If a current sample (absolute value) overcomes **ICURR_SENSE_OC_NORM** (programmable via SPI in the **adc_ovc_curr_threshold_norm** register), the **curr_sense_ovc_norm** flag is set and FAULTL pin is risen. This functionality is meant to detect overcurrent events that could damage the battery pack when the system ignition is ON.
  - This check can be masked by programming **ovc_norm_msk = 1**.
- When L9963E is in **Cyclic Wakeup** state, current is continuously sampled while the device is in the ON phase. If a current sample (absolute value) overcomes **ICURR_SENSE_OC_SLEEP** (programmable via SPI in the **adc_ovc_curr_threshold_sleep** register), the **curr_sense_ovc_sleep** flag is set, L9963E moves to **Normal** state and **FAULTL** pin is risen. This functionality is meant to detect anomalous current leakage from the battery pack when the system ignition is OFF.
  - This check can be masked by programming **ovc_sleep_msk = 1**.

When L9963E operates in **Cyclic Wakeup** and the Coulomb Counter is enabled, the ON phase ends when the Voltage Conversion Routine is over (**DUTY_ON = '0'**) and the Coulomb Counter has acquired at least one current sample.

5 Register map

The following paragraph contains the device register map.

Table 71. Register map legend

Field	Value	Description
Type	RO	Read Onlu
	RW	Read/Write
	WO	Write Only
	RLR	Latch Clear on Read
Reset Sources	A	POR Standby
	B	POR Main
	X	Undefined

Table 72. SPI register map

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
DEV_GEN_CFG	0x1							
		chip_ID	RW	13	5	0x0	A	All 0s → No address (Init state) X → Dev ID of SPI Protocol (L9963E SPI Protocol Details)
		isotx_en_h	RW	12	1	0x0	A	0 → ISOH port disabled 1 → ISOH port enabled
		out_res_tx_iso	RW	10	2	0x0	A	Selects ISOH/L port differential signal amplitude See Table 18
		iso_freq_sel	RW	8	2	0x0	B	Selects ISOH/L port carrier frequency See Table 18
		Noreg7	RO	7	1	0x0	X	
		HeartBeatCycle	RW	4	3	0x4	A	Selects heartbeat period See Table 37
		FaultH_EN	RW	3	1	0x0	A	Enables FAULTH receiver See Table 36
		HeartBeat_En	RW	2	1	0x0	B	Enables Heartbeat generation See Table 36
		Farthest_Unit	RW	1	1	0x0	A	Configures the unit as the stack topmost See Table 36
		FaultL_force	RW	0	1	0x0	B	0 → FAULTL not forced high 1 → FAULTL forced high

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
fastch_baluv	**0x2**							
		CommTimeout	RW	16	2	0x0	A	Configures the communication timeout See Table 11
		Gpio_fastchg_OT_delta_thr	RW	8	8	0x0	A	Determines the fastcharge overtemperature threshold See Table 48
		Vcell_bal_UV_delta_thr	RW	0	8	0x0	A	Determines the balancing undervoltage threshold See Table 39
Bal_1	**0x3**							
		comm_timeout_dis	RW	17	1	0x0	A	0 → Communication timeout enabled 1 → Communication timeout disabled
		slp_bal_conf	RW	16	1	0x0	A	0 → Silent balancing disabled 1 → Silent balancing enabled
		bal_start	RW	15	1	0x0	A	10 → balancing start 01 → balancing stop Others → no effect
		bal_stop	RW	14	1	0x0	A	
		TimedBalTimer	RO	7	7	0x0	A	Balancing timer. Resolution depends on TimedBalacc See Table 43
		WDTimedBalTimer	RO	0	7	0x0	A	Balancing timer watchdog. Resolution depends on TimedBalacc See Table 43
Bal_2	**0x4**							
		Balmode	RW	16	2	0x1	A	01 → Manual balancing 10 → Timed balancing Others → No effect
		TimedBalacc	RW	15	1	0x0	A	Selects balancing timer resolution See Table 43
		ThrTimedBalCell14	RW	8	7	0x0	A	Timed balancing threshold for cell 14
		Noreg7	RO	7	1	0x0	X	
		ThrTimedBalCell13	RW	0	7	0x0	A	Timed balancing threshold for cell 13
Bal_3	**0x5**							
		first_wup_done	RO	17	1	0x0	A	0 → First powerup not properly done 1 → First powerup ended successfully
		trimming_retrigger	RW	16	1	0x0	B	Triggers NVM download Refer to Section 4.10.1 NVM read
		Lock_isoh_isofreq	RW	15	1	0x0	B	0 → isotx_en_h and iso_freq_sel are unlocked

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
								1 → isotx_en_h and iso_freq_sel are write protected
		ThrTimedBalCell12	RW	8	7	0x0	A	Timed balancing threshold for cell 12
		Noreg7	RO	7	1	0x0	X	
		ThrTimedBalCell11	RW	0	7	0x0	A	Timed balancing threshold for cell 11
Bal_4	**0x6**							
		clk_mon_en	RW	17	1	0x0	A	0 → Main oscillator monitor disabled 1 → Main oscillator monitor enabled
		Noreg16	RW	16	1	0x0	A	
		clk_mon_init_done	RO	15	1	0x0	B	0 → Main oscillator monitor not started 1 → Main oscillator monitor started
		ThrTimedBalCell10	RW	8	7	0x0	A	Timed balancing threshold for cell 10
		Noreg7	RO	7	1	0x0	X	
		ThrTimedBalCell9	RW	0	7	0x0	A	Timed balancing threshold for cell 9
Bal_5	**0x7**							
		transceiver_on_by_up	RW	17	1	0x0	A	0 → Transceiver mode not forced by MCU 1 → Transceiver mode forced by MCU
		transceiver_valid_by_up	RW	16	1	0x0	A	0 → Value on transceiver_on_by_up discarded 1 → Value on transceiver_on_by_up applied to device configuration
		Noreg15	RO	15	1	0x0	X	
		ThrTimedBalCell8	RW	8	7	0x0	A	Timed balancing threshold for cell 8
		Noreg7	RO	7	1	0x0	X	
		ThrTimedBalCell7	RW	0	7	0x0	A	Timed balancing threshold for cell 7
Bal_6	**0x8**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		ThrTimedBalCell6	RW	8	7	0x0	A	Timed balancing threshold for cell 6
		Noreg7	RO	7	1	0x0	X	
		ThrTimedBalCell5	RW	0	7	0x0	A	Timed balancing threshold for cell 5
Bal_7	**0x9**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		ThrTimedBalCell4	RW	8	7	0x0	A	Timed balancing threshold for cell 4

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		Noreg7	RO	7	1	0x0	X	
		ThrTimedBalCell3	RW	0	7	0x0	A	Timed balancing threshold for cell 3
Bal_8	**0xA**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		ThrTimedBalCell2	RW	8	7	0x0	A	Timed balancing threshold for cell 2
		Noreg7	RO	7	1	0x0	X	
		ThrTimedBalCell1	RW	0	7	0x0	A	Timed balancing threshold for cell 1
VCELL_THRESH_UV_OV	**0xB**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		threshVcellOV	RW	8	8	0x0	A	Determines cell overvoltage threshold Cell Voltage ADC electrical characteristics See Table 39
		threshVcellUV	RW	0	8	0x0	A	Determines cell undervoltage threshold See Table 39
VBATT_SUM_TH	**0xC**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		VBATT_SUM_OV_TH	RW	8	8	0x0	A	Determines battery stack overvoltage threshold See Table 40
		VBATT_SUM_UV_TH	RW	0	8	0x0	A	Determines battery stack undervoltage threshold See Table 40
ADCV_CONV	**0xD**							
		ADC_CROSS_CHECK	RW	17	1	0x0	A	0 → Cell open diagnostics executed during Cx open check 1 → ADC Cross check executed during Cx open check
		TCYCLE_OVF	RLR	16	1	0x0	B	0 → No period overflow detected during cyclic conversions 1 → Period overflow detected during cyclic conversions
		SOC	WO	15	1	0x0	B	0 → No on-demand conversion 1 → Triggers on-demand conversion
		OVR_LATCH	RLR	14	1	0x0	B	0 → No configuration override occurred

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
								1 → Configuration override occurred
		CONF_CYCLIC_EN	RW	13	1	0x0	A	0 → Cyclic conversions disabled 1 → Cyclic conversions enabled
		DUTY_ON	RO	12	1	0x0	B	0 → No conversion ongoing 1 → Conversion ongoing
		ADC_FILTER_SOC	RW	9	3	0x0	B	Determines the filter window used for on-demand conversions. See Table 39
		GPIO_CONV	WO	8	1	0x0	B	0 → GPIO conversion disabled for on-demand conversion 1 → GPIO conversion performed during on-demand conversion
		GPIO_TERM_CONV	WO	7	1	0x0	B	0 → GPIO open check disabled for on-demand conversion 1 → GPIO open check performed during on-demand conversion
		CELL_TERM_CONV	WO	6	1	0x0	B	0 → Cx open check disabled for on-demand conversion 1 → Cx open check performed during on-demand conversion
		BAL_TERM_CONV	WO	5	1	0x0	B	0 → Balancing open check disabled for on-demand conversion 1 → Balancing open check performed during on-demand conversion
		HWSC	WO	4	1	0x0	B	0 → HWSC disabled for on-demand conversion 1 → HWSC performed during on-demand conversion
		TCYCLE	RW	1	3	0x0	A	Determines the period of cyclic conversions executed in Normal state. See Table 68
		CYCLIC_CONTINOUS	RW	0	1	0x0	A	0 → Cyclic conversions triggered periodically by TCYCLE timer 1 → Cyclic conversions performed continuously
NCYCLE_PROG_1	**0xE**							
		T_CELL_SET	RW	16	2	0x0	A	00 → No settling time 01 → 175 µs settling time 10 → 350 µs settling time 11 → 700 µs settling time
		NCYCLE_GPIO_TERM	RW	13	3	0x0	A	Determines GPIO open check periodicity during cyclic executions See Table 68

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		NCYCLE_CELL_TERM	RW	10	3	0x0	A	Determines Cx open check periodicity during cyclic executions See Table 68
		NCYCLE_BAL_TERM	RW	7	3	0x0	A	Determines Balancing open check periodicity during cyclic executions See Table 68
		BAL_TIM_AUTO_PAUSE	RW	6	1	0x0	A	0 → Balancing timer not frozen during balancing auto pause 1 → Balancing timer frozen during balancing auto pause
		BAL_AUTO_PAUSE	RW	5	1	0x1	A	0 → Balancing auto pause disabled 1 → Balancing auto pause enabled
		CYCLIC_UPDATE	RW	4	1	0x0	A	0 → Measurement registers not updated during cyclic conversions 1 → Measurement registers updated during cyclic conversions
		CROSS_ODD_EVEN_CELL	RW	3	1	0x0	B	0 → ADCs not swapped 1 → ADCs swapped
		PCB_open_en_odd_curr	RW	2	1	0x0	B	0 → PCB open diagnostic current disabled on odd cells 1 → PCB open diagnostic current enabled on odd cells
		PCB_open_en_even_curr	RW	1	1	0x0	B	0 → PCB open diagnostic current disabled on even cells 1 → PCB open diagnostic current enabled on even cells
		Noreg0	RO	0	1	0x0	X	
NCYCLE_PROG_2	**0xF**							
		VTREF_EN	RW	17	1	0x0	A	0 → VTREF regulator disabled 1 → VTREF regulator enabled
		VTREF_DYN_EN	RW	16	1	0x0	A	0 → VTREF regulator always ON 1 → VTREF regulator turned ON only during Voltage Conversion Routine
		NCYCLE_GPIO	RW	13	3	0x0	A	Determines GPIO measurement periodicity during cyclic executions See Table 68
		NCYCLE_HWSC	RW	10	3	0x0	A	Determines HWSC periodicity during cyclic executions See Table 68
		Noreg9	RO	9	1	0x0	X	
		ADC_FILTER_CYCLE	RW	6	3	0x0	A	Determines the filter window used for cyclic conversion in Normal state. See Table 39

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		TCYCLE_SLEEP	RW	3	3	0x0	A	Determines the period of cyclic conversions executed in cyclic wake up. See Table 68
		ADC_FILTER_SLEEP	RW	0	3	0x0	A	Determines the filter window used for cyclic conversion in cyclic wake up state. See Table 39
BalCell14_7act	**0x10**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		BAL14	RW	14	2	0x1	A	10 → Balancing enabled Others → Balancing disabled
		BAL13	RW	12	2	0x1	A	
		BAL12	RW	10	2	0x1	A	
		BAL11	RW	8	2	0x1	A	
		BAL10	RW	6	2	0x1	A	
		BAL9	RW	4	2	0x1	A	
		BAL8	RW	2	2	0x1	A	
		BAL7	RW	0	2	0x1	A	
BalCell6_1act	**0x11**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		BAL6	RW	14	2	0x1	A	10 → Balancing enabled Others → Balancing disabled
		BAL5	RW	12	2	0x1	A	
		BAL4	RW	10	2	0x1	A	
		BAL3	RW	8	2	0x1	A	
		BAL2	RW	6	2	0x1	A	
		BAL1	RW	4	2	0x1	A	
		Noreg3	RO	3	1	0x0	X	
		Noreg2	RO	2	1	0x0	X	
		bal_on	RO	1	1	0x0	A	See Table 42
		eof_bal	RO	0	1	0x0	A	
FSM	**0x12**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		SW_RST	WO	14	2	0x0	B	10 → Triggers software reset Others → No effect
		GO2SLP	WO	12	2	0x0	B	10 → Moves the device to sleep Others → No effect

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		FSMstatus	RO	8	4	0x0	B	0001 → Sleep 0010 → Init 0100 → Normal 1000 → Cyclic wake up
		Noreg7	RO	7	1	0x0	X	
		Noreg6	RO	6	1	0x0	X	
		Noreg5	RO	5	1	0x0	X	
		wu_gpio7	RO	4	1	0x0	B	0 → Last wake up source was not GPIO7 1 → Last wake up source was GPIO7
		wu_spi	RO	3	1	0x0	B	0 → Last wake up source was not SPI 1 → Last wake up source was SPI
		wu_isoline	RO	2	1	0x0	B	0 → Last wake up source was not isolated SPI 1 → Last wake up source was isolated SPI
		wu_faulth	RO	1	1	0x0	B	0 → Last wake up source was not FAULTH 1 → Last wake up source was FAULTH
		wu_cyc_wup	RO	0	1	0x0	B	0 → Last wake up source was not TCYCLE_SLEEP 1 → Last wake up source was TCYCLE_SLEEP
GPOxOn_and_GPI93	**0x13**							
		GPO9on	RW	17	1	0x0	B	0 → GPIO forced low 1 → GPIO forced high
		GPO8on	RW	16	1	0x0	B	
		GPO7on	RW	15	1	0x0	B	
		GPO6on	RW	14	1	0x0	B	
		GPO5on	RW	13	1	0x0	B	
		GPO4on	RW	12	1	0x0	B	
		GPO3on	RW	11	1	0x0	B	
		Noreg10	RO	10	1	0x0	X	
		Noreg9	RO	9	1	0x0	X	
		GPI9	RO	8	1	0x0	B	Value read on GPIO
		GPI8	RO	7	1	0x0	B	
		GPI7	RO	6	1	0x0	B	
		GPI6	RO	5	1	0x0	B	
		GPI5	RO	4	1	0x0	B	
		GPI4	RO	3	1	0x0	B	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		GPI3	RO	2	1	0x0	B	Value read on GPIO
		Noreg1	RO	1	1	0x0	X	
		Noreg0	RO	0	1	0x0	X	
GPIO9_3_CONF	**0x14**							
		GPIO9_CONFIG	RW	16	2	0x0	A	00 → Analog input 01 → Not to be used 10 → Digital input 11 → Digital output
		GPIO8_CONFIG	RW	14	2	0x2	A	
		GPIO7_CONFIG	RW	12	2	0x2	A	
		GPIO6_CONFIG	RW	10	2	0x0	A	
		GPIO5_CONFIG	RW	8	2	0x0	A	
		GPIO4_CONFIG	RW	6	2	0x0	A	
		GPIO3_CONFIG	RW	4	2	0x0	A	
		GPIO7_WUP_EN	RW	3	1	0x0	A	0 → GPIO7 not used as wake up input 1 → GPIO7 used as wake up input
		Noreg2	RO	2	1	0x0	X	
		Noreg1	RO	1	1	0x0	X	
		Noreg0	RO	0	1	0x0	X	
GPIO3_THR	**0x15**							
		GPIO3_OT_TH	RW	9	9	0x0	A	Determines GPIO3 overtemperature threshold See Table 48
		GPIO3_UT_TH	RW	0	9	0x0	A	Determines GPIO3 undertemperature threshold See Table 48
GPIO4_THR	**0x16**							
		GPIO4_OT_TH	RW	9	9	0x0	A	Determines GPIO4 overtemperature threshold See Table 48
		GPIO4_UT_TH	RW	0	9	0x0	A	Determines GPIO4 undertemperature threshold See Table 48
GPIO5_THR	**0x17**							
		GPIO5_OT_TH	RW	9	9	0x0	A	Determines GPIO5 overtemperature threshold See Table 48
		GPIO5_UT_TH	RW	0	9	0x0	A	Determines GPIO5 undertemperature threshold See Table 48
GPIO6_THR	**0x18**							
		GPIO6_OT_TH	RW	9	9	0x0	A	Determines GPIO6 overtemperature threshold

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
								See Table 48
		GPIO6_UT_TH	RW	0	9	0x0	A	Determines GPIO6 undertemperature threshold See Table 48
GPIO7_THR	**0x19**							
		GPIO7_OT_TH	RW	9	9	0x0	A	Determines GPIO7 overtemperature threshold See Table 48
		GPIO7_UT_TH	RW	0	9	0x0	A	Determines GPIO7 undertemperature threshold See Table 48
GPIO8_THR	**0x1A**							
		GPIO8_OT_TH	RW	9	9	0x0	A	Determines GPIO8 overtemperature threshold See Table 48
		GPIO8_UT_TH	RW	0	9	0x0	A	Determines GPIO8 undertemperature threshold See Table 48
GPIO9_THR	**0x1B**							
		GPIO9_OT_TH	RW	9	9	0x0	A	Determines GPIO9 overtemperature threshold See Table 48
		GPIO9_UT_TH	RW	0	9	0x0	A	Determines GPIO9 undertemperature threshold See Table 48
VCELLS_EN	**0x1C**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	
		VCELL14_EN	RW	13	1	0x0	A	
		VCELL13_EN	RW	12	1	0x0	A	
		VCELL12_EN	RW	11	1	0x0	A	
		VCELL11_EN	RW	10	1	0x0	A	
		VCELL10_EN	RW	9	1	0x0	A	0 → Cell disabled 1 → Cell enabled
		VCELL9_EN	RW	8	1	0x0	A	
		VCELL8_EN	RW	7	1	0x0	A	
		VCELL7_EN	RW	6	1	0x0	A	
		VCELL6_EN	RW	5	1	0x0	A	
		VCELL5_EN	RW	4	1	0x0	A	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		VCELL4_EN	RW	3	1	0x0	A	0 → Cell disabled 1 → Cell enabled
		VCELL3_EN	RW	2	1	0x0	A	
		VCELL2_EN	RW	1	1	0x0	A	
		VCELL1_EN	RW	0	1	0x0	A	
Faultmask	**0x1D**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	
		VCELL14_BAL_UV_MSK	RW	13	1	0x0	A	0 → Balancing undervoltage not masked 1 → Balancing undervoltage masked
		VCELL13_BAL_UV_MSK	RW	12	1	0x0	A	
		VCELL12_BAL_UV_MSK	RW	11	1	0x0	A	
		VCELL11_BAL_UV_MSK	RW	10	1	0x0	A	
		VCELL10_BAL_UV_MSK	RW	9	1	0x0	A	
		VCELL9_BAL_UV_MSK	RW	8	1	0x0	A	
		VCELL8_BAL_UV_MSK	RW	7	1	0x0	A	
		VCELL7_BAL_UV_MSK	RW	6	1	0x0	A	
		VCELL6_BAL_UV_MSK	RW	5	1	0x0	A	
		VCELL5_BAL_UV_MSK	RW	4	1	0x0	A	
		VCELL4_BAL_UV_MSK	RW	3	1	0x0	A	
		VCELL3_BAL_UV_MSK	RW	2	1	0x0	A	
		VCELL2_BAL_UV_MSK	RW	1	1	0x0	A	
		VCELL1_BAL_UV_MSK	RW	0	1	0x0	A	
Faultmask2	**0x1E**							
		EEPROM_DWNLD_DONE	RO	17	1	0x0	A	0 → NVM not downloaded 1 → NVM downloaded
		EEPROM_CRC_ERR_SECT_0	RO	16	1	0x0	A	0 → No CRC error in trimming data 1 → CRC error in trimming data
		EEPROM_CRC_ERRMSK_SECT_0	RW	15	1	0x0	A	0 → CRC error in trimming data not masked 1 → CRC error in trimming data masked
		EEPROM_CRC_ERR_CAL_RAM	RO	14	1	0x0	A	0 → No CRC error in voltage calibration data 1 → CRC error in voltage calibration data
		EEPROM_CRC_ERRMSK_CAL_RAM	RW	13	1	0x0	A	0 → CRC error in voltage calibration data not masked 1 → CRC error in voltage calibration data masked

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		EEPROM_CRC_ERR_CAL_FF	RO	12	1	0x0	A	0 → No CRC error in current calibration data 1 → CRC error in current calibration data
		EEPROM_CRC_ERRMSK_CAL_FF	RW	11	1	0x0	A	0 → CRC error in current calibration data not masked 1 → CRC error in current calibration data masked
		RAM_CRC_ERR	RLR	10	1	0x0	A	0 → No CRC error in RAM content 1 → CRC error in RAM content
		RAM_CRC_ERRMSK	RW	9	1	0x0	A	0 → CRC error in RAM content not masked 1 → CRC error in RAM content masked
		trim_dwnl_tried	RO	8	1	0x0	A	0 → No attempt to download NVM was executed 1 → Attempt to download NVM executed
		TrimmCalOk	RO	7	1	0x0	A	0 → Trimming and calibration data are corrupted 1 → Trimming and calibration data are integer
		Gpio9_fastchg_OT_MSK	RW	6	1	0x0	A	0 → GPIO fast charge overtemperature not masked 1 → GPIO fast charge overtemperature masked
		Gpio8_fastchg_OT_MSK	RW	5	1	0x0	A	
		Gpio7_fastchg_OT_MSK	RW	4	1	0x0	A	
		Gpio6_fastchg_OT_MSK	RW	3	1	0x0	A	
		Gpio5_fastchg_OT_MSK	RW	2	1	0x0	A	
		Gpio4_fastchg_OT_MSK	RW	1	1	0x0	A	
		Gpio3_fastchg_OT_MSK	RW	0	1	0x0	A	
CSA_THRESH_NORM	**0x1F**							
		adc_ovc_curr_threshold_norm	RW	0	18	0x0	A	Determines the CSA overcurrent threshold in Normal state See Table 41
CSA_GPIO_MSK	**0x20**							
		adc_ovc_curr_threshold_sleep	RW	13	5	0x0	A	Determines the CSA overcurrent threshold in Cyclic wake up state See Table 41
		CoulombCounter_en	RW	12	1	0x0	A	0 → Coulomb Counter disabled 1 → Coulomb Counter enabled
		ovc_sleep_msk	RW	11	1	0x0	A	0 → CSA overcurrent in cyclic wake up not masked 1 → CSA overcurrent in cyclic wake up masked

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		ovc_norm_msk	RW	10	1	0x0	A	0 → CSA overcurrent in normal not masked 1 → CSA overcurrent in normal masked
		sense_plus_open	RLR	9	1	0x0	B	0 → Open failure not detected on CSA non-inverting input 1 → Open failure detected on CSA non-inverting input
		sense_minus_open	RLR	8	1	0x0	B	0 → Open failure not detected on CSA inverting input 1 → Open failure detected on CSA inverting input
		Noreg7	RO	7	1	0x0	X	
		Gpio9_OT_UT_MSK	RW	6	1	0x0	A	0 → GPIO over/under temperature not masked 1 → GPIO over/under temperature masked
		Gpio8_OT_UT_MSK	RW	5	1	0x0	A	
		Gpio7_OT_UT_MSK	RW	4	1	0x0	A	
		Gpio6_OT_UT_MSK	RW	3	1	0x0	A	
		Gpio5_OT_UT_MSK	RW	2	1	0x0	A	
		Gpio4_OT_UT_MSK	RW	1	1	0x0	A	
		Gpio3_OT_UT_MSK	RW	0	1	0x0	A	
Vcell1	**0x21**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell1	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell1	RO	0	16	0x0	B	Cell 1 voltage measurement
Vcell2	**0x22**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell2	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell2	RO	0	16	0x0	B	Cell 2 voltage measurement
Vcell3	**0x23**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell3	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell3	RO	0	16	0x0	B	Cell 3 voltage measurement
Vcell4	**0x24**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell4	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell4	RO	0	16	0x0	B	Cell 4 voltage measurement

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
Vcell5	**0x25**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell5	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell5	RO	0	16	0x0	B	Cell 5 voltage measurement
Vcell6	**0x26**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell6	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell6	RO	0	16	0x0	B	Cell 6 voltage measurement
Vcell7	**0x27**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell7	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell7	RO	0	16	0x0	B	Cell 7 voltage measurement
Vcell8	**0x28**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell8	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell8	RO	0	16	0x0	B	Cell 8 voltage measurement
Vcell9	**0x29**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell9	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell9	RO	0	16	0x0	B	Cell 9 voltage measurement
Vcell10	**0x2A**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell10	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell10	RO	0	16	0x0	B	Cell 10 voltage measurement
Vcell11	**0x2B**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell11	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell11	RO	0	16	0x0	B	Cell 11 voltage measurement
Vcell12	**0x2C**							
		Noreg17	RO	17	1	0x0	X	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		d_rdy_Vcell12	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell12	RO	0	16	0x0	B	Cell 12 voltage measurement
Vcell13	**0x2D**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell13	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell13	RO	0	16	0x0	B	Cell 13 voltage measurement
Vcell14	**0x2E**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_Vcell14	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VCell14	RO	0	16	0x0	B	Cell 14 voltage measurement
Ibattery_synch	**0x2F**							
		CUR_INST_Synch	RO	0	18	0x0	B	Pack current sample synchronized with last on-demand conversion
Ibattery_calib	0x30							
		CUR_INST_calib	RO	0	18	X	B	Pack current sample continuously updated
CoulCntrTime	**0x31**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		CoulombCntTime	RO	0	16	0x0	B	Number of current samples acquired
CoulCntr_msb	**0x32**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		CoulombCounter_msb	RO	0	16	0x0	B	Current sample accumulator (MSB)
CoulCntr_lsb	**0x33**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		CoulombCounter_lsb	RO	0	16	0x0	B	Current sample accumulator (LSB)
GPIO3_MEAS	**0x34**							
		ratio_abs_3_sel	RW	17	1	0x0	A	0 → Absolute value 1 → Ratiometric value
		d_rdy_gpio3	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		GPIO3_MEAS	RO	0	16	0x0	B	GPIO 3 measurement data

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
GPIO4_MEAS	**0x35**							
		ratio_abs_4_sel	RW	17	1	0x0	A	0 → Absolute value 1 → Ratiometric value
		d_rdy_gpio4	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		GPIO4_MEAS	RO	0	16	0x0	B	GPIO 4 measurement data
GPIO5_MEAS	**0x36**							
		ratio_abs_5_sel	RW	17	1	0x0	A	0 → Absolute value 1 → Ratiometric value
		d_rdy_gpio5	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		GPIO5_MEAS	RO	0	16	0x0	B	GPIO 5 measurement data
GPIO6_MEAS	**0x37**							
		ratio_abs_6_sel	RW	17	1	0x0	A	0 → Absolute value 1 → Ratiometric value
		d_rdy_gpio6	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		GPIO6_MEAS	RO	0	16	0x0	B	GPIO 6 measurement data
GPIO7_MEAS	**0x38**							
		ratio_abs_7_sel	RW	17	1	0x0	A	0 → Absolute value 1 → Ratiometric value
		d_rdy_gpio7	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		GPIO7_MEAS	RO	0	16	0x0	B	GPIO 7 measurement data
GPIO8_MEAS	**0x39**							
		ratio_abs_8_sel	RW	17	1	0x0	A	0 → Absolute value 1 → Ratiometric value
		d_rdy_gpio8	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		GPIO8_MEAS	RO	0	16	0x0	B	GPIO 8 measurement data
GPIO9_MEAS	**0x3A**							
		ratio_abs_9_sel	RW	17	1	0x0	A	0 → Absolute value 1 → Ratiometric value
		d_rdy_gpio9	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		GPIO9_MEAS	RO	0	16	0x0	B	GPIO 9 measurement data
TempChip	**0x3B**							
		Noreg17	RO	17	1	0x0	X	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	
		Noreg13	RO	13	1	0x0	X	
		Noreg12	RO	12	1	0x0	X	
		Noreg11	RO	11	1	0x0	X	
		Noreg10	RO	10	1	0x0	X	
		Noreg9	RO	9	1	0x0	X	
		OTchip	RLR	8	1	0x0	B	0 → No chip overtemperature detected 1 → Chip overtemperature detected
		TempChip	RO	0	8	0x0	B	Device temperature data
Faults1	**0x3C**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	
		VANA_OV	RLR	13	1	0x0	B	0 → VANA overvoltage not detected 1 → VANA overvoltage detected
		VDIG_OV	RLR	12	1	0x0	B	0 → VDIG overvoltage not detected 1 → VDIG overvoltage detected
		VTREF_UV	RLR	11	1	0x0	B	0 → VTREF undervoltage not detected 1 → VTREF undervoltage detected
		VTREF_OV	RLR	10	1	0x0	B	0 → VTREF overvoltage not detected 1 → VTREF overvoltage detected
		VREG_UV	RLR	9	1	0x0	B	0 → VREG undervoltage not detected 1 → VREG undervoltage detected
		VREG_OV	RLR	8	1	0x0	B	0 → VREG overvoltage not detected 1 → VREG overvoltage detected
		VCOM_OV	RLR	7	1	0x0	B	0 → VCOM overvoltage not detected 1 → VCOM overvoltage detected
		VCOM_UV	RLR	6	1	0x0	B	0 → VCOM undervoltage not detected 1 → VCOM undervoltage detected
		HeartBeat_fault	RLR	5	1	0x0	B	0 → Heartbeat absence not detected 1 → Heartbeat absence detected
		FaultHline_fault	RLR	4	1	0x0	B	0 → No fault incoming from upper level

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
								1 → Fault incoming from upper level
		Fault_L_line_status	RO	3	1	0x0	B	Reads FAULTL pin value
		Noreg2	RO	2	1	0x0	X	
		Noreg1	RO	1	1	0x0	X	
		Comm_timeout_flt	RLR	0	1	0x0	A	0 → Communication timeout not expired 1 → Communication timeout expired
Faults2	**0x3D**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	
		Noreg13	RO	13	1	0x0	X	
		SPIENlatch	RO	12	1	0x0	A	Value latched on SPIEN at powerup
		Noreg11	RO	11	1	0x0	X	
		OSCFail	RLR	10	1	0x0	B	0 → Main oscillator not stuck/out of range 1 → Main oscillator stuck/out of range
		Noreg9	RO	9	1	0x0	X	
		loss_agnd	RLR	8	1	0x0	B	0 → GND not lost 1 → GND lost
		loss_dgnd	RLR	7	1	0x0	B	
		loss_cgnd	RLR	6	1	0x0	B	
		loss_gndref	RLR	5	1	0x0	B	
		Noreg4	RO	4	1	0x0	X	
		CoCouOvF	RLR	3	1	0x0	B	0 → Coulomb Counter not overflown 1 → Coulomb Counter overflown
		EoBtimeerror	RLR	2	1	0x0	A	0 → No error detected between balancing timers 1 → Error detected between watchdog and primary balancing timer
		curr_sense_ovc_sleep	RLR	1	1	0x0	B	0 → CSA overcurrent not detected during cyclic wake up 1 → CSA overcurrent detected during cyclic wake up
		curr_sense_ovc_norm	RLR	0	1	0x0	B	0 → CSA overcurrent not detected during normal state 1 → CSA overcurrent detected during normal state
BAL_OPEN	**0x3E**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		BAL14_OPEN	RLR	15	1	0x0	B	
		BAL13_OPEN	RLR	14	1	0x0	B	
		BAL12_OPEN	RLR	13	1	0x0	B	
		BAL11_OPEN	RLR	12	1	0x0	B	
		BAL10_OPEN	RLR	11	1	0x0	B	
		BAL9_OPEN	RLR	10	1	0x0	B	
		BAL8_OPEN	RLR	9	1	0x0	B	0 → Balancing open not detected
		BAL7_OPEN	RLR	8	1	0x0	B	1 → Balancing open detected
		BAL6_OPEN	RLR	7	1	0x0	B	
		BAL5_OPEN	RLR	6	1	0x0	B	
		BAL4_OPEN	RLR	5	1	0x0	B	
		BAL3_OPEN	RLR	4	1	0x0	B	
		BAL2_OPEN	RLR	3	1	0x0	B	
		BAL1_OPEN	RLR	2	1	0x0	B	
		Noreg1	RO	1	1	0x0	X	
		Noreg0	RO	0	1	0x0	X	
BAL_SHORT	**0x3F**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		BAL14_SHORT	RLR	15	1	0x0	B	
		BAL13_SHORT	RLR	14	1	0x0	B	
		BAL12_SHORT	RLR	13	1	0x0	B	
		BAL11_SHORT	RLR	12	1	0x0	B	
		BAL10_SHORT	RLR	11	1	0x0	B	
		BAL9_SHORT	RLR	10	1	0x0	B	
		BAL8_SHORT	RLR	9	1	0x0	B	0 → Balancing short not detected
		BAL7_SHORT	RLR	8	1	0x0	B	1 → Balancing short detected
		BAL6_SHORT	RLR	7	1	0x0	B	
		BAL5_SHORT	RLR	6	1	0x0	B	
		BAL4_SHORT	RLR	5	1	0x0	B	
		BAL3_SHORT	RLR	4	1	0x0	B	
		BAL2_SHORT	RLR	3	1	0x0	B	
		BAL1_SHORT	RLR	2	1	0x0	B	
		Noreg1	RO	1	1	0x0	X	
		Noreg0	RO	0	1	0x0	X	
VSUMBATT	**0x40**							
		vsum_batt19_2	RO	0	18	0x0	B	Digital sum of cells (MSB)

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
VBATTDIV	**0x41**							
		vsum_batt1_0	RO	16	2	0x0	B	Digital sum of cells (LSB)
		VBATT_DIV	RO	0	16	0x0	B	VBAT direct conversion data
CELL_OPEN	**0x42**							
		data_ready_vsum	RLR	17	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		data_ready_vbattdiv	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		Noreg15	RLR	15	1	0x0	B	
		CELL14_OPEN	RLR	14	1	0x0	B	0 → Cx open not detected 1 → Cx open detected
		CELL13_OPEN	RLR	13	1	0x0	B	
		CELL12_OPEN	RLR	12	1	0x0	B	
		CELL11_OPEN	RLR	11	1	0x0	B	
		CELL10_OPEN	RLR	10	1	0x0	B	
		CELL9_OPEN	RLR	9	1	0x0	B	
		CELL8_OPEN	RLR	8	1	0x0	B	
		CELL7_OPEN	RLR	7	1	0x0	B	
		CELL6_OPEN	RLR	6	1	0x0	B	
		CELL5_OPEN	RLR	5	1	0x0	B	
		CELL4_OPEN	RLR	4	1	0x0	B	
		CELL3_OPEN	RLR	3	1	0x0	B	
		CELL2_OPEN	RLR	2	1	0x0	B	
		CELL1_OPEN	RLR	1	1	0x0	B	
		CELL0_OPEN	RLR	0	1	0x0	B	
VCELL_UV	**0x43**							
		Noreg17	RO	17	1	0x0	X	
		VBATT_WRN_UV	RLR	16	1	0x0	B	0 → VBAT UV comparator not triggered 1 → VBAT UV comparator triggered
		VBATTCRIT_UV	RLR	15	1	0x0	B	0 → VBAT critical UV not detected 1 → VBAT critical UV detected
		VSUM_UV	RLR	14	1	0x0	B	0 → Sum of cells UV not detected 1 → Sum of cells UV detected
		VCELL14_UV	RLR	13	1	0x0	B	0 → Cell UV not detected 1 → Cell UV detected
		VCELL13_UV	RLR	12	1	0x0	B	
		VCELL12_UV	RLR	11	1	0x0	B	
		VCELL11_UV	RLR	10	1	0x0	B	
		VCELL10_UV	RLR	9	1	0x0	B	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		VCELL9_UV	RLR	8	1	0x0	B	0 → Cell UV not detected 1 → Cell UV detected
		VCELL8_UV	RLR	7	1	0x0	B	
		VCELL7_UV	RLR	6	1	0x0	B	
		VCELL6_UV	RLR	5	1	0x0	B	
		VCELL5_UV	RLR	4	1	0x0	B	
		VCELL4_UV	RLR	3	1	0x0	B	
		VCELL3_UV	RLR	2	1	0x0	B	
		VCELL2_UV	RLR	1	1	0x0	B	
		VCELL1_UV	RLR	0	1	0x0	B	
VCELL_OV	**0x44**							
		Noreg17	RO	17	1	0x0	X	
		VBATT_WRN_OV	RLR	16	1	0x0	B	0 → VBAT OV comparator not triggered 1 → VBAT OV comparator triggered
		VBATTCRIT_OV	RLR	15	1	0x0	B	0 → VBAT critical OV not detected 1 → VBAT critical OV detected
		VSUM_OV	RLR	14	1	0x0	B	0 → Sum of cells OV not detected 1 → Sum of cells OV detected
		VCELL14_OV	RLR	13	1	0x0	B	0 → Cell OV not detected 1 → Cell OV detected
		VCELL13_OV	RLR	12	1	0x0	B	
		VCELL12_OV	RLR	11	1	0x0	B	
		VCELL11_OV	RLR	10	1	0x0	B	
		VCELL10_OV	RLR	9	1	0x0	B	
		VCELL9_OV	RLR	8	1	0x0	B	
		VCELL8_OV	RLR	7	1	0x0	B	
		VCELL7_OV	RLR	6	1	0x0	B	
		VCELL6_OV	RLR	5	1	0x0	B	
		VCELL5_OV	RLR	4	1	0x0	B	
		VCELL4_OV	RLR	3	1	0x0	B	
		VCELL3_OV	RLR	2	1	0x0	B	
		VCELL2_OV	RLR	1	1	0x0	B	
		VCELL1_OV	RLR	0	1	0x0	B	
VGPIO_OT_UT	**0x45**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		GPIO9_OT	RLR	13	1	0x0	B	0 → GPIO OT not detected 1 → GPIO OT detected
		GPIO8_OT	RLR	12	1	0x0	B	
		GPIO7_OT	RLR	11	1	0x0	B	
		GPIO6_OT	RLR	10	1	0x0	B	
		GPIO5_OT	RLR	9	1	0x0	B	
		GPIO4_OT	RLR	8	1	0x0	B	
		GPIO3_OT	RLR	7	1	0x0	B	
		GPIO9_UT	RLR	6	1	0x0	B	0 → GPIO UT not detected 1 → GPIO UT detected
		GPIO8_UT	RLR	5	1	0x0	B	
		GPIO7_UT	RLR	4	1	0x0	B	
		GPIO6_UT	RLR	3	1	0x0	B	
		GPIO5_UT	RLR	2	1	0x0	B	
		GPIO4_UT	RLR	1	1	0x0	B	
		GPIO3_UT	RLR	0	1	0x0	B	
VCELL_BAL_UV	**0x46**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	
		VCELL14_BAL_UV	RLR	13	1	0x0	B	0 → Cell balancing UV not detected 1 → Cell balancing UV detected
		VCELL13_BAL_UV	RLR	12	1	0x0	B	
		VCELL12_BAL_UV	RLR	11	1	0x0	B	
		VCELL11_BAL_UV	RLR	10	1	0x0	B	
		VCELL10_BAL_UV	RLR	9	1	0x0	B	
		VCELL9_BAL_UV	RLR	8	1	0x0	B	
		VCELL8_BAL_UV	RLR	7	1	0x0	B	
		VCELL7_BAL_UV	RLR	6	1	0x0	B	
		VCELL6_BAL_UV	RLR	5	1	0x0	B	
		VCELL5_BAL_UV	RLR	4	1	0x0	B	
		VCELL4_BAL_UV	RLR	3	1	0x0	B	
		VCELL3_BAL_UV	RLR	2	1	0x0	B	
		VCELL2_BAL_UV	RLR	1	1	0x0	B	
		VCELL1_BAL_UV	RLR	0	1	0x0	B	
GPIO_fastchg_OT	**0x47**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		Noreg14	RO	14	1	0x0	X	
		GPIO9_OPEN	RLR	13	1	0x0	B	0 → GPIO open not detected 1 → GPIO open detected
		GPIO8_OPEN	RLR	12	1	0x0	B	
		GPIO7_OPEN	RLR	11	1	0x0	B	
		GPIO6_OPEN	RLR	10	1	0x0	B	
		GPIO5_OPEN	RLR	9	1	0x0	B	
		GPIO4_OPEN	RLR	8	1	0x0	B	
		GPIO3_OPEN	RLR	7	1	0x0	B	
		GPIO9_fastchg_OT	RLR	6	1	0x0	B	0 → GPIO fast charge OT not detected 1 → GPIO fast charge OT detected
		GPIO8_fastchg_OT	RLR	5	1	0x0	B	
		GPIO7_fastchg_OT	RLR	4	1	0x0	B	
		GPIO6_fastchg_OT	RLR	3	1	0x0	B	
		GPIO5_fastchg_OT	RLR	2	1	0x0	B	
		GPIO4_fastchg_OT	RLR	1	1	0x0	B	
		GPIO3_fastchg_OT	RLR	0	1	0x0	B	
MUX_BIST_FAIL	**0x48**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		HWSC_DONE	RLR	14	1	0x0	B	0 → HWSC not executed 1 → HWSC terminated
		MUX_BIST_FAIL	RLR	0	14	0x0	B	0 → No failure detected on Cx conversion path 1 → Failure detected on Cx conversion path
BIST_COMP	**0x49**							
		VBAT_COMP_BIST_FAIL	RLR	17	1	0x0	B	0 → VBAT comparator BIST not failed 1 → VBAT comparator BIST failed
		VREG_COMP_BIST_FAIL	RLR	16	1	0x0	B	0 → VREG comparator BIST not failed 1 → VREG comparator BIST failed
		VCOM_COMP_BIST_FAIL	RLR	15	1	0x0	B	0 → VCOM comparator BIST not failed 1 → VCOM comparator BIST failed
		VTREF_COMP_BIST_FAIL	RLR	14	1	0x0	B	0 → VTREF comparator BIST not failed 1 → VTREF comparator BIST failed
		BIST_BAL_COMP_HS_FAIL	RLR	7	7	0x0	B	0 → Balancing comparator BIST not failed on even cells

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
								1 → Balancing comparator BIST failed on even cells
		BIST_BAL_COMP_LS_FAIL	RLR	0	7	0x0	B	0 → Balancing comparator BIST not failed on odd cells 1 → Balancing comparator BIST failed on odd cells
OPEN_BIST_FAIL	**0x4A**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	
		OPEN_BIST_FAIL	RLR	0	14	0x0	B	0 → No failure detected on Sx/Bx_x-1 conversion path 1 → Failure detected on Sx/Bx_x-1 conversion path
GPIO_BIST_FAIL	**0x4B**							
		GPO9short	RLR	17	1	0x0	B	
		GPO8short	RLR	16	1	0x0	B	
		GPO7short	RLR	15	1	0x0	B	
		GPO6short	RLR	14	1	0x0	B	
		GPO5short	RLR	13	1	0x0	B	
		GPO4short	RLR	12	1	0x0	B	
		GPO3short	RLR	11	1	0x0	B	
		Noreg10	RO	10	1	0x0	X	
		Noreg9	RO	9	1	0x0	X	
		Noreg8	RLR	8	1	0x0	B	
		VTREF_BIST_FAIL	RLR	7	1	0x0	B	0 → VCOM comparator BIST not failed 1 → VCOM comparator BIST failed
		GPIO_BIST_FAIL	RLR	0	7	0x0	B	0 → No failure detected on GPIO conversion path 1 → Failure detected on GPIO conversion path
VTREF	**0x4C**							
		Noreg17	RO	17	1	0x0	X	
		d_rdy_vtref	RLR	16	1	0x0	B	0 → Data was already read once 1 → Fresh new data
		VTREF_MEAS	RO	0	16	0x0	B	VTREF conversion data
NVM_WR_1	**0x4D**							
		Noreg17	RO	17	1	0x0	X	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		Noreg16	RO	16	1	0x0	X	
		NVM_WR_15_0	RW	0	16	0x0	B	Write buffer for NVM sector 0_15
NVM_WR_2	**0x4E**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_WR_31_16	RW	0	16	0x0	B	Write buffer for NVM sector 16_31
NVM_WR_3	**0x4F**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_WR_47_32	RW	0	16	0x0	B	Write buffer for NVM sector 32_47
NVM_WR_4	**0x50**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_WR_63_48	RW	0	16	0x0	B	Write buffer for NVM sector 48_63
NVM_WR_5	**0x51**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_WR_79_64	RW	0	16	0x0	B	Write buffer for NVM sector 64_79
NVM_WR_6	**0x52**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_WR_95_80	RW	0	16	0x0	B	Write buffer for NVM sector 80_95
NVM_WR_7	**0x53**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_WR_111_96	RW	0	16	0x0	B	Write buffer for NVM sector 96_111
NVM_RD_1	**0x54**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_RD_15_0	RO	0	16	0x0	B	Read buffer for NVM sector 0_15
NVM_RD_2	**0x55**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_RD_31_16	RO	0	16	0x0	B	Read buffer for NVM sector 16_31
NVM_RD_3	**0x56**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	

Register Name	Address	Field name	Type	Bit offset	Bit width	Reset value	Reset sources	Description
		NVM_RD_47_32	RO	0	16	0x0	B	Read buffer for NVM sector 32_47
NVM_RD_4	**0x57**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_RD_63_48	RO	0	16	0x0	B	Read buffer for NVM sector 48_63
NVM_RD_5	**0x58**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_RD_79_64	RO	0	16	0x0	B	Read buffer for NVM sector 64_79
NVM_RD_6	**0x59**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_RD_95_80	RO	0	16	0x0	B	Read buffer for NVM sector 80_95
NVM_RD_7	**0x5A**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		NVM_RD_111_96	RO	0	16	0x0	B	Read buffer for NVM sector 96_111
NVM_CMD_CNTR	**0x5B**							
		Noreg17	RO	17	1	0x0	X	
		Noreg16	RO	16	1	0x0	X	
		Noreg15	RO	15	1	0x0	X	
		Noreg14	RO	14	1	0x0	X	
		Noreg13	RO	13	1	0x0	X	
		Noreg12	RO	12	1	0x0	X	
		NVM_WR_BUSY	RO	11	1	0x0	B	0 → NVM controller not busy 1 → NVM controller busy
		NVM_OPER	RW	9	2	0x0	B	00/01 → No Action 10 → Erase 11 → Write
		NVM_PROGRAM	RW	8	1	0x0	B	0 → NVM controller not armed to execute operation defined by NVM_OPER 1 → NVM controller armed to execute operation defined by NVM_OPER
		NVM_CNTR	RO	0	8	0x0	B	Counts the number of write cycles executed See Table 52
NVM_UNLCK_PRG	**0x5C**							
		NVM_UNLOCK_START	WO	0	18	0x0	B	

6 Application information

6.1 Layout recommendations

6.1.1 PCB stackup

In order to achieve the best performances in terms of accuracy and EMC, an optimal PCB layer partitioning must be chosen. ST recommends the following stackup on a 4-layer board:

- **Top layer**: analog sense lines (refer to Section 6.1.3 Cell balancing (Force) and cell sensing (Sense) lines)
  - Battery supply and sense line (pin VBAT)
  - Cell voltage sense (pins Cx)
  - Current sense (pins ISENSEx)
  - NTC sense (pins GPIOx)
  - GNDREF
- **2nd layer**: ground planes (refer to Section 6.1.2 Ground connections for further details)
  - AGND under sense lines
  - DGND under communication and digital lines
  - GND_ESD/PACK_GND under the ESD caps in the battery connector region
- **3rd layer**: analog force lines (refer to Section 6.1.3 Cell balancing (Force) and cell sensing (Sense) lines)
  - Balancing lines (pins Sx and Bx_x-1)
- **Bottom layer**: analog COM lines and Digital lines
  - Isolated COM line (pins ISOHx/ISOLx)
  - Digital lines (pins GPIOx)
  - Regulators (pins VREG, VCOM, VTREF, VANA)

6.1.2 Ground connections

In order to achieve the best performances in terms of accuracy and EMC, care must be taken while designing ground connections.

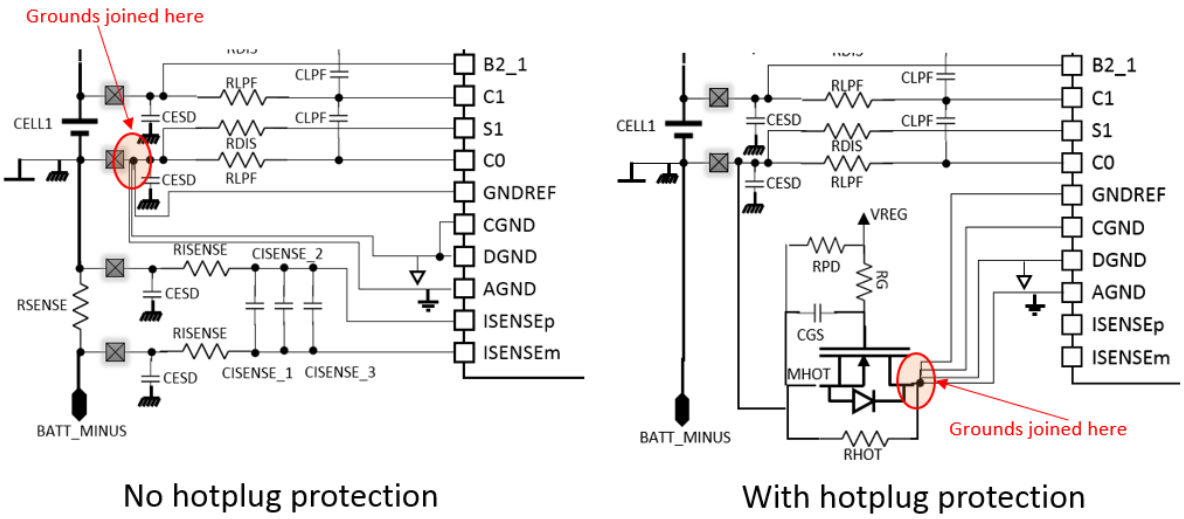
L9963E features 4 ground pins used as internal reference:

- **AGND**: ⏚ is the reference plane for the L9963E internal analog circuitry and must be kept as “clean” as possible in order not to catch noise from the nearby switching components. It can be used as 2nd layer of the PCB to shield voltage sense lines routed on the 1st layer.
- **DGND**: ▽ is the reference plane for the L9963E internal digital circuitry and it introduces noise on the PCB due to the logic switching activity. It must be separated from AGND plane and can be routed over the 2nd PCB layer.
- **CGND**: is the reference line for the L9963E internal communication circuitry. It is connected to the output buffer of SDO line and it acts as a reference for the ISOHx and ISOLx signals. It can be joined with DGND plane at device pin level.
- **GNDREF**: is the reference line for the L9963E internal ADCs. It carries low current and must be connected to the negative terminal of the battery pack, over the 1st layer, shielded by AGND as it was a cell voltage sense line. This will guarantee a clean and precise reference for all the internal ADCs.

L9963E performances are guaranteed if ground shift between AGND/DGND/CGND/GNDREF is kept below 100 mV. Hence, all the planes/lines mentioned above must be joined on the same node. This node is normally represented by the PCB connector to the battery pack ground, corresponding to the negative terminal of the first cell (PACK_GND ⊥).

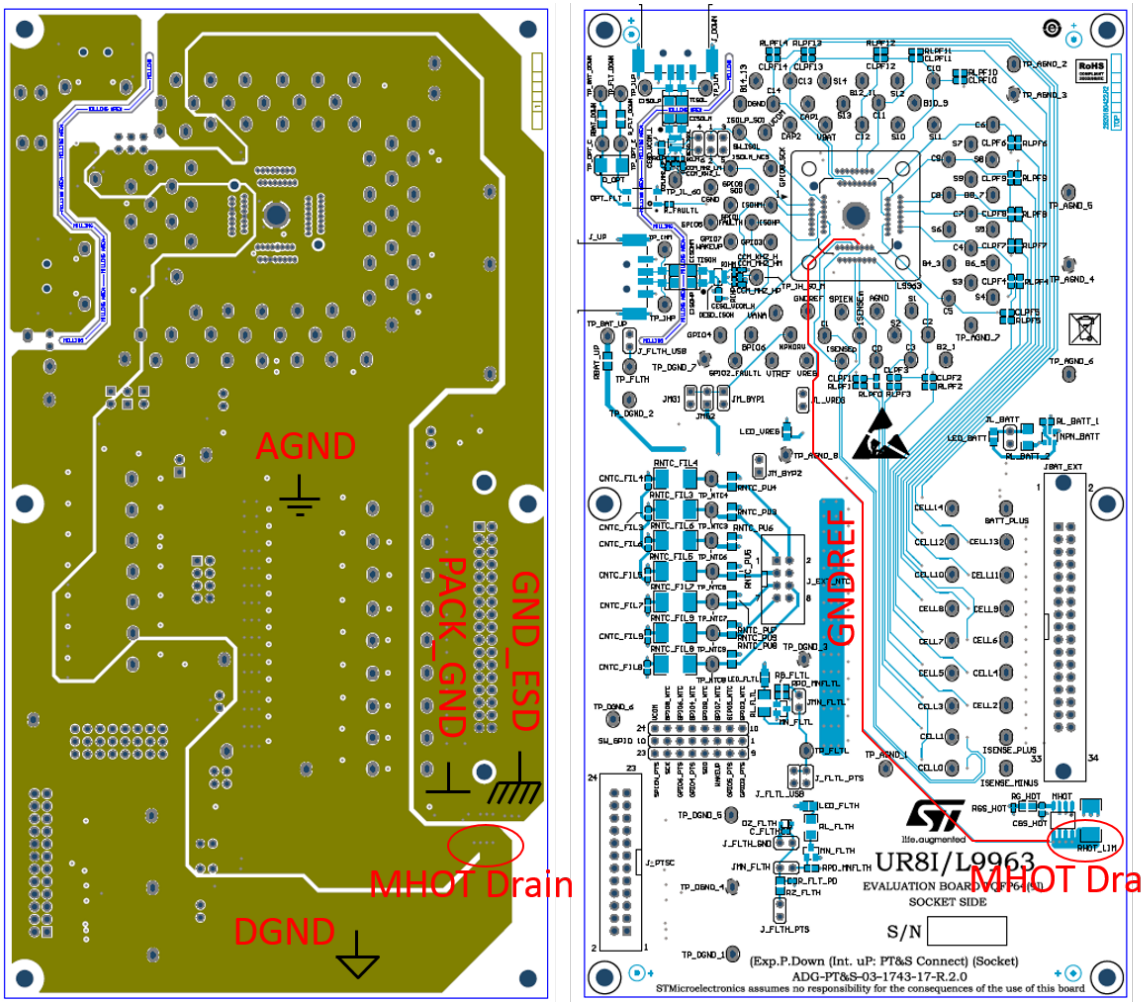
In case the **Hotplug** circuitry is mounted, the grounds collection node becomes the drain terminal of the MOSFET MHOT (refer to Figure 27).

Figure 27. **Grounds collection node**



ESD strikes at system level can damage both L9963E and analog front end components. In order to provide an effective protection, charge released upon strike must be properly deviated towards the GND_ESD ⏚. This is achieved by proper grounding of the ESD capacitors to such a dedicated ground plane, which is then joined with the other grounds at the PCB connector to PACK_GND, regardless of the hotplug protection implementation. In fact, the ESD strike must bypass MHOT in order not to damage it.

Figure 28. **Layout example of ground connections**

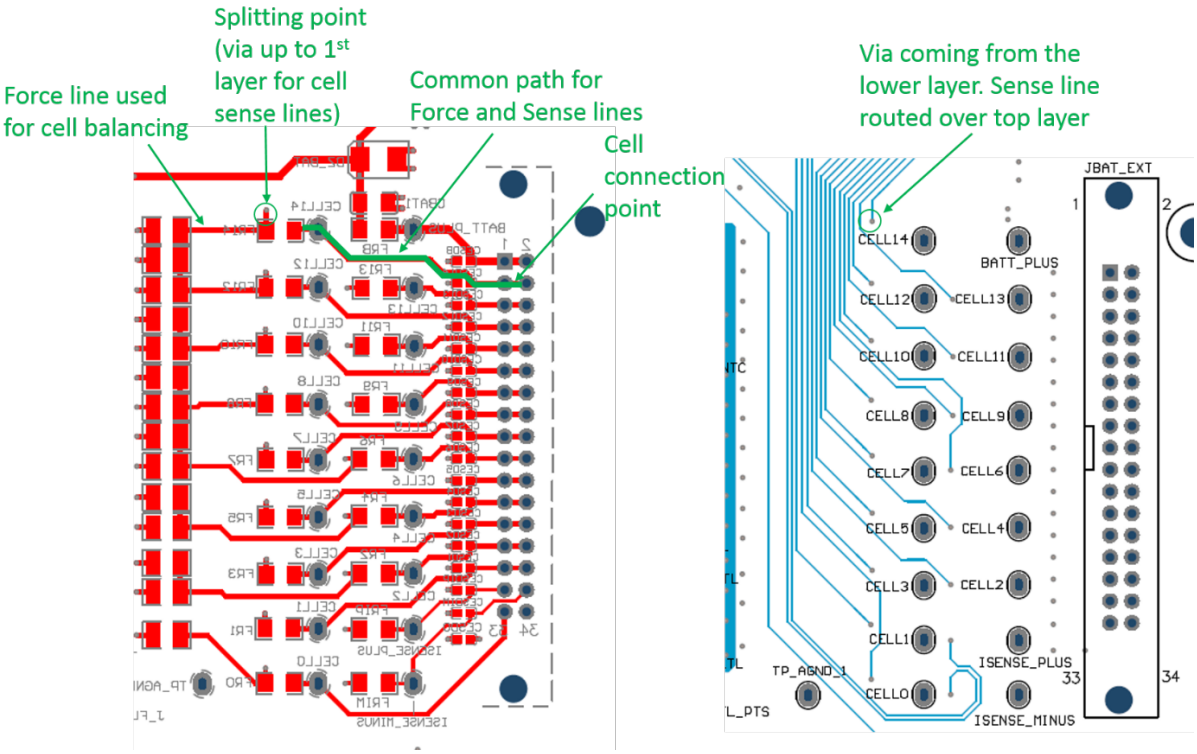


6.1.3 Cell balancing (Force) and cell sensing (Sense) lines

To increase cell voltage measurement accuracy during balancing, the voltage drop over the PCB lanes connected to the cells has to be minimized. In order to do so, voltage sense lines connected to L9963E Cx pins and cell balancing lines connected to Sx/Bx_x-1 pins must be split as close as possible to the PCB connector.

As recommended in **PCB Stackup**, cell sense lines must be routed over the top layer, shielded by AGND, while balancing lines can be routed over the 3rd layer. Splitting must be done after the ESD caps and ferrite beads, in order to guarantee protection from strikes and EMI robustness. Figure 29 shows a layout example.

Figure 29. Example of best practice for splitting cell force and sense lines



6.1.4 Regulator capacitors

L9963E features only linear regulators, in order not to introduce any switching noise on the PCB. Nevertheless, regulator capacitors must be placed as close as possible to the corresponding device pin in order to avoid loops generated by long traces and filter any ripple caused by current absorption peaks.

Mounting capacitors on the bottom side of the PCB, close to the L9963E footprint is a good option.

6.1.5 ESD clamps for communication interfaces

Routing of the PCB traces connected to the ESD clamp of the vertical interface is critical in order to ensure maximum reduction of the spikes.

Even if the ISOHx and ISOLx pins are connected to the ECU global pins through a transformer, this component does not guarantee total protection against very fast spikes due to ESD strikes and/or sudden external shorts to battery/ground. In fact, the transformer parasitic capacitance between primary and secondary windings (in the order of magnitude of pF) is still able to couple very fast voltage transients from one side to the other.

In order to clamp such spikes, ST recommends using the D_ESD component in the **ISO Lines Circuit**. To achieve maximum clamping effectiveness, recommendations shown in Figure 30 and Figure 31 must be followed, in order to reduce parasitic effects due to the inductances of the PCB lanes.

Figure 30. **Recommended routing technique in order to reduce additional spikes due to lanes parasitic inductance**

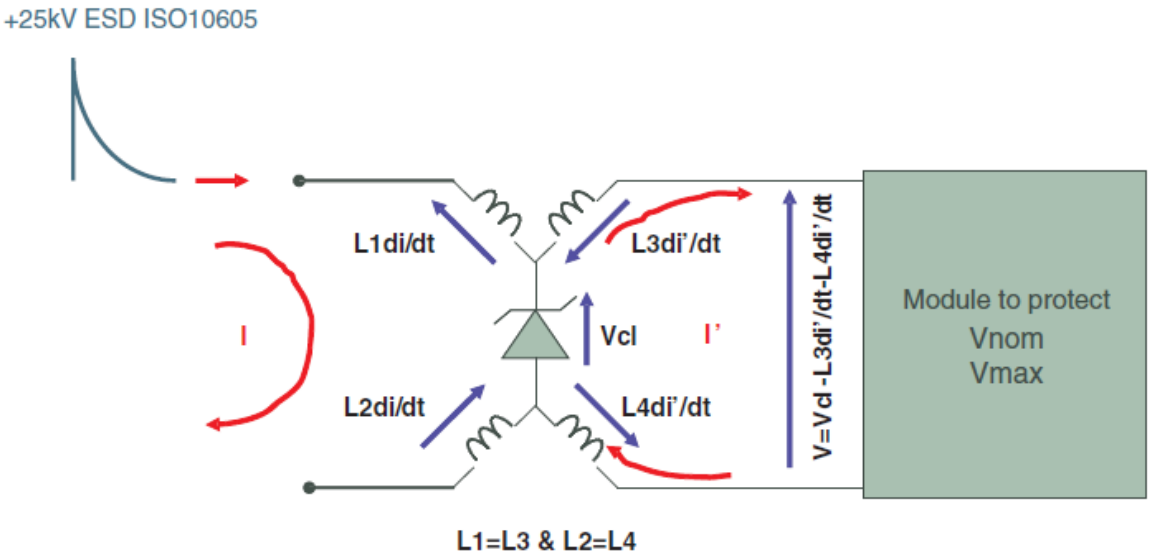
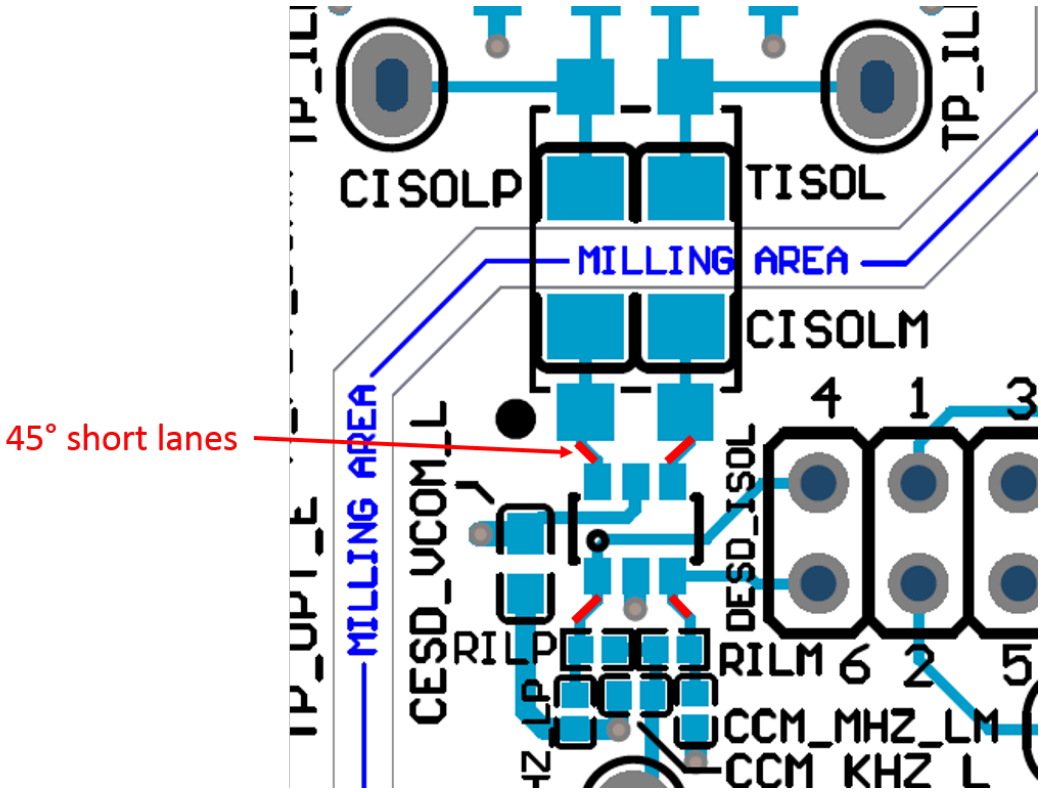


Figure 31. **Layout for ESD protections according to the recommended technique**



6.2 Typical application circuit and bill of material

Figure 32. Typical application circuit

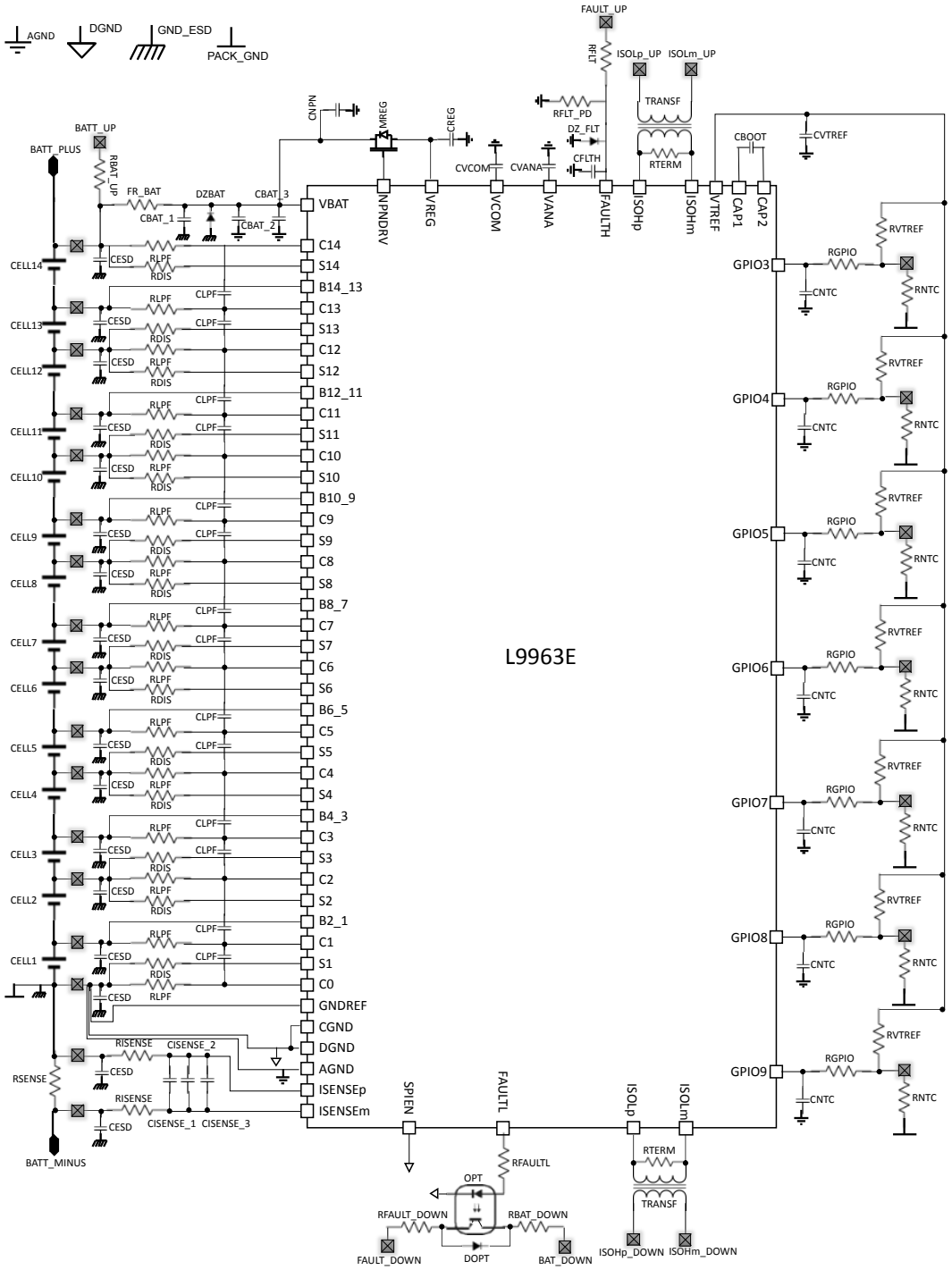


Table 73. Recommended components for typical application scenario

Components	Value	Unit	Max. tolerance	Rating	Comments
FRBAT	1	kΩ	@100 MHz	1.4 A @ 125 °C	Ferrite bead helps limiting the inrush current due to hotplug. It also filters high frequency noise. The BLM31KN102SH1L is recommended. It can be replaced with a 10 Ω RBAT resistor. Higher resistance values are not recommended since they introduce an error in VBAT measurement, proportional to R_{BAT}*I_{VBAT}.
DZBAT	68	V			The SMA6T68AY is recommended for protecting VBAT against damage during hotplug and ESD events. Connect to GND_ESD.
CBAT_3	100	pF	10%	100 V	Filter high frequency noise on VBAT sense line. Place as close as possible to VBAT pin. Connect to AGND.
CBAT_2	33	nF	10%	100 V	Filter high frequency noise on VBAT sense line. Place as close as possible to VBAT pin. Connect to AGND.
CBAT_1	2.2	µF	10%	100 V	Provide battery stabilization. Filter noise on VBAT sense line. Connect to GND_ESD. Do not exceed 2.2 µF.
CVCOM	220	nF	10%	16 V	Tank for the VCOM regulator. Mount as close as possible to VCOM pin. Total capacity on the VCOM pin must be equal to 2.2 µF. When isolated SPI communication is implemented via **Transformer-Based Insulation**, the recommended capacity partitioning is: • 1 µF as CESD_VCOM on the ISOH clamp. Connect to GND_ESD (refer to Section 6.8 ISO lines circuit) • 1 µF as CESD_VCOM on the ISOL clamp. Connect to GND_ESD (refer to Section 6.8 ISO lines circuit) • 220 nF as CVCOM directly on the VCOM pin. Connect to AGND
CVCOM	2.2	µF	10%	16 V	Tank for the VCOM regulator. Mount as close as possible to VCOM pin. This configuration is recommended when isolated SPI communication is implemented via **Capacitive-Based Insulation**.
CVANA	2.2	µF	10%	6.3 V	Tank for the VANA regulator. Connect to AGND.
CVTREF	2.2	µF	10%	16 V	Tank for the VTREF regulator. Connect to AGND.
CBOOT	1	µF	10%	16 V	Bootstrap capacitor.

6.3 Cell voltage sensing circuit

Figure 33 shows the recommended cell voltage sensing circuit.

Figure 33. Typical cell voltage sensing circuit

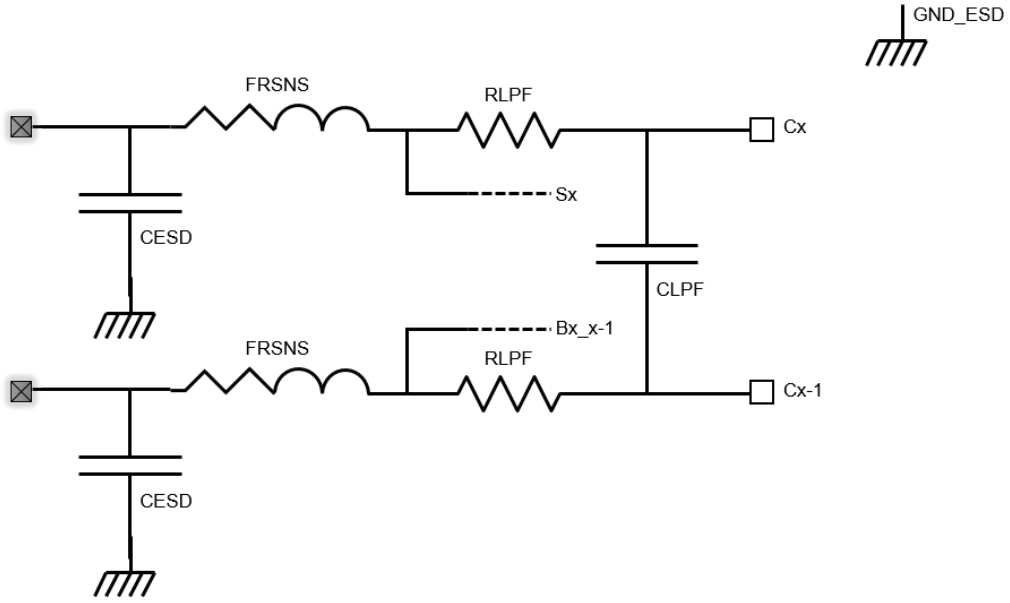
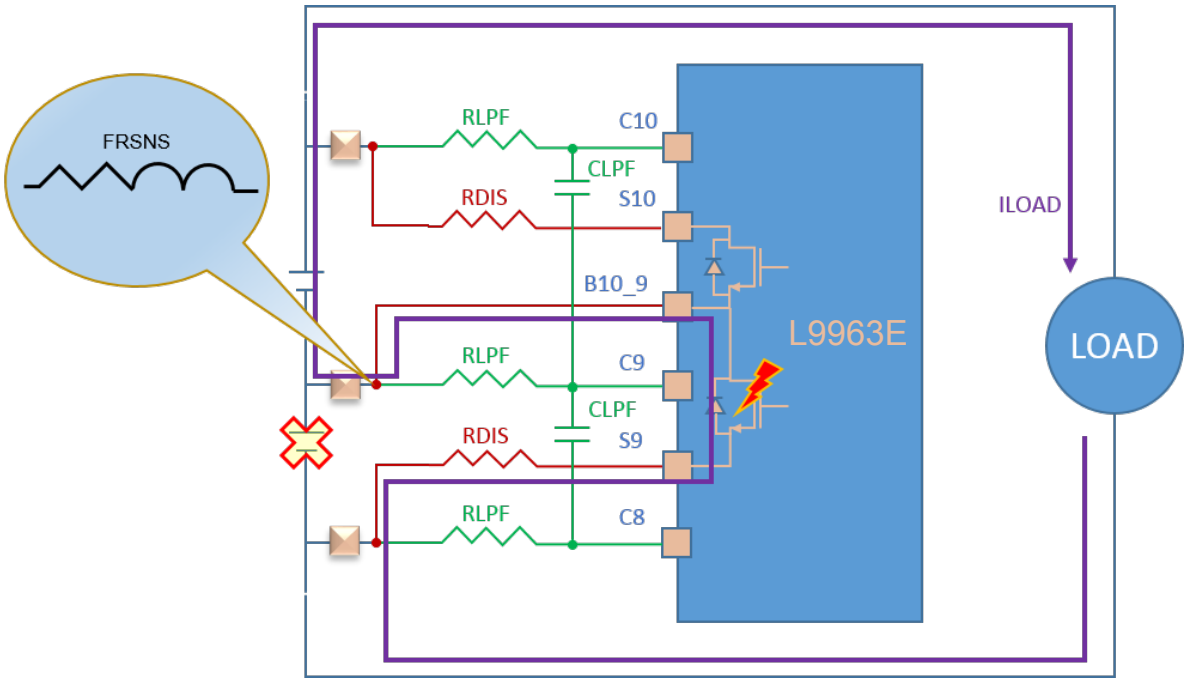


Table 74. Typical BOM for cell voltage sensing circuit

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{LPF}	100	Ω	10%	1/16 W	LPF resistor for cell voltage measurement. Do not exceed 3 kΩ, otherwise cell open failure could be detected. Higher values of resistance cause higher measurement offset error due to the leakage I_{CELL_LEAK} from Cx pins (see Table 39). A typical value of 100 Ω is recommended for pre-filtering the input signal in the analog domain and pass BCI trials. The differential filter cut-off frequency is $f_C = \frac{1}{4\pi R_{LPF} C_{LPF}}$ Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.
C_{LPF}	10	nF	10%	50 V	LPF capacitor for cell voltage measurement. The differential filter cut-off frequency is $f_C = \frac{1}{4\pi R_{LPF} C_{LPF}}$. The capacitors also allow better energy distribution during hotplug events. Do not modify this value, since it alters cell open diagnostic settling time.
C_{ESD}	47	nF	10%	100 V	Protect against ESD events and ISO spikes. Connect to GND_ESD.
FR_{SNS}	1	kΩ	@100 MHz	1 A @ 125 °C	Add robustness against BCI. Guarantees fail safe in case of open on busbar (refer to Figure 34 as an example). MPZ2012S102ATD25 is recommended.

Figure 34. **Fail Safe in case of open on busbar**



6.4 Current sense circuit

Figure 35 shows the recommended cell voltage sensing circuit.

Figure 35. **Typical current sensing analog front end**

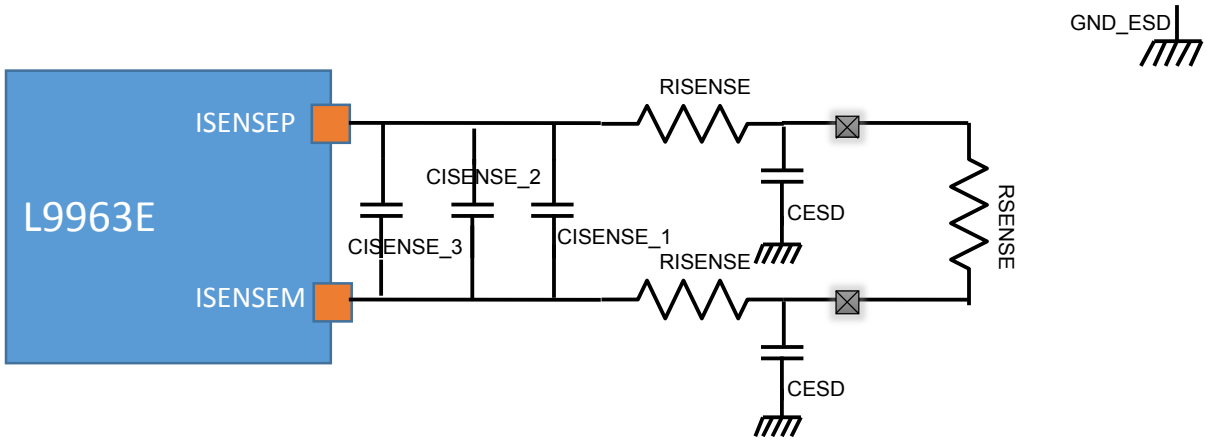


Table 75. **Current sense BOM**

Components	Value	Unit	Max. tolerance	Rating	Comments
C_{ESD}	47	nF	10%	100 V	Protect against ESD events and ISO spikes. Connect to GND_ESD

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{SENSE}	100	µΩ			Shunt resistor used for current sensing and coulomb counting. Rating depends on the maximum battery current (R_{SENSE} * $I_{SENSE\_MAX}^2$). Different RSENSE values are possible as long as R_{SENSE} * I_{SENSE} stays in the differential measurement range [-150 ; +150] mV and the ISENSEp/ISENSEm AMR are not violated
C_{ISENSE_1}	10	µF	10%	10 V	Filter low frequency noise on the ISENSEp/ISENSEm input.
C_{ISENSE_2}	68	nF	10%	10 V	Filter high frequency noise on the ISENSEp/ISENSEm input.
C_{ISENSE_3}	33	pF	10%	10 V	Filter high frequency noise on the ISENSEp/ISENSEm input. Place as close as possible to ISENSEp/ISENSEm pins.
R_{ISENSE}	100	Ω	1%	1 W	Filter noise on the ISENSEp/ISENSEm input and pass BCI tests. Exceeding 100 Ω causes a higher measurement error. Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.

6.5 VREG regulator circuit

VREG is the main device regulator, handling most of the current consumed by L9963E in Normal mode.

Figure 36. VREG regulator circuits

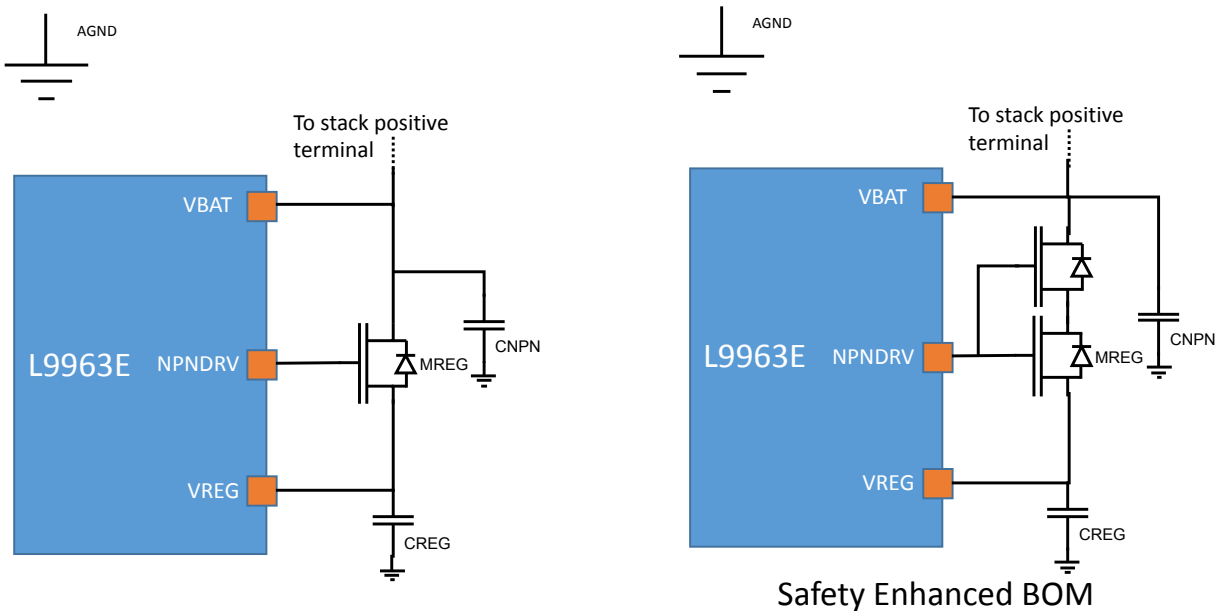


Table 76. VREG regulator BOM

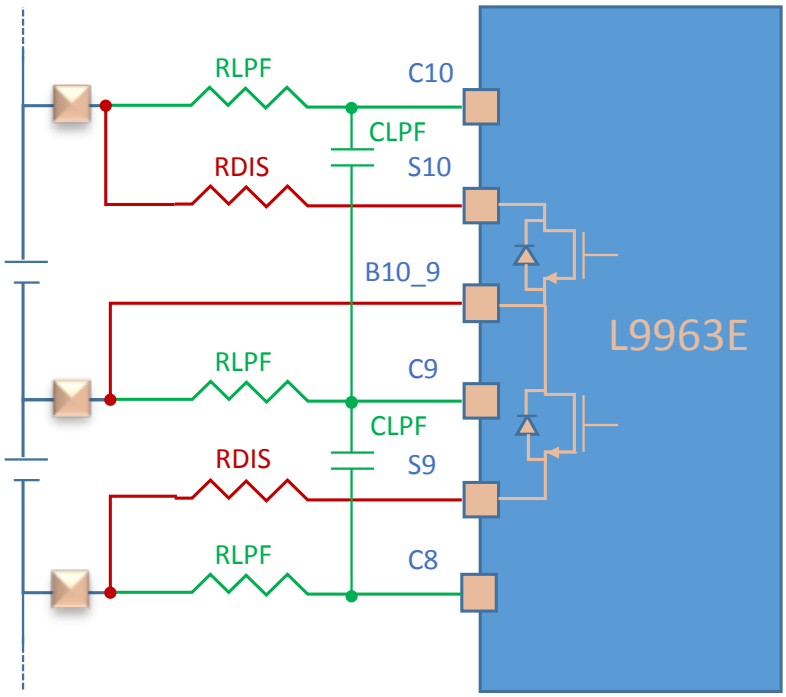
Components	Value	Unit	Max. tolerance	Rating	Comments
C_{NPN}	100	nF	20%	100 V	Provide battery stabilization for regulator. Filter noise coming from battery pack. Place close to MOS drain. Connect to AGND

Components	Value	Unit	Max. tolerance	Rating	Comments
M_{REG}	3	V	V_{GS_TH} max	V_{DS} ≥ 80V	The STL8N10LF3 (single FET) is recommended for applications requiring optimized thermal performances The STL8DN10LF3 (dual FET) is recommended for applications requiring also a higher safety integrity level. Alternatively, the STD25NF10LA is also supported. For all components, follow MOSFET datasheet in order to optimize Rth value.
C_{REG}	4.7	µF	10%	16 V	Tank for the VREG regulator. Mount as close as possible to VREG pin. Connect to AGND

6.6 Cell balancing circuits

6.6.1 Cell balancing with internal MOSFETs

Figure 37. Cell monitoring with internal balancing



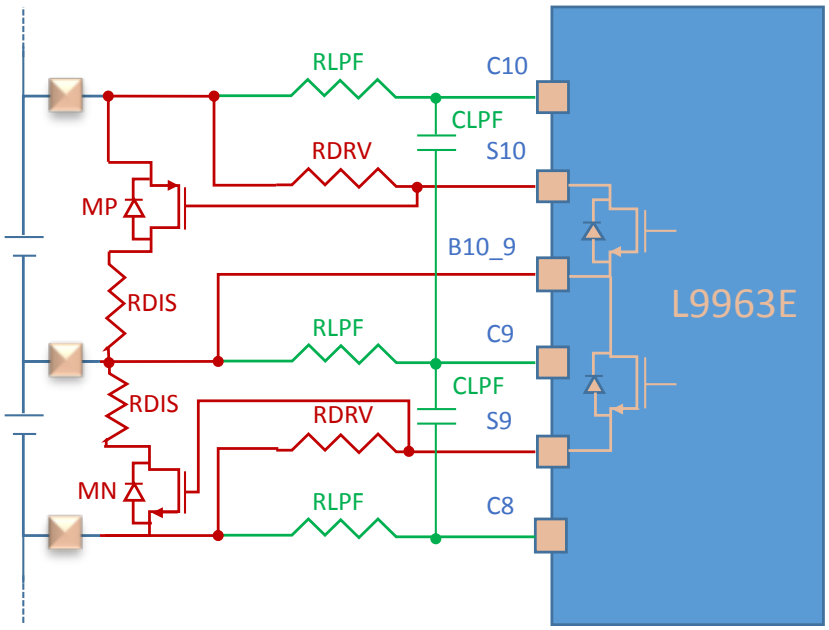
- Force lines used for balancing. Connect them as close as possible to the cell connector. This improves cell voltage sensing while balancing is ongoing, by minimizing the voltage drop on the sense lines while current is being sunk
- Sense lines used for cell voltage measurement. Keep away from noisy lines. Recommended PCB layout strategy is to route them over the first layer and shield them using the second layer as GND plane

Table 77. Internal balancing components with recommended values

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{DIS}	39	Ω	10%	3/4 W	Any value is possible, as long as the cell balance current does not exceed the required current limitation (200 mA). Maximum cell balance current in application is $I_{BALmax} = \frac{V_{CELLmax}}{R_{DIS}}$ Mounting less than 39 Ω may seriously jeopardize hotplug capability of the internal balancing FETs. Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.

6.6.2 Cell balancing with external MOSFETs

Figure 38. Cell monitoring with external balancing with the mixed NMOS and PMOS transistors



- Force lines used for balancing. Connect them as close as possible to the cell connector. This improves cell voltage sensing while balancing is ongoing, by minimizing the voltage drop on the sense lines while current is being sunk
- Sense lines used for cell voltage measurement. Keep away from noisy lines. Recommended PCB layout strategy is to route them over the first layer and shield them using the second layer as GND plane

Table 78. External balancing components with recommended values

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{DRV}	2	kΩ	10%	1/10 W	The drop on R_{DRV} generates the VGS = V_{CELL} to turn on the external balance FET. Max 3.3 kΩ. Values lower than the recommended one can be used when both internal and external paths have to be exploited for balancing. However, current in the internal balancing path must not exceed 200 mA. Maximum internal cell balance current in application is $I_{BALmax} = \frac{V_{CELLmax}}{R_{DRV}}$
R_{DIS}	10	Ω	10%	3 W	Any value is possible, as long as the cell balance current does not exceed the maximum drain current of the external FET. Maximum external cell balance current in application is $I_{BALmax} = \frac{V_{CELLmax}}{R_{DIS}}$
M_P					The BSS308PE is recommended for the balancing of even cells
M_N					The 2V7002K is recommended for the balancing of odd cells

6.7 FAULT line circuit

The **FAULT Line** implementation varies according to the system topology. In all cases, fault signal follows a monodirectional approach, propagating in the top-down direction. Transceivers are not included in the fault line and can be bypassed.

6.7.1 Distributed BMS

In a distributed BMS there are several independent cell monitoring units, each mounted on its own PCB. To ease harness routing and allow for signal regeneration through L9963E acting as a buffer, daisy chained approaches are preferred rather than bus configurations. Hence, in a fashion similar to **ISO Lines Circuit**, **FAULT Line** is also daisy chained, as shown in Figure 39.

For safety purposes, it is better to feed the daisy chained fault line through the VBAT line, rather than using VCOM regulator.

On one hand, using VCOM would result in a much simpler circuit, because FAULTH signal would be in the 5 V digital domain. On the other hand, this would imply routing a 5 V global wire in the harness, thus exposing it to all related transients. In the end, a failure affecting the VCOM global wire would cut off both **Isolated Serial Peripheral Interface** and **FAULT Line**.

Feeding the fault line with VBAT makes it totally independent from **Isolated Serial Peripheral Interface**, thus achieving better redundancy and a higher level of safety.

Figure 39. **FAULT link between daisy chained devices**

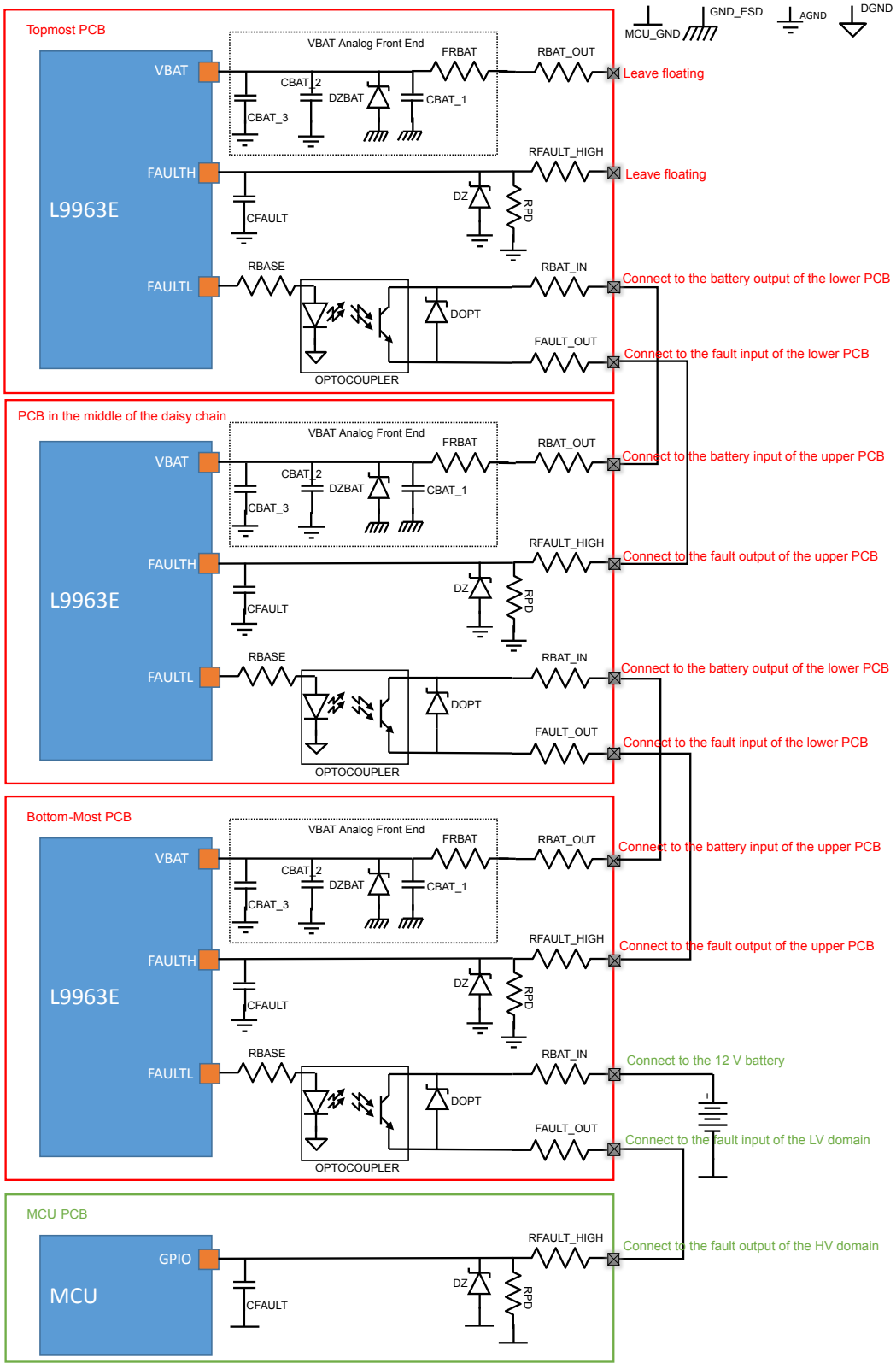


Table 79. **FAULT line BOM**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{BAT_OUT}	10	kΩ	10%	1/2 W	Protect against STG and provide polarization for FAULT signal propagation to the upper BMU Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.
R_{PD}	18	kΩ	10%	1/10 W	Pull-down resistor for FAULT input
D_Z	4.7	V			The SZMM3Z4V7T1G is recommended for clamping the voltage on the FAULT input
R_{FAULT_HIGH}	6.2	kΩ	10%	1/2 W	Filtering the FAULT signal and limiting the ESD inrush current. Protect the FAULTH input in case of external short to battery. Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.
C_{FAULT}	2.2	nF	10%	50 V	Filtering the FAULT signal and improving ESD protection and immunity to ISO spikes
R_{BASE}	2	kΩ	10%	1/16 W	Limit base current to the optoisolator
OPT	3.75	kVrms			The PS2703-1-F3-K-A is recommended for isolated propagation of the FAULT signal
R_{BAT_IN}	6.2	kΩ	10%	1/2 W	Protect against external shorts and provide polarization for FAULT signal propagation to the lower BMU Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.
R_{FAULT_OUT}	6.2	kΩ	10%	1/2 W	Protect against external shorts and provide polarization for FAULT signal propagation to the lower BMU Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.
D_{OPT}	82	V			Protect against sudden external shorts or ESD strikes. The SMA6T82AY is recommended.

6.7.2 Centralized BMS

In a centralized BMS, the **FAULT Line** can be easily implemented via a wired-OR approach. This allows a consistent simplification of the BOM.

The optocouplers can be all fed by the same supply as the MCU. Then, only a pull-down resistor and an RC filter are needed to interface the fault output bus to the GPIO used to read back the fault status.

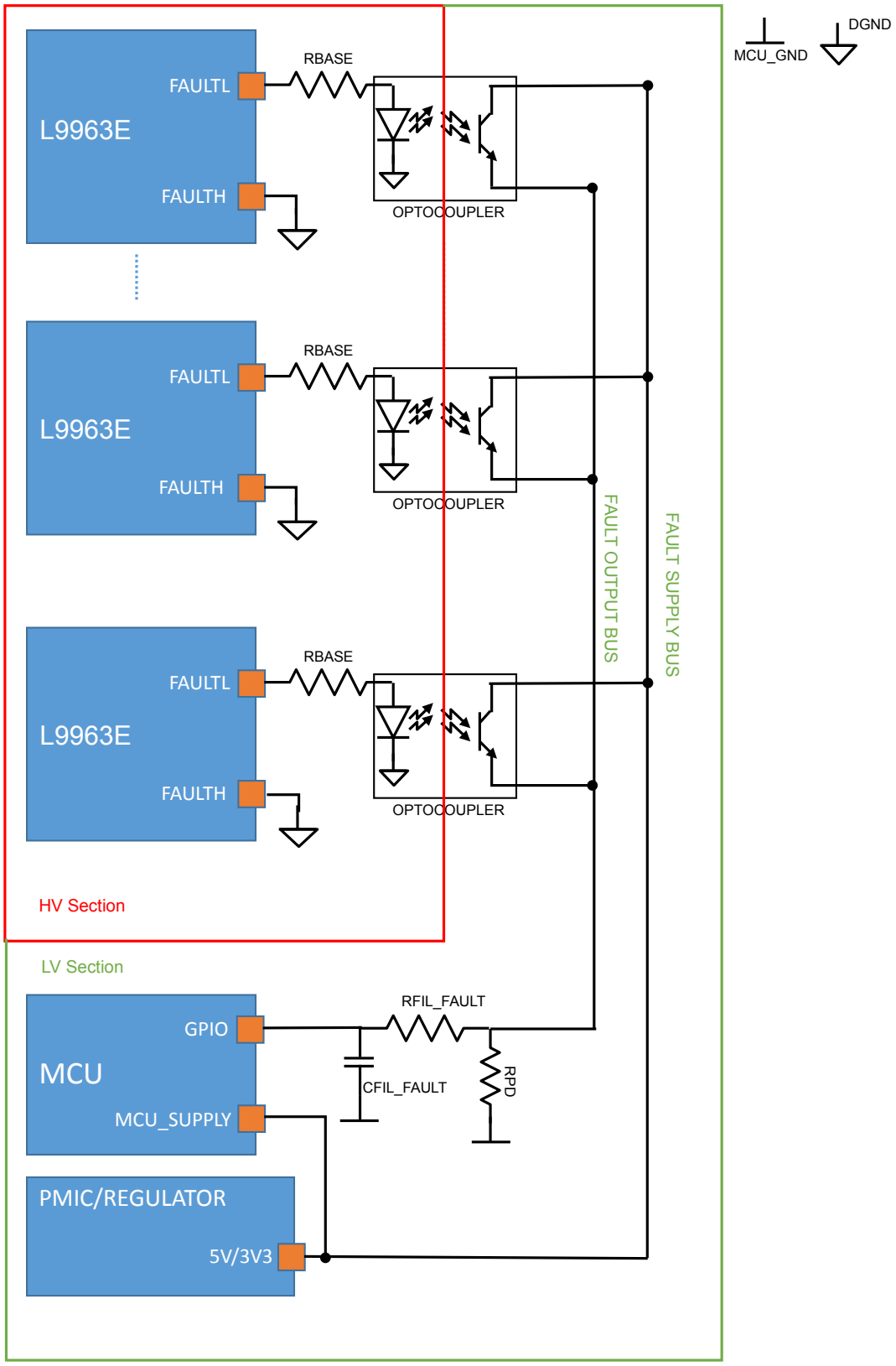
FAULTH input is not used and must be connected to DGND.

The recommended circuit is shown in Figure 40.

Table 80. Fault line BOM for a centralized BMS

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{PD}	10	kΩ	10%	1/16 W	Pull-down resistor for FAULT input
R_{FIL_FAULT}	1	kΩ	10%	1/16 W	Filtering the FAULT signal. Place this as close as possible to the MCU GPIO sensing the fault line.
C_{FIL_FAULT}	100	pF	10%	16 V	Filtering the FAULT signal. Place this as close as possible to the MCU GPIO sensing the fault line.
R_{BASE}	2	kΩ	10%	1/16 W	Limit base current to the optoisolator
OPT	3.75	kVrms			The PS2703-1-F3-K-A is recommended for isolated propagation of the FAULT signal

Figure 40. **Recommended FAULT line design in a centralized BMS**



6.8 ISO lines circuit

The following section illustrates the typical analog front end to communicate about the vertical insulated interface.

6.8.1 Transformer-based insulation

The transformer-based insulation is recommended for global communication lines between different modules in a distributed BMS. It offers better insulation and higher immunity to BCI, being the transformer an intrinsic common mode filter.

Figure 41. Transformer based ISO lines circuit

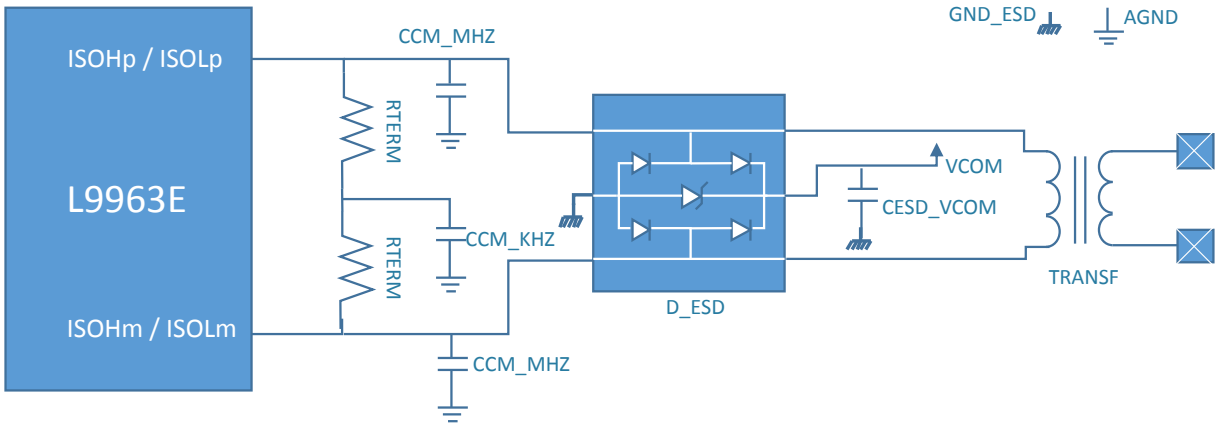


Table 81. Transformer-based ISO lines BOM

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{TERM}	60	Ω	10%	1/16 W	Termination resistance. Differential output signal amplitude can be calculated with the following equation: $V_{ISO_{DIFF}} = V_{COM}\frac{R_{TERM}}{R_{DIFF\_ISO\_OUT}}$
C_{CM_KHZ}	6.8	nF	10%	10 V	Filter common mode noise in the kHz range (inverter and other power converters). Pole introduced is $f_{cut\_khz} = \frac{1}{\pi C_{CM\_KHZ}\left(\frac{R_{ISO_{DIFF}}}{2} + R_{TERM} + 7.2k\Omega\right)}$. Do not exceed 10 nF, otherwise common mode settling time upon ISO port enable will last too long. Connect to AGND.
C_{CM_MHZ}	22	pF	10%	16 V	Filter common mode noise in the MHz range for improved BCI immunity. Pole introduced is $f_{cut\_mhz} = \frac{1}{2\pi C_{CM\_MHZ} R_{TERM}}$. Do not exceed 47 pF, otherwise differential output signal in high frequency mode might be strongly distorted. Connect to AGND.
C_{ESD_VCOM}	1	µF	10%	16 V	Deviate energy clamped by D_{ESD} directly to AGND, preventing any ESD strike from affecting other PCB components. Total capacity on the VCOM pin must be equal to 2.2 µF. Hence, in BMS configuration, the recommended capacity distribution is: 1 µF as C_{ESD_VCOM} on the ISOH clamp, 1 µF as C_{ESD_VCOM} on the ISOL clamp, 200 nF as C_{VCOM} directly on the VCOM pin (refer to Table 73). Connect to GND_ESD
D_{ESD}					It must be mounted only for **Distributed BMS** where isolated SPI pins are global pins or the ECU.

Components	Value	Unit	Max. tolerance	Rating	Comments
					The USBLC6-2SC6Y is the recommended ESD clamp device. It also protects the circuitry from spikes caused by a sudden short to battery on the global ISO lines. Care must be taken while routing the component on the PCB in order to minimize inductive spikes upon ESD strikes. Refer to the **AN2689 - Protection of automotive electronics from electrical hazards, guidelines for design and component selection**, section 5 – PCB layout recommendations.
TRANSF				3.75 kV	The ESMIT-4180/A is recommended for isolated communication interface

6.8.2 Capacitive-based insulation

The capacitive-based insulation is recommended for local communication lines between different L9963E in a centralized BMS. It helps reducing the bill of material, while still guaranteeing common mode filtering between stacked devices.

As shown in **Centralized BMS**, it is recommended to implement the isolation between HV and LV domains using a transformer, for better EMC performances.

Figure 42. Capacitive based ISO lines circuit

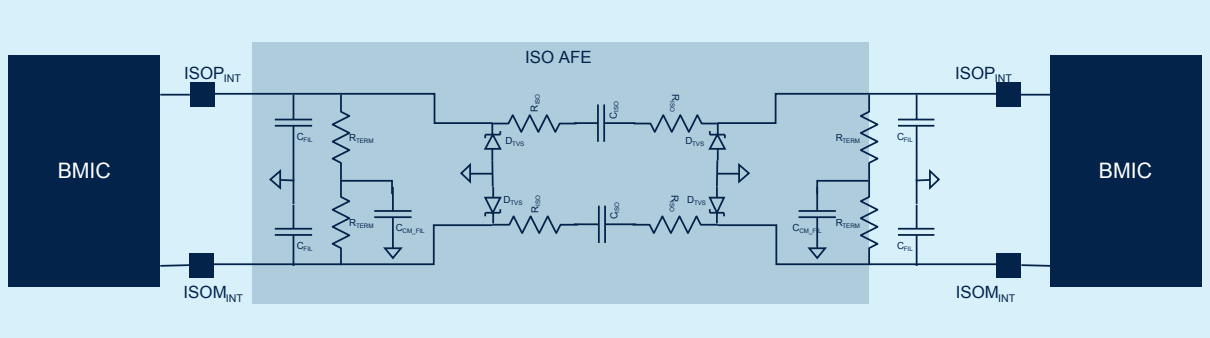


Table 82. Capacitive-based ISO lines BOM

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{TERM}	59	Ω	10%	1/16 W	Termination resistance. Differential output signal amplitude can be calculated with the following equation: $V_{ISO_{DIFF}} = V_{COM}\frac{R_{TERM}}{R_{DIFF\_ISO\_OUT}}$
C_{CM_FIL}	6.8	nF	10%	10 V	Filter common mode noise in the kHz range (inverter and other power converters). Pole introduced is $f_{cut\_khz} = \frac{1}{\pi C_{CM\_KHZ}\left(\frac{R_{ISO_{DIFF}}}{2} + R_{TERM} + 7.2k\Omega\right)}$. Do not exceed 10 nF, otherwise common mode settling time upon ISO port enable will last too long. Connect to AGND.
C_{ISO}	47	nF	10%	100 V	Filters the common mode, while letting the differential mode pass. It acts as a high-pass filter with a cutoff frequency of $f_{cut} = \frac{1}{2\pi\left[\left(\frac{R_{DIFF\_ISO\_OUT}}{2}\middle\|\middle\|R_{TERMO}\right) + R_{TERM}\right]C_{ISOP}}$
C_{FIL}	22	pF	10%	16 V	Noise filtering capacitor
D_{TVS}					SZESD8351P2T5G or PESD5V0V1. TVS for withstanding hotplug

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{ISO}	6.8	Ω	10%	1/10 W	Resistor for limiting inrush current during hotplug

6.9 NTC analog front end

6.9.1 Single ended measurement

In the single ended approach the external NTC is connected between PCB global input and battery pack GND. This strategy requires only a single PCB global pin for each external NTC. However, even if L9963E AGND is connected to pack GND at PCB level, measurement precision could be affected by shifts between the two grounds, which can be seen as a VTREF variation. In order to increase measurement precision, connection of the NTC to AGND through an additional PCB connector or **Differential Measurement** can be exploited.

Figure 43. Example of NTC single ended measurement

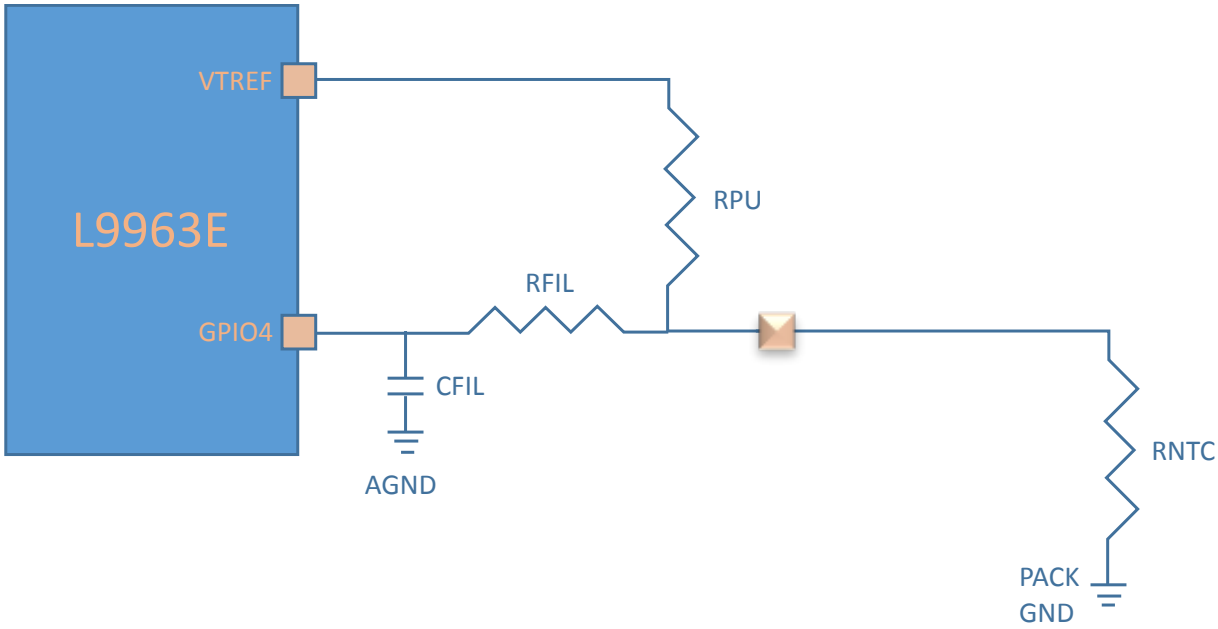


Table 83. NTC analog front end BOM for single ended measurement

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{NTC}	10	kΩ	1%		Recommended external NTC typical value. The NTCALUG02A103F is a good option for evaluation purposes
R_{FIL}	3.9	kΩ	10%	1.5 W	Protect the GPIO in case of external STG/STB. Limit the ESD inrush current. Filter the NTC signal: cut-off frequency is $f_C = \frac{1}{2\pi R_{FIL} C_{FIL}}$. Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.
C_{FIL}	100	nF	10%	100 V	Protect against ESD events and ISO spikes. Filter the NTC signal: cut-off frequency is $f_C = \frac{1}{2\pi R_{FIL} C_{FIL}}$. Connect to AGND
R_{PU}	10	kΩ	1%	0.5 W	Provide VTREF/2 polarization for NTC typical value. Protect VTREF pin in case of external short to battery/GND.

Components	Value	Unit	Max. tolerance	Rating	Comments
					Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.

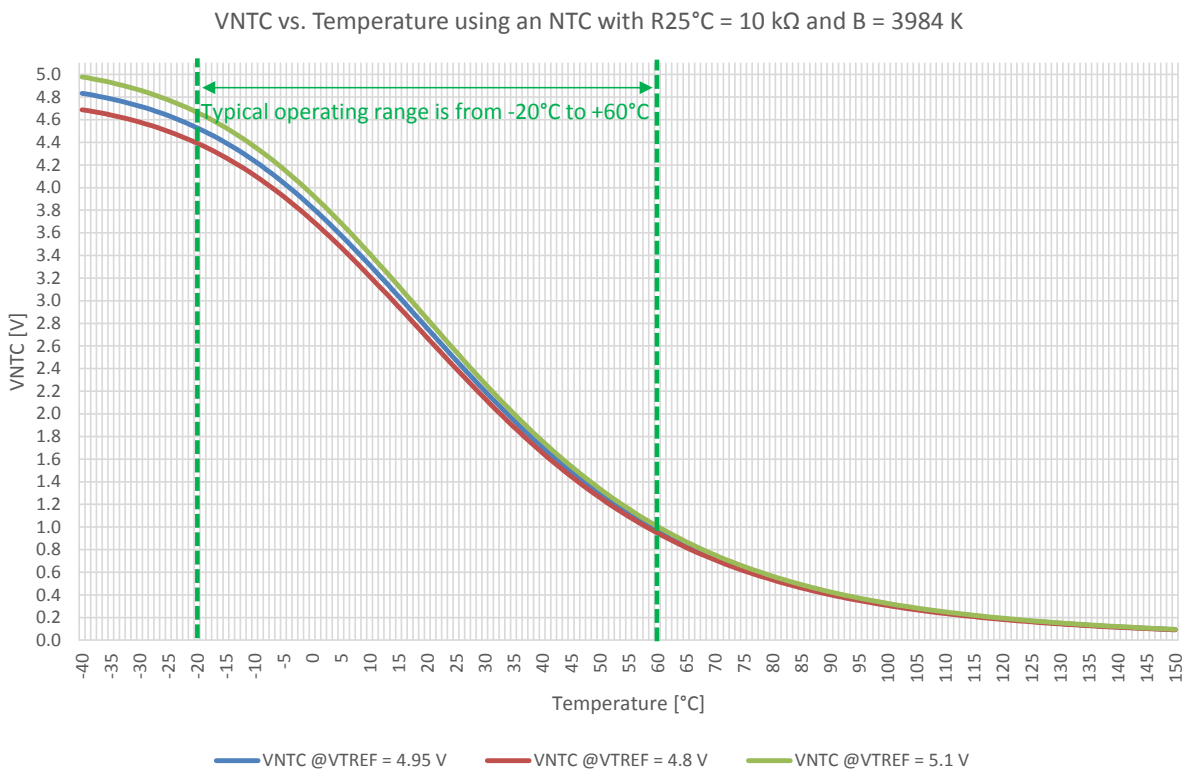
In this configuration, the NTC voltage varies according to the following equation:

NTC voltage variation with temperature (single ended measurement)

$$\begin{cases} V_{NTC}\left(T\right) = V_{TREF} \times \dfrac{R_{NTC}(T)}{R_{NTC}(T) + R_{PU}} \\ R_{NTC}(T) = R_{25°C} \times e^{B\left(\frac{1}{T(K)} - \frac{1}{298.15}\right)} \\ T(°C) = \dfrac{B}{\frac{B}{298.15} + \ln\left(\dfrac{\frac{R_{PU} \times V_{NTC}}{VTREF - V_{NTC}}}{R_{25°C}}\right)} - 273.15 \end{cases} \quad (18)$$

L9963E provides both VNTC and VTREF measurements via SPI registers, allowing MCU to calculate cell temperature as in the Eq. (18).

Figure 44. VNTC vs. temperature example (single ended measurement)



6.9.2 Differential measurement

In the single ended approach the external NTC is connected between two PCB global inputs. This eliminates the issue of GND shift but requires an additional global pin for each NTC. Using two GPIOs to measure the NTC voltage is not mandatory, but simplifies the calculations.

Figure 45. Example of NTC differential measurement

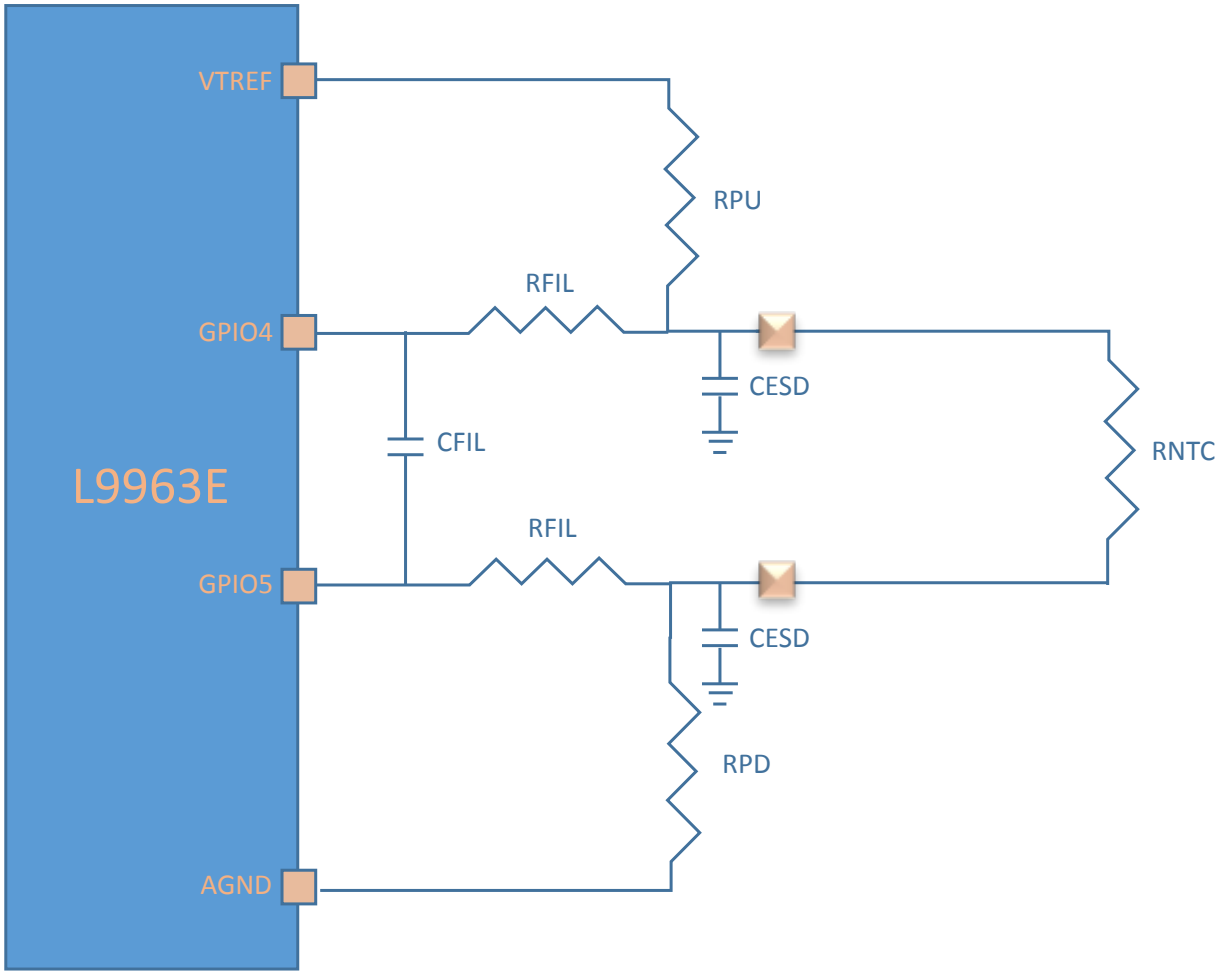


Table 84. NTC analog front end BOM for differential measurement

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{NTC}	10	kΩ	1%		Recommended external NTC typical value @25 °C. The NTCALUG02A103F is a good option for evaluation purposes
R_{FIL}	3.3	kΩ	10%	1.5 W	Protect the GPIO in case of external STG/STB. Limit the ESD inrush current. Filter the NTC signal: cut-off frequency is $f_C = \frac{1}{4\pi R_{FIL} C_{FIL}}$. Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.
C_{FIL}	100	nF	10%	16 V	Protect against ESD events and ISO spikes. Filter the NTC signal: cut-off frequency is $f_C = \frac{1}{2\pi R_{FIL} C_{FIL}}$. Connect to AGND.

Components	Value	Unit	Max. tolerance	Rating	Comments
C_{ESD}	47	nF	10%	100 V	Protect against ESD events and ISO spikes. Connect to GND_ESD
R_{PU}	10	kΩ	1%	0.5 W	Provide VTREF/3 polarization for NTC typical value. Protect VTREF pin in case of external short to battery/GND. Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead.
R_{PD}	10	kΩ	1%	0.5 W	Provide VTREF/3 polarization for NTC typical value. Protect AGND pin in case of external short to battery Do not use thin film resistors on these lines connected to ECU global pins. They could drift upon System Level ESD strikes. Use thick film or metal foil instead. Connect to AGND.

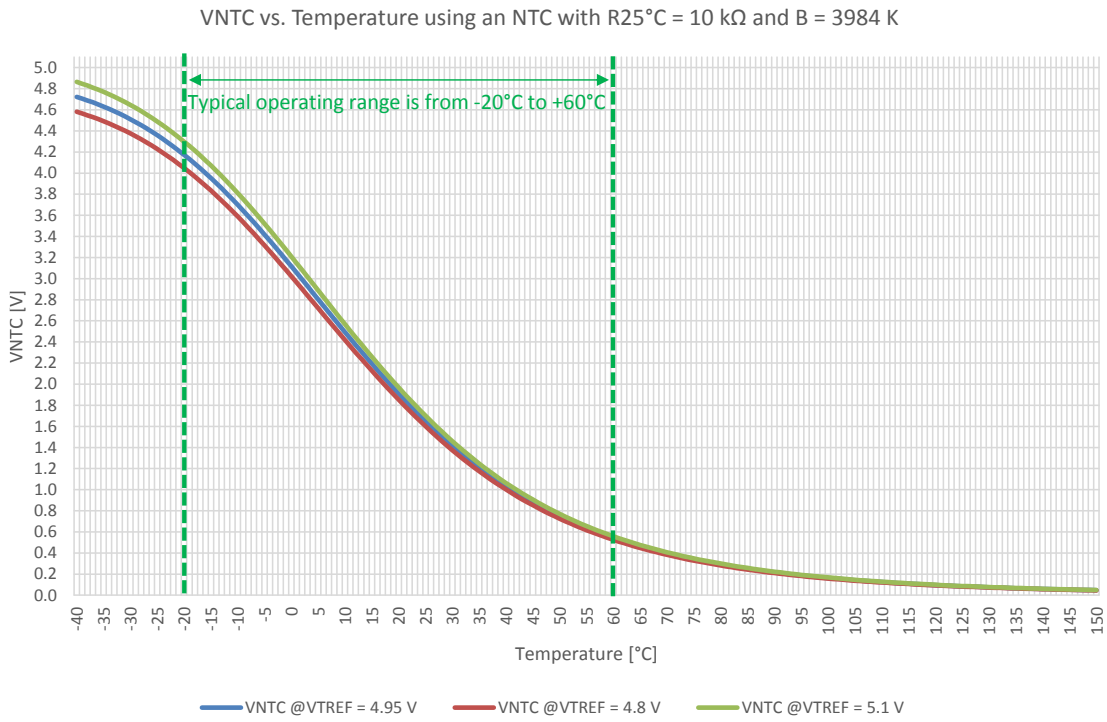
In this configuration, the NTC voltage varies according to the following equation:

NTC voltage variation with temperature (differential measurement)

$$\begin{cases} V_{NTC}\left(T\right) = V_{TREF} \times \dfrac{R_{NTC}(T)}{R_{NTC}(T) + 2R_{PU}} \\ R_{NTC}(T) = R_{25°C} \times e^{B\left(\frac{1}{T(K)} - \frac{1}{298.15}\right)} \\ T(°C) = \dfrac{B}{\frac{B}{298.15} + \ln\left(\dfrac{\frac{2R_{PU} \times V_{NTC}}{VTREF - V_{NTC}}}{R_{25°C}}\right)} - 273.15 \end{cases} \quad (19)$$

L9963E provides both V_{NTC} and VTREF measurements via SPI registers, thus allowing MCU to calculate cell temperature as in the Eq. (19).

Figure 46. VNTC vs. temperature example (differential measurement)



6.10 Unused pins

The following paragraph contains instructions about how to connect unused pins. If these indications are not met, L9963E will not operate properly.

6.10.1 Cell pins

6.10.1.1 Cell minimum configuration

The minimum configuration that allows L9963E correct functionality is the following:

- At least the following four cells must be mounted:
  - CELL1
  - CELL2
  - CELL13
  - CELL14
- The **VCELLX_EN** bit must be set to **'1'** only for these four cells, in order to allow correct conversion and diagnostics.
- Nominal stack voltage must be always higher than $V_{BAT\_UV\_WARNING}$.

6.10.1.2 Cell maximum configuration

The maximum configuration that L9963E can handle is:

- All the fourteen cells mounted
- The **VCELLX_EN** bit must be set to **'1'** for all the cells
- Nominal stack voltage must be always lower than the VBAT operating range specified in Table 2.

Refer to Figure 32 as an example.

6.10.1.3 Unmounted cells

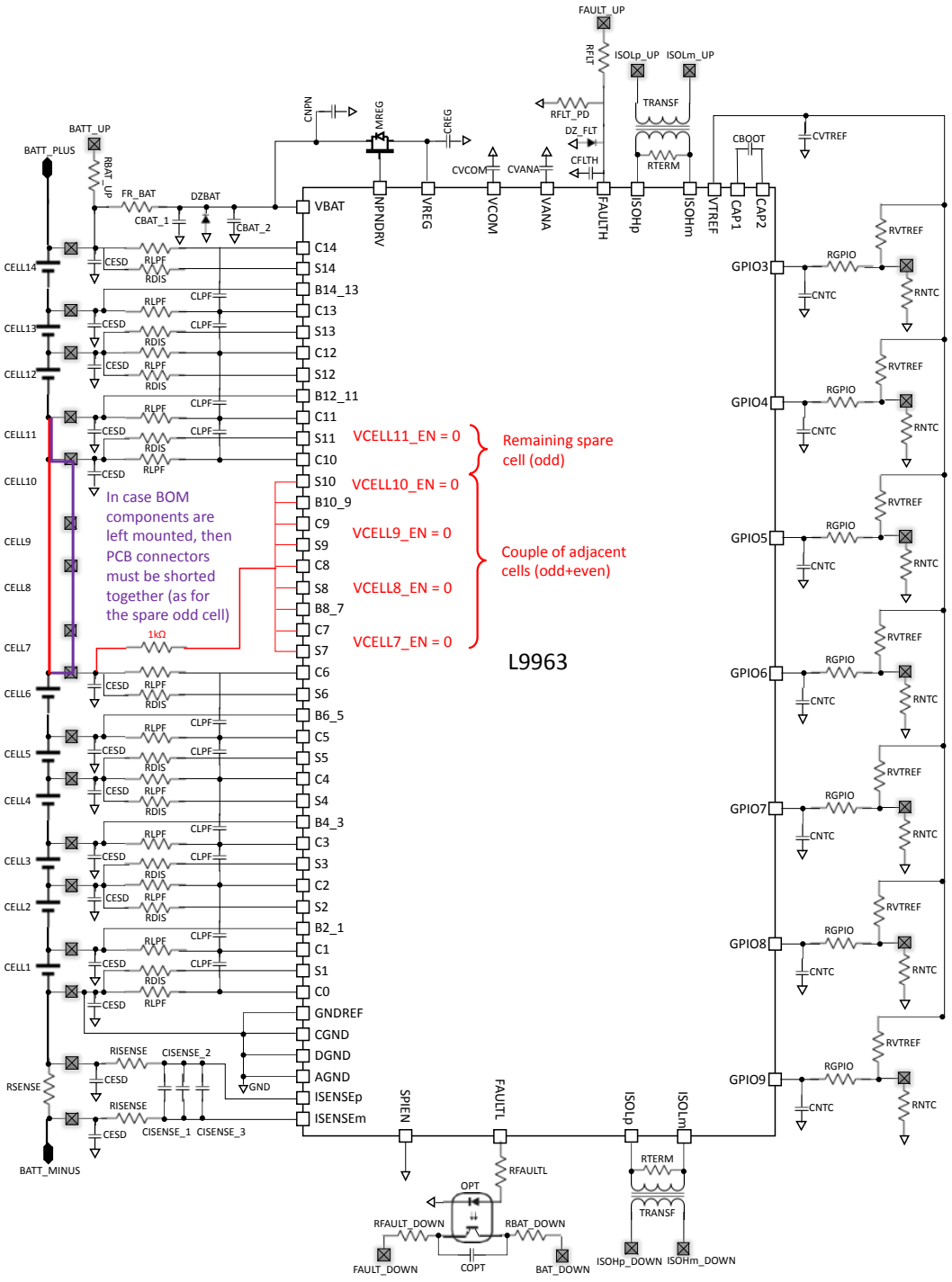
If less than 14 cells are mounted, the following indications must be followed in order to ensure proper measurement and diagnostic operation:

If **N** cells are not mounted:

- Unmount **N/2** ajacent couples as shown in Figure 47:
  - In case analog front end components are left mounted
    - Simply short unused cells PCB connectors
  - In case analog front end components are removed from BOM
    - Unused pins must be first shorted together to eliminate differential noise
    - Shorted traces must be connected to the PCB connector of the lower mounted cell, through a 1 kΩ resistor
- If a remaining spare cell has to be left unmounted, then it must be an odd cell, as shown in Figure 47:
  - In order to guarantee the correct biasing of the internal sensing & balancing circuitry, the recommended components must be mounted and connection to the busbar has to be done

Cells not mounted must have their corresponding **VCELLx_EN** bit set to **'0'** in order to disable the related diagnostics, otherwise wrong failures could be latched (such as cell UV).

Figure 47. **How to handle unmounted cells**



6.10.2 Unused GPIOs

The unused GPIOs must be connected in a proper way in order to avoid unwanted leakage.

6.10.2.1 GPIO3-9

When one pin among GPIO3 to GPIO9 is not used in application:

- It must be shorted to GND plane (AGND is recommended)
- It must be configured as Digital Input by user SW, in order to avoid being converted during **Voltage Conversion Routine**

6.10.2.2 *FAULT line (GPIO1-2)*

When **FAULT Line** is not used in application:

- GPIO1_FAULTH pin must be shorted (or pulled-down with a resistor) to GND plane (AGND is recommended)
- GPIO2_FAULTL pin must be connected to GND plane (DGND is recommended) through a 100 kΩ pulldown resistor

6.10.3 Current sense

When current sense is not used in application:

- Pin ISENSEp must be shorted to pin ISENSEm in order to reject differential noise
- The shorted trace must be connected to GND plane (AGND is recommended) in order to reject common mode noise

6.10.4 ISOH port

When the ISOH port is not used in application:

- Pin ISOHp and ISOHm must be shorted together in order to reject differential noise. They are internally pulled down to reject common mode noise.

6.10.5 Busbar connection

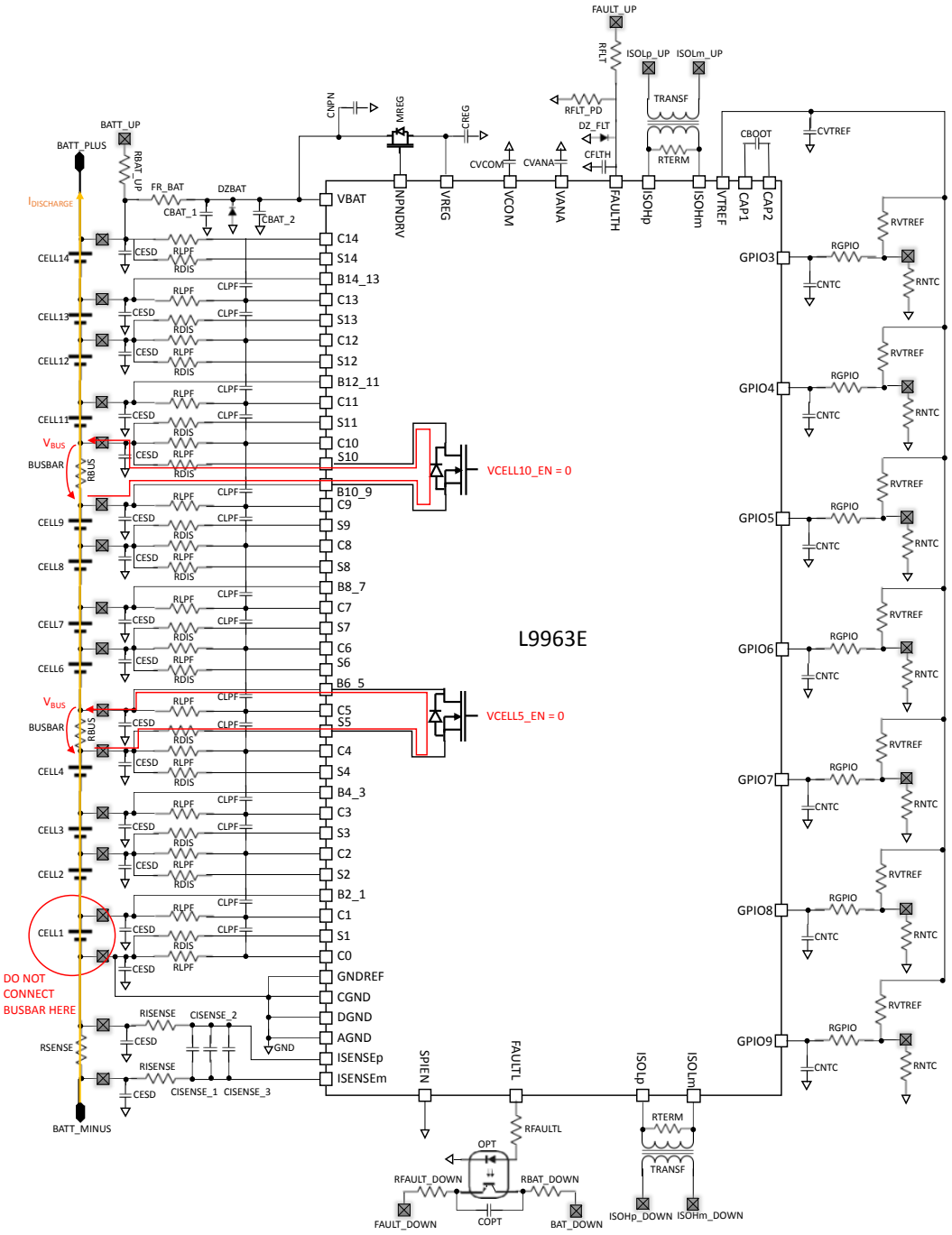
Figure 48 shows an example of application featuring small cell modules connected through a busbar. Since the busbar exhibits a small parasitic resistance R_{BUS}, a negative voltage drop equal to RBUS*ICELL appears at those cell terminals during the battery discharge phase.

Generally, such a drop never exceeds -2 V. L9963E has been engineered to sustain this kind of application without damaging the internal ESD clamps. In fact, all cell terminals (except the C0-C1 pair), can sustain negative differential voltages without undergoing any damage, as listed in Table 3. Busbar connection can be applied between any cell terminal pair, except the ones reserved for the four mandatory cells (refer to Section 6.10.1.1 Cell minimum configuration).

The internal balancing FET in parallel to the busbar can be protected mounting the same R_{DIS} discharge resistor recommended in Table 77. When negative voltage arises, a small current will flow through the body-drain diode. Such a current, equal to (V_{BUS} – V_{BODY_DRAIN}) / R_{DIS} will not damage the balancing FET. For instance, considering V_{BUS} = -2 V, V_{BODY_DRAIN} = 1 V and R_{DIS} = 39 Ω, the current will be limited to 25 mA.

Moreover, since this reverse current flows only through the balancing path, it will not alter neighboring cells measurement, since no drop occurs on the R_{LPF} filtering resistors, as shown in Figure 48.

Figure 48. **How to connect cell modules and busbar**



6.11 Communication architectures

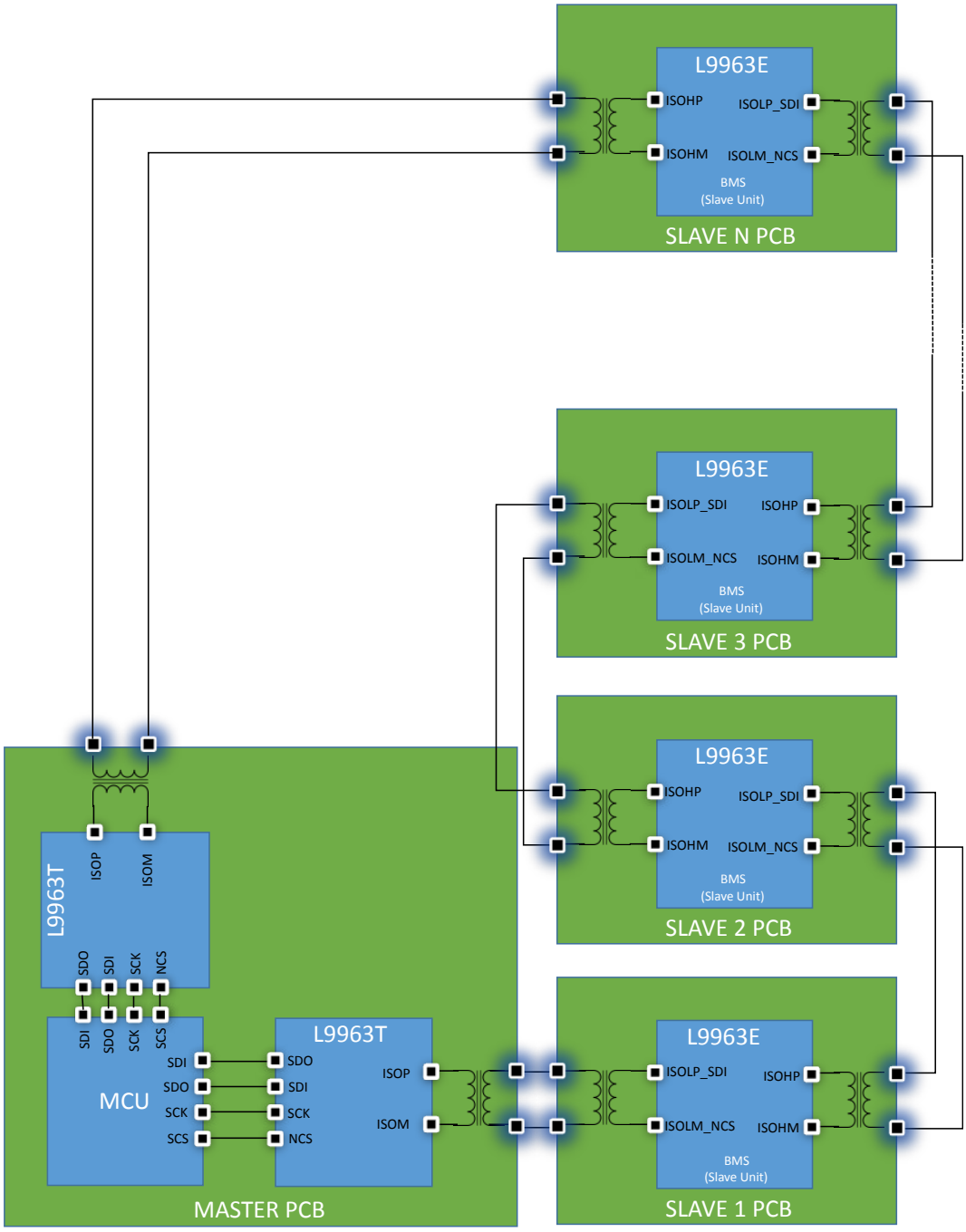
6.11.1 Distributed BMS

In the distributed approach, the BMS is made of a Master PCB and several Slave PCBs.

- L9963E in the Slave PCBs is configured with **SPIEN = 0**, thus communicating on the vertical interface through isolated SPI
- L9963E in the Master PCB is configured as SPI Slave and translates SPI frames into suitable pulses to be transmitted over the vertical interface

Transformer-Based Insulation is recommended on each Slave PCB in order to protect circuitry from shorts on external wires, while also adding robustness to BCI.

Figure 49. Distributed BMS

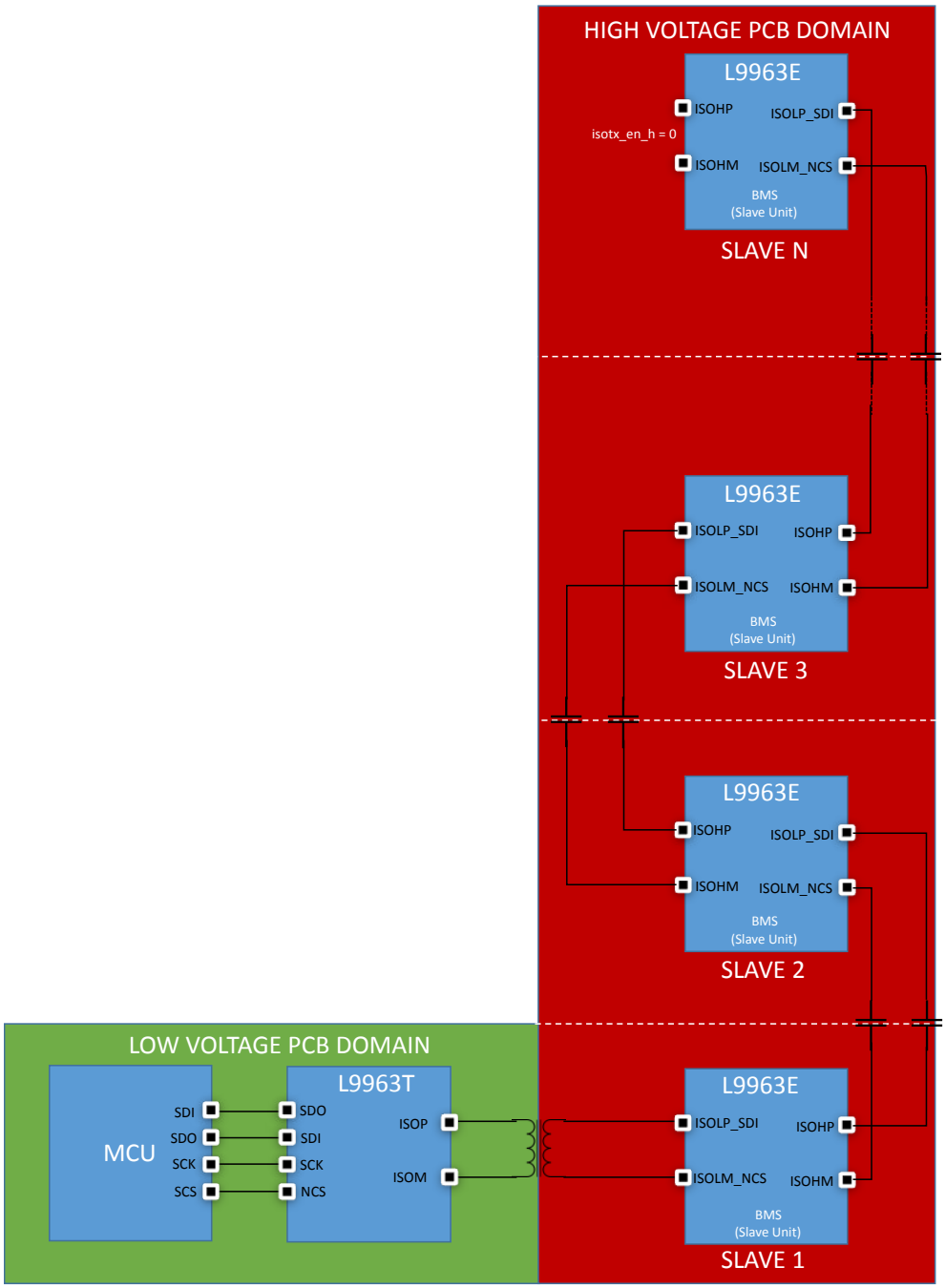


6.11.2 Centralized BMS

In the centralized approach, a single PCB holds the whole BMS circuitry. It features both Low Voltage and High Voltage domains:

- L9963E in the High Voltage domain is configured with **SPIEN = 0**, communicating on the vertical interface through isolated SPI, implementing **Capacitive-Based Insulation**.
- The L9963T transceiver positioned in the Low Voltage domain acts as SPI to isolated SPI transceiver, translating commands sent by the MCU via SPI into differential signals propagating through the vertical interface (and vice-versa). Alternatively, L9963E in Transceiver mode can be used instead of L9963T. In both cases, **Transformer-Based Insulation** is used.

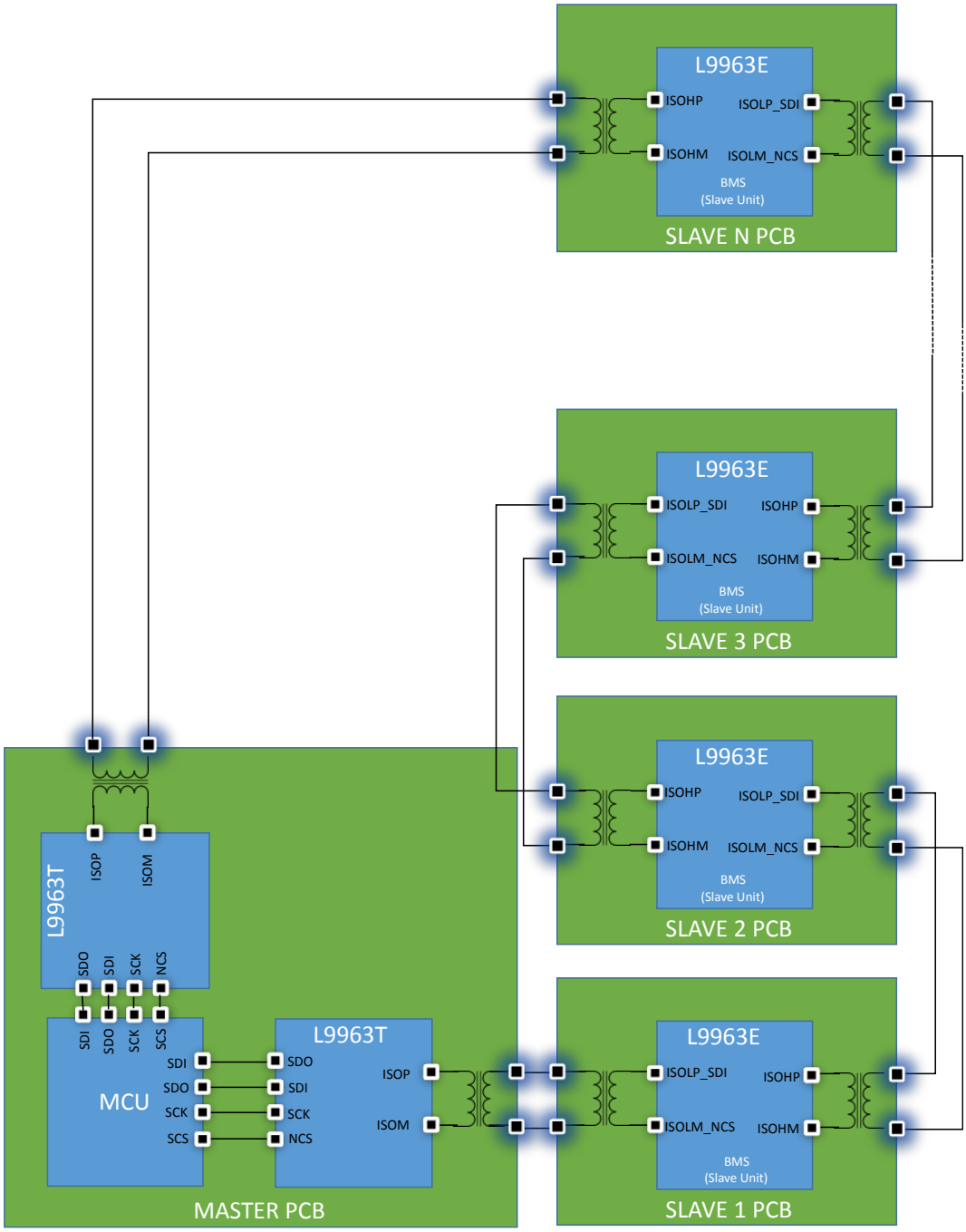
Figure 50. Centralized BMS



6.11.3 Dual access ring

The dual access ring topology allows a higher communication integrity level, guaranteeing recovery upon single open failure on communication wires. It requires 2 SPI peripherals on the MCU and 2 L9963E transceivers on the MASTER PCB.

Figure 51. Dual access ring



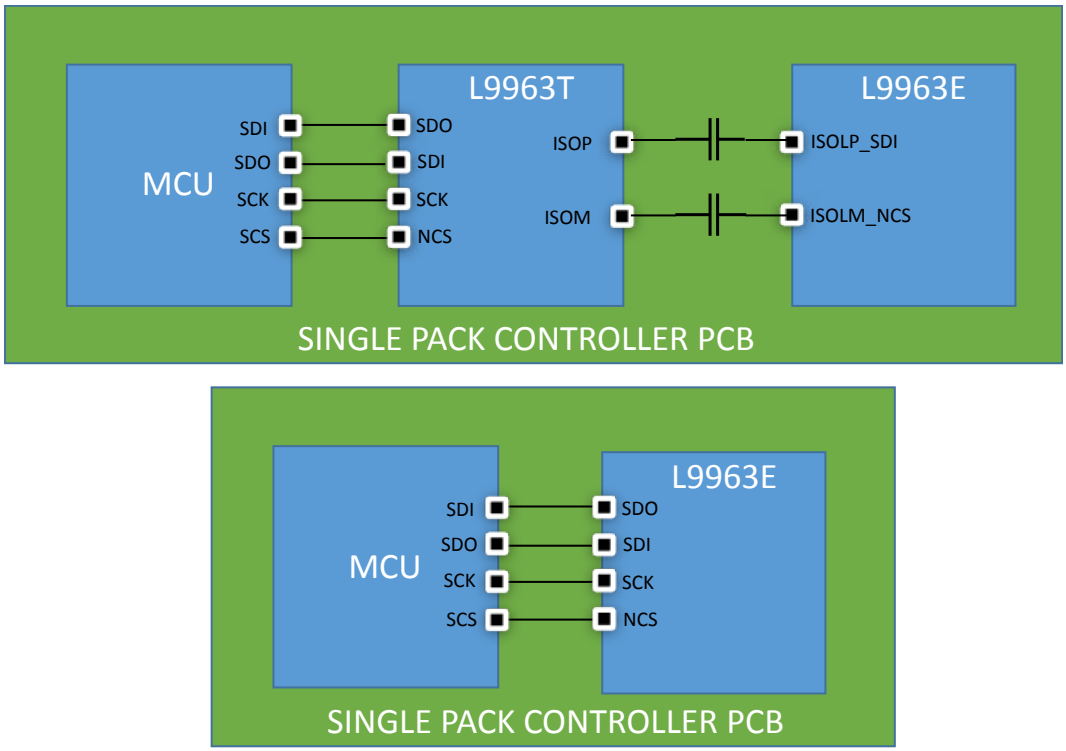
6.11.4 Single module BMS

In the single module approach, the MCU and L9963E monitoring the battery pack are placed on the same PCB.

Two scenarios are possible:

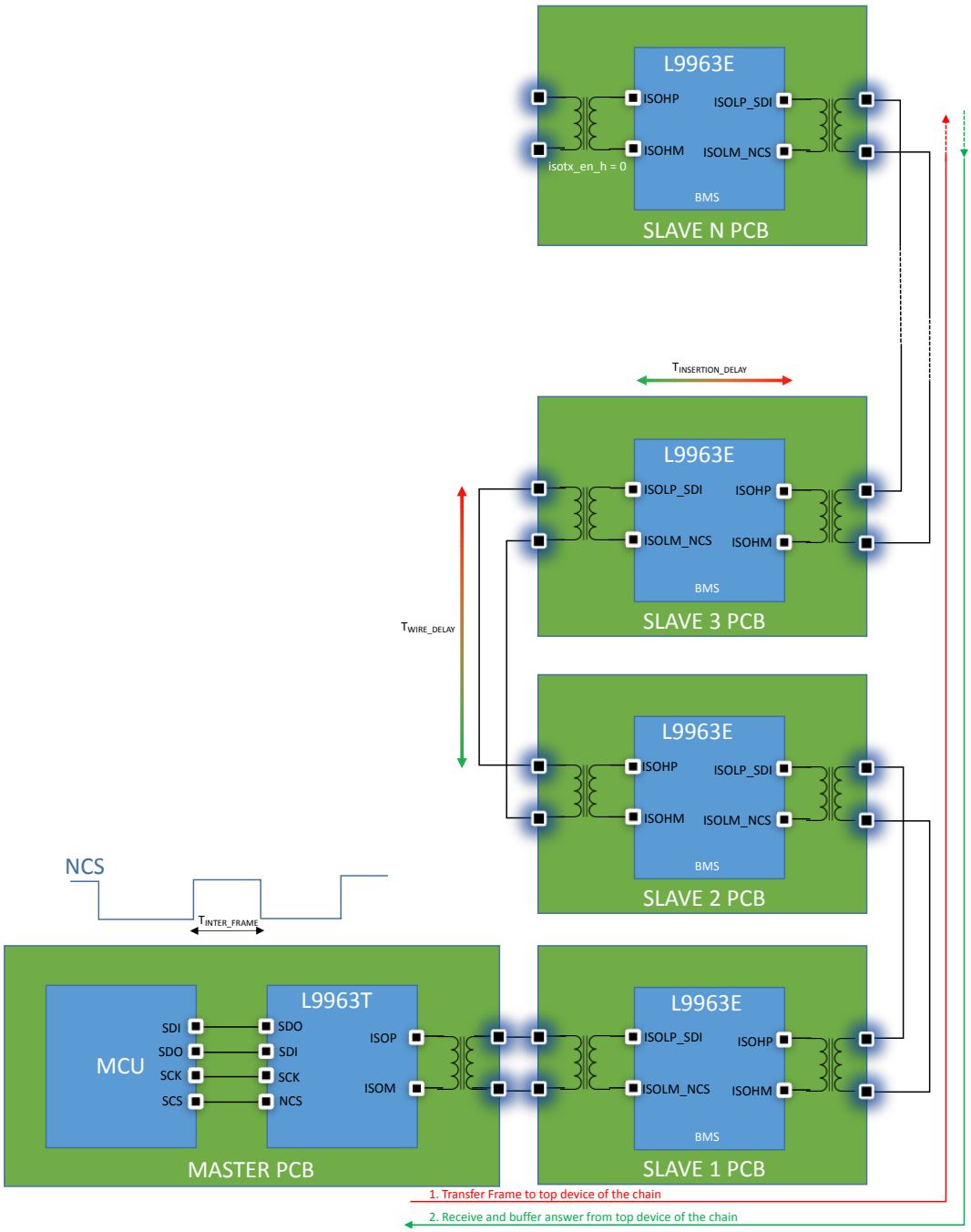
- Isolated BMS: in case BMS ground is different from MCU ground, an isolation stage is needed. The L9963T transceiver can be used along with **Capacitive-Based Insulation**. L9963E is configured with **SPIEN = 0**
- Non-Isolated BMS: in case BMS and MCU share the same ground, no isolation stage is needed. L9963E is configured with **SPIEN = 1** and directly connected to MCU SPI Master.

Figure 52. Single pack BMS (with isolation stage)



6.11.5 Inter-frame delay

Figure 53. **Inter-frame delay estimation**



Minimum inter-frame delay T_{INTER_FRAME} shall be enough to guarantee no conflict in the worst case represented by communication with the farthest unit of the daisy chain. The inter-frame delay can be estimated through the following equation:

Minimum Inter-Frame Delay Estimation

$$\begin{cases} T_{INTER\_FRAME_{min}} = 2 \times \left[N_{DEVICES} \times \left(T_{WIRE_{DELAY}} + T_{INSERTION_{DELAY}}\right) + 41 T_{BIT_{LENGTH}}\right] + T_{ANSWER\_DELAY} \\ T_{WIRE\_DELAY} = 3.335 \times \sqrt{\varepsilon_r} \times L_{WIRE}[ns] \\ T_{INSERTION_{DELAY}} = \dfrac{T_{BIT\_LENGTH}}{3} \\ T_{BIT_{LENGTH}} = T_{BIT_{LENGHT_{FAST}}} \, or \, T_{BIT_{LENGHT_{SLOW}}} \\ T_{ANSWER\_DELAY} = T_{ANSWER\_DELAY\_FAST} \, or \, T_{ANSWER\_DELAY\_SLOW} \end{cases} \quad (20)$$

Where **ε_r** is the relative permittivity of the dielectric material of the twisted pair, and **TBIT_LENGTH** depends on the **iso_freq_sel** bit. The insertion of a L9963E introduces less than a bit time delay. Each L9963E acts as a buffer, regenerating the signal. Hence, attenuation should not represent an issue.

For instance, a daisy chain of 14 devices with 2 m long wires between each node, with a twisted pair made of copper conductor and polyethylene insulator (ε_r = 2.25), requires a **38.25 µs** inter-frame delay when operating in high frequency mode, and a **282 µs** delay when in low speed configuration.

ST recommends using at least **1.5 times** the minimum inter-frame delay estimated. This compensates the formula inaccuracy and all the external factors that could influence transmission delay. For instance, in the example above, the recommended inter-frame delay would be **425 µs** for low frequency operation and **60 µs** for the high speed configuration.

Since the protocol is out of frame, when switching from a frequency mode to another, the following frame must still be issued after the old inter-frame delay.

6.11.6 Choosing the twisted pair

L9963E vertical communication interface has been extensively validated at bench using a 24 AWG, 10 m long, unshielded twisted pair, whose insulating material is a 100 V rated PVC, with a relative permittivity ε_r = 4.

Different wires can be used, taking into account the following recommendations:

- Changing the wire AWG and/or length may affect signal attenuation. If signal appears too attenuated at receiver side, the transmitter amplitude can be increased acting on **out_res_tx_iso**
- Increasing the wire length will lead to higher signal propagation delays, eventually degenerating in inter-symbolic interference. Propagation delay can be estimated using the following equation

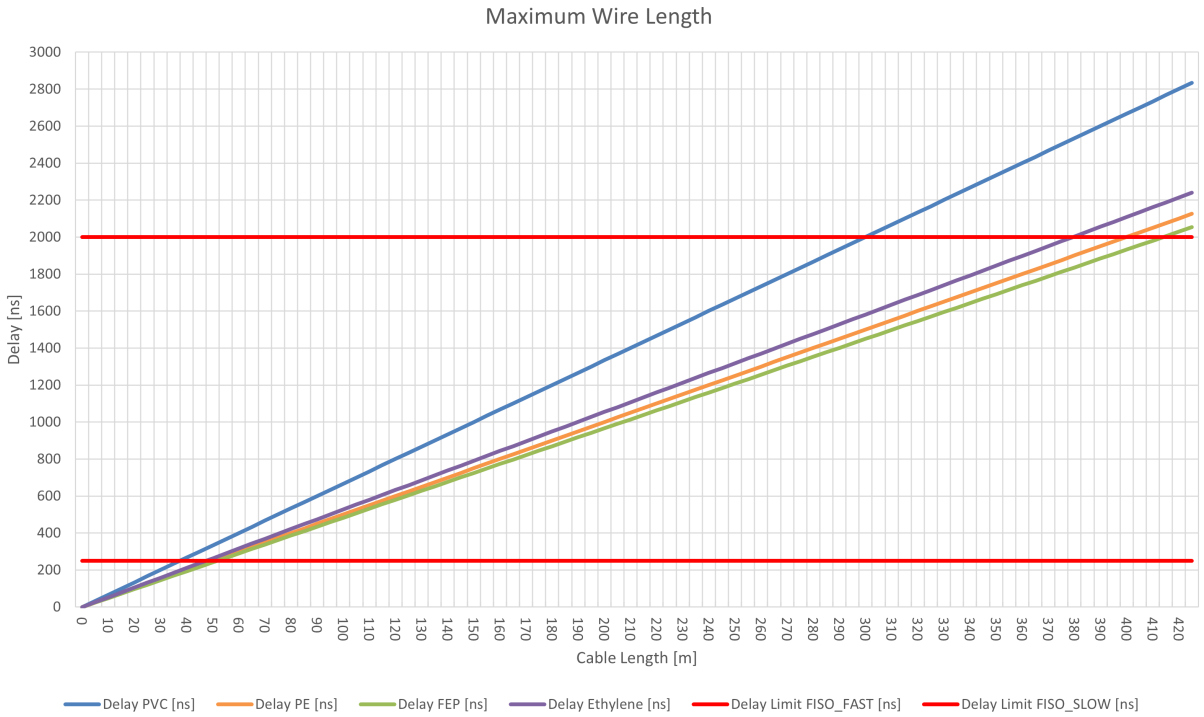
  Signal propagation delay estimation on vertical communication interface

$$T_{PD}\left[ns/m\right] = 3.335\sqrt{\varepsilon_r} \quad (21)$$

Figure 54 plots the signal propagation delay (ns) vs. different wire insulating materials. Referring to Figure 10, if such a delay exceeds $2T_{PULSE}$, the transmitter starts generating a new symbol before the receiver has finished receiving the previous one. The wire becomes acting as a transmission line and intersymbolic interference may occur.

The worst case is represented by operation at high-frequency (F_{ISO_FAST}), determining a constraint of 250 ns max. propagation delay. On the contrary, switching to low frequency (F_{ISO_SLOW}) allows reaching longer distances (paying always attention to signal attenuation, that must be verified on receiver side).

Figure 54. Maximum wire length according to wire insulator and operating frequency



6.12 Transceiver mode

L9963T is the recommended device to be used as transceiver in daisy chain topologies. Nevertheless, due to legacy, L9963E can still be configured as a transceiver by applying proper SPI settings.

6.12.1 Configuring L9963E as transceiver

To configure L9963E as transceiver, the following connections must be applied to the power supply pins before the device is first powered on (refer to Figure 55):

- VBAT, VREG, VCOM and VTREF pins must be shorted together and connected to a 5V power supply (VDD5; might be the same regulator supplying the microcontroller)
- The NPNDRV, CAP1 and CAP2 must be left floating
- VANA must be connected to a tank capacitor as in BMS mode

After the first powerup, MCU can force the transceiver mode by setting **transceiver_on_by_up** and **transceiver_valid_by_up** bit.[end]

L9963E configured as transceiver:

- Does not execute **Voltage Conversion Routine**
- Does not execute **Coulomb Counting Routine**
- Is sensitive to VCOM and VTREF OV/UV failures
- Is not sensitive to VREG UV and VBAT UV/OV failures
- Propagates any failure received via **FAULT Line** to the MCU through the FAULTL pin
- Does not activate **Cell Balancing**

6.12.2 Transceiver pinout

The following table lists pin functions and external connections for transceiver usage:

Table 85. Pinout description for transceiver mode

Pin	Type(1)	Connect to	Comments
VBAT	P	VDD5	
NPNDRV	AO	Leave Floating	VREG regulator internally disabled
VREG	P	VDD5	
VCOM	P	VDD5	VCOM regulator internally disabled
VANA	P	Tank capacitor	Same tank as in BMS mode. Refer to Table 73
FAULTH	DI	AFE circuitry	Same analog front end as in BMS mode (refer to Table 79). The only exception is RFLT_PD = 47 kΩ instead of 18 kΩ
ISOHp	DIO	AFE circuitry	Same analog front end as in BMS mode. Refer to Table 73
ISOHm	DIO	AFE circuitry	
VTREF	P	VDD5	VTREF regulator internally disabled
CAP1	P	Leave Floating	Bootstrap internally disabled
CAP2	P	Leave Floating	
GPIO3-6	AI	GND	
WAKEUP	DI	Microcontroller Digital Output	GPIO7 is used as wakeup input determining operation in Sleep/Normal states
SCK	DI	Microcontroller SCK	Lower port is forced to operate as SPI, regardless of the SPIEN pin. However, to add robustness, the SPIEN pin must be connected to VDD5, thus adding some redundancy
SDO	DO	Microcontroller SDI	
NCS	DI	Microcontroller CS	
SDI	DI	Microcontroller SDO	
FAULTL	DO	Microcontroller Digital Input	Propagates the FAULTH signal
SPIEN	DI	VDD5	Lower port is forced to operate as SPI
ISENSEp	AI	GND	Current sense interface is disabled
ISENSEm	AI		
AGND	G	GND	
DGND	G	GND	
CGND	G	GND	
GNDREF	G	GND	
CX	AI	GND	Cell measurement is disabled
SX	AO	Leave Floating	Cell balancing is disabled
B_{X+1_X}	AO	Leave Floating	

1. *P = Power supply, AO = Analog Output, DI = Digital Input, DIO = Digital Input/Output, AI = Analog Input, DO = Digital Output, G = Ground.*

6.12.3 Transceiver application circuit and bill of material

Figure 55. **Transceiver circuit**

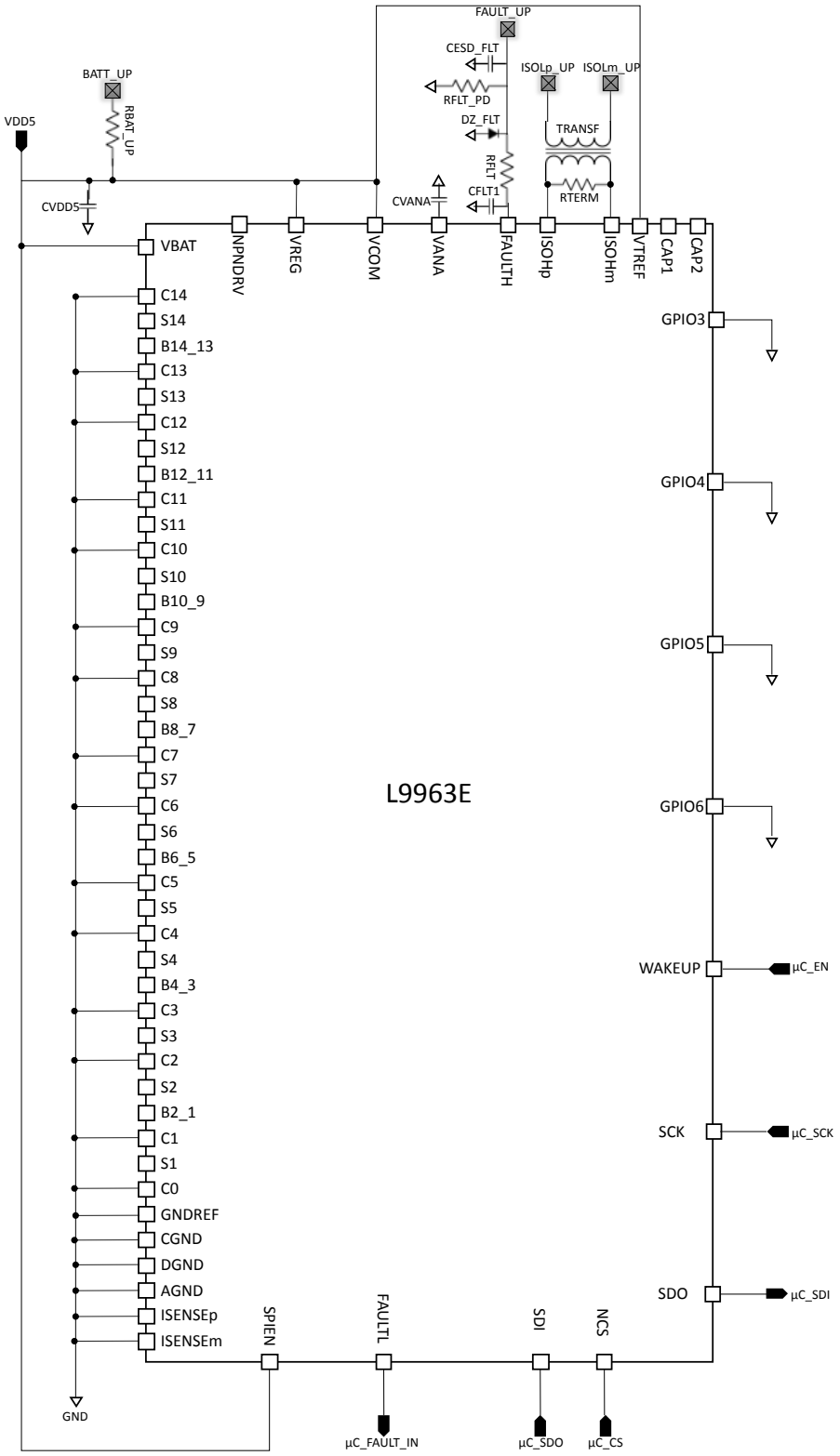


Table 86. **Recommended components for transceiver use**

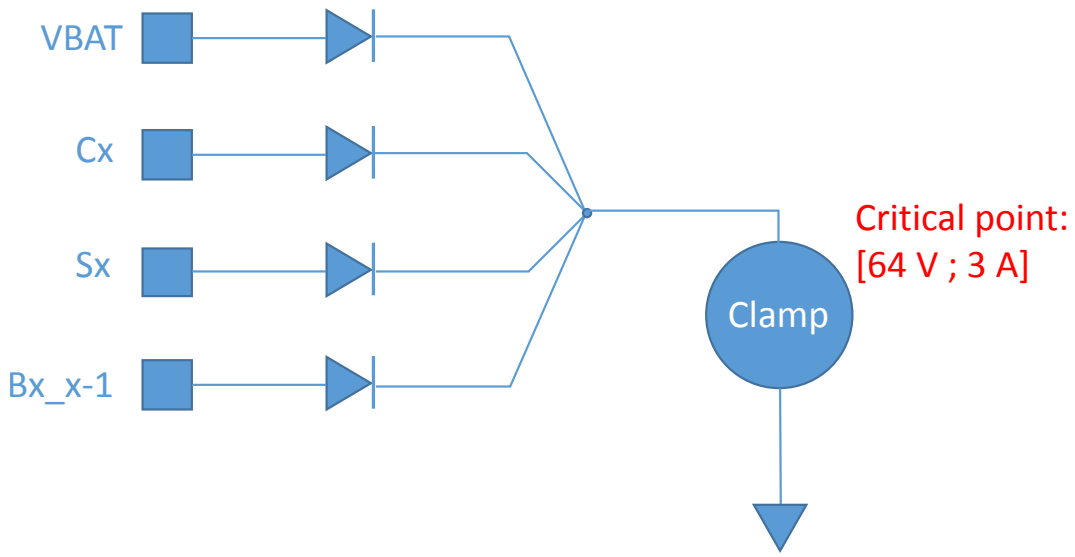
Components	Value	Units	Tolerance	Comments
C_{VDD5}	10	µF	10%	Provide battery stabilization for the VCOM and VREG power inputs. 6.3V rating
R_{BAT_UP}	10	kΩ	10%	Protect against STG and provide polarization for FAULT signal propagation to the upper BMU
C_{VANA}	2.2	µF	10%	Tank for the VANA regulator. 6.3 V rating
C_{ESD_FLT}	6.8	nF	10%	ESD capacitor for the FAULT input. 6.3 V rating
R_{FLT_PD}	47	kΩ	10%	Pull-down resistor for FAULT input
D_{Z_FLT}	4.7	V		The SZMM3Z4V7T1G is recommended for clamping the voltage on the FAULT input
R_{FLT}	10	kΩ	10%	Filtering the FAULT signal and limiting the ESD inrush current
C_{FLT1}	2.2	nF	10%	Filtering the FAULT signal and improving ESD protection. 6.3 V rating
TRANSF				The ESMIT-4180/A is recommended for isolated communication interface
R_{TERM}	120	Ω	10%	ISO line termination

6.13 Hotplug

Care must be taken while connecting the battery cells to the battery monitoring PCB. Each cell connection causes a hotplug phenomenon that can damage L9963E if the energy flowing through the device is not properly limited.

L9963E features an integrated clamp connected to all cell-relevant pins. Such a structure is capable of withstanding hotplug transients up to its critical point, shown in Figure 56. Hotplug energy input to a pin is entirely deviated towards the centralized clamp and cannot propagate to other pins, since protection diodes will block the current.

Figure 56. **L9963E centralized clamp**



6.13.1 Requirements for safe cell hotplug

L9963E can safely handle hotplug if the following conditions are met:

- The recommended components and configurations for cell voltage sensing and balancing are used (refer to Section 6.3 Cell voltage sensing circuit and Section 6.6.1 Cell balancing with internal MOSFETs)
- The **VBAT**, **Cx**, **Sx** and **Bx_x-1** pin absolute voltage vs AGND during hotplug must not exceed **64 V**

Zeners in parallel to each cell are not needed, since the device can withstand very high transient differential voltages between those pins, as listed in Table 3. Moreover, R_{LPF} resistors in series to **Cx** pins will limit the current flowing into the centralized clamp (green paths in Figure 57).

The internal balancing MOSFETs mounted between **Bx_x-1** and **Sx** pins are equipped with zener feedback that clamps their VDS to V_{BAL_CLAMP} during hotplug (orange paths in Figure 57). The feedback will turn them ON, allowing the hotplug current to flow through their channel. Balancing resistors (R_{DIS}) will limit the current.

Hotplug current also flows through the body-drain diode of the internal balancing MOSFETs. Also in this case, current is limited by R_{DIS} balancing resistors (orange paths in Figure 57).

6.13.2 Additional external components for hotplug protection

In case **Requirements for safe cell hotplug** are not met by the application, additional external components must be mounted in order to limit the hotplug current flowing in the centralized ESD clamp.

The most critical paths are those involving **VBAT** and **Bx_x-1** pins (red paths in Figure 57), since no series resistance is present to limit the inrush current in the centralized clamp.

Adding the structure in Figure 57 on the GND path will help withstanding the hotplug by limiting the inrush current incoming from any L9963E pin connected to the centralized clamp.

Working principle is the following:

- When L9963E is OFF and no cell is connected, the VTREF/VREG regulator is shut down and M_{HOT} is safely kept off by the R_{PD} pull down resistor
- Upon the first hotplug event, inrush current incoming from the centralized clamp is forced to flow into R_{HOT} resistor, which offers proper limiting in order to not violate the critical point shown in Figure 56
- Any VDS voltage spike on MHOT during hotplug could be coupled to the gate via the parasitic Miller capacitance. Unwanted turn-on is safely filtered by C_{GS}, that helps keeping VGS below the threshold voltage. Hence, M_{HOT} will stay OFF during hotplug.
- After L9963E powerup and addressing
  - If M_{HOT} is connected to VTREF, MCU has to program **VTREF_EN = 1** and **VTREF_DYN_EN = 0** in order to turn on M_{HOT}. Using the option **VTREF_EN = 1** and **VTREF_DYN_EN = 1** is not recommended when M_{HOT} is connected to VTREF. If VTREF dynamic enable is required by application, connect MHOT to VREG instead.
  - If M_{HOT} is connected to VREG, no action is required, since this regulator will turn on autonomously
- Finally, during L9963E normal operation, M_{HOT} will be ON, guaranteeing a very low impedance path (few mΩ) on the AGND line.
  - Such a small shift between L9963E GND and battery pack GND will not alter cell measurement at all, since cell ADCs are fully differential. Hence, both cell and sum of cells measurements will be accurate.
  - Moreover, since L9963E only drains few mA from the battery pack, error introduced on the VBAT stack measurement via internal voltage divider will be negligible
  - Also the CSA used for Coulomb Counting features a fully differential architecture, being immune to such a small common mode shift

Figure 57. **Hotplug paths**

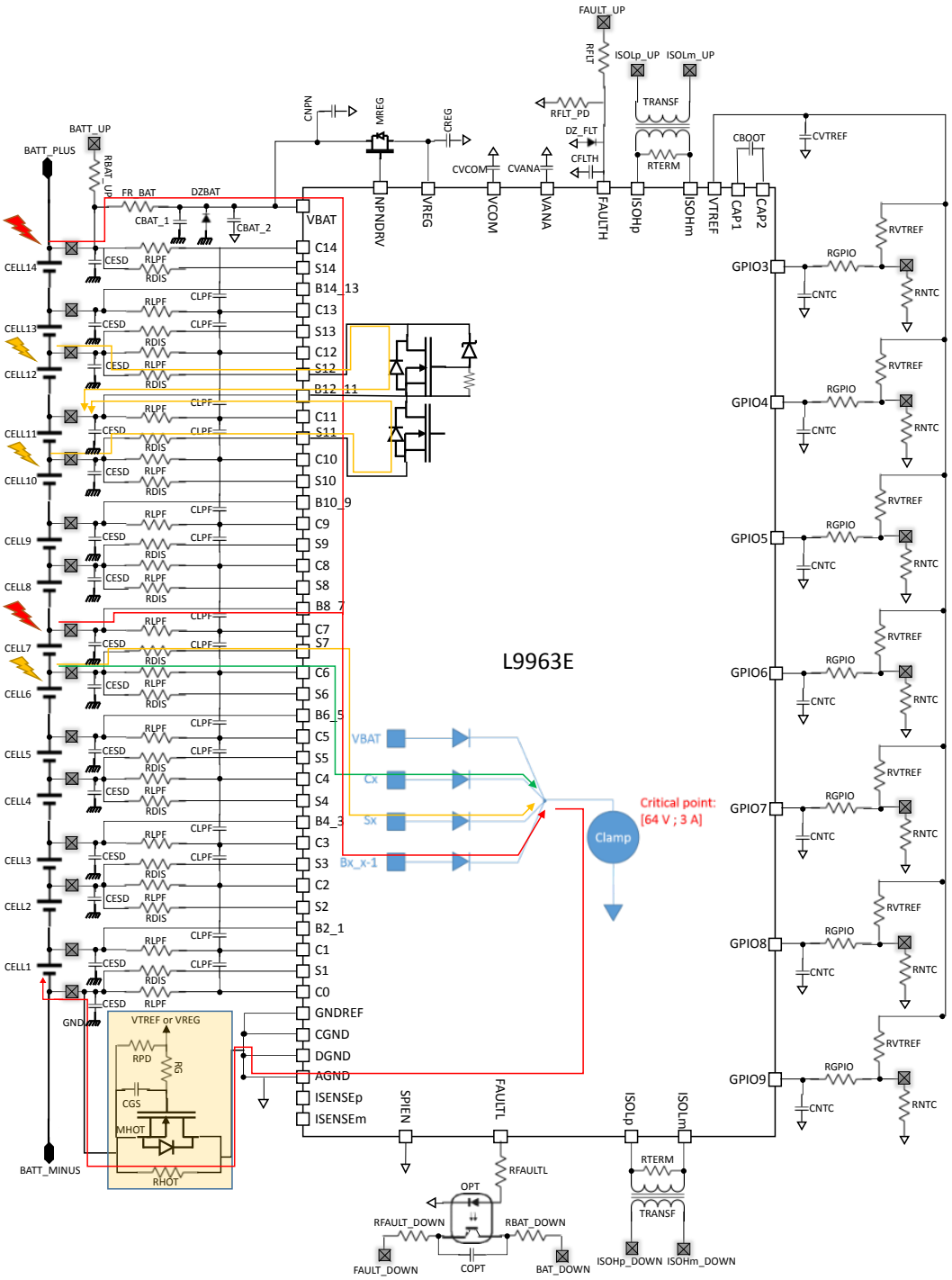


Table 87. **Additional components for hotplug protection**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{HOT}	47	Ω	10%	1 W	Limits the inrush current flowing through the centralized clamp upon hotplug
M_{HOT}				100 V	The PMN280ENEAX is the recommended component to sustain hotplug energy in centralized BMS with very high voltage battery packs. It features 100 V breakdown voltage, so it won't be damaged during hotplug. Its R_{DS_ON} is 12.5 mΩ, thus guaranteeing a very low impedance path on the GND line, once in normal operation
				60 V	The STN4NF06L is the recommended component to sustain hotplug energy in distributed BMS. It features 60 V breakdown voltage, so it won't be damaged during hotplug. Its R_{DS_ON} is 21 mΩ, thus guaranteeing a very low impedance path on the GND line, once in normal operation
C_{GS}	4.7	nF	10%	16 V	Filters any VDS spike coupled to the gate during hotplug via the M_{HOT} parasitic Miller capacitance. Along with R_G, adds a delay in M_{HOT} turn on path, thus keeping the transistor safely OFF during hotplug.
R_{PD}	100	kΩ	10%	1/10 W	Keeps M_{HOT} safely OFF when L9963E power is removed. It only drains 50 uA from VTREF during normal operation
R_G	1	kΩ	10%	1/10 W	Limits the VTREF inrush current when turning ON M_{HOT}

7 Recommended soldering profile

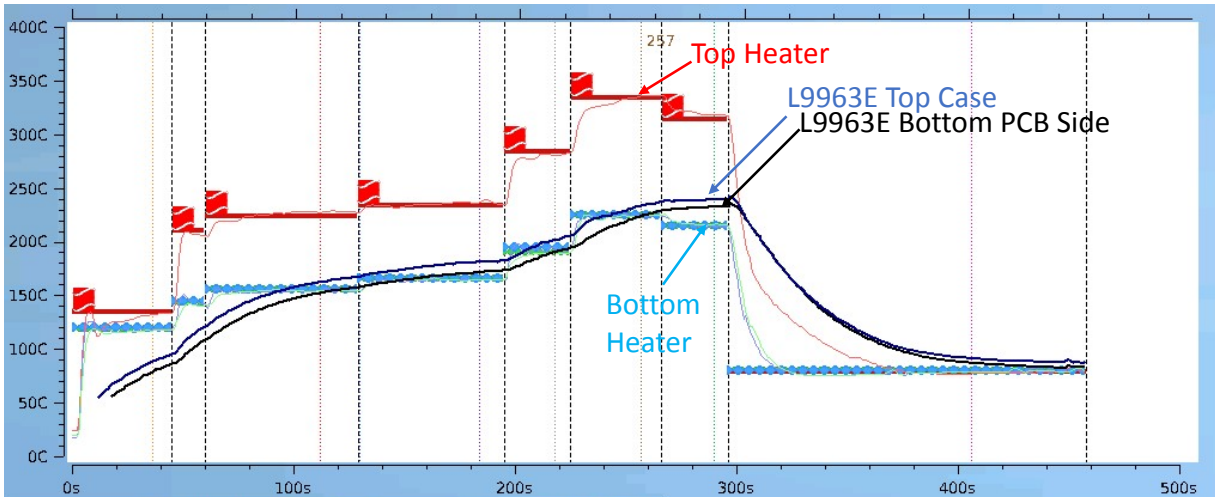
The soldering profile in Figure 58 is compliant to JEDEC J-STD-020 standard. It is recommended to follow these indications in order to achieve the best performances in terms of accuracy and reliability.

Table 88. Reflow soldering profile according to JEDEC J-STD-020

Item	Description
Reflow category	
Reflow Condition	Sn-Pb eutectic assembly
Package Type	Thickness < 2.5 mm and volume < 350 mm^3
Preheat	
Minimum temperature	Ts_{min} = 100 °C
Maximum temperature	Ts_{max} = 150 °C
Duration	ts = 60-120 s
Liquidus phase	
Liquidus Temperature	T_L = 183 °C
Average ramp-up rate (from T_L to T_p)	3°C/s max
Peak Temperature	T_p = 240 °C
Peak Duration	t_p = 10-30 s
Ramp-down	
Ramp-down rate (from T_p to T_L)	6°C/s max.
Ramp-down duration (T_p to 25 °C)	6 min. max.

Note: all temperatures are referred to the package top case.

Figure 58. Recommended soldering profile

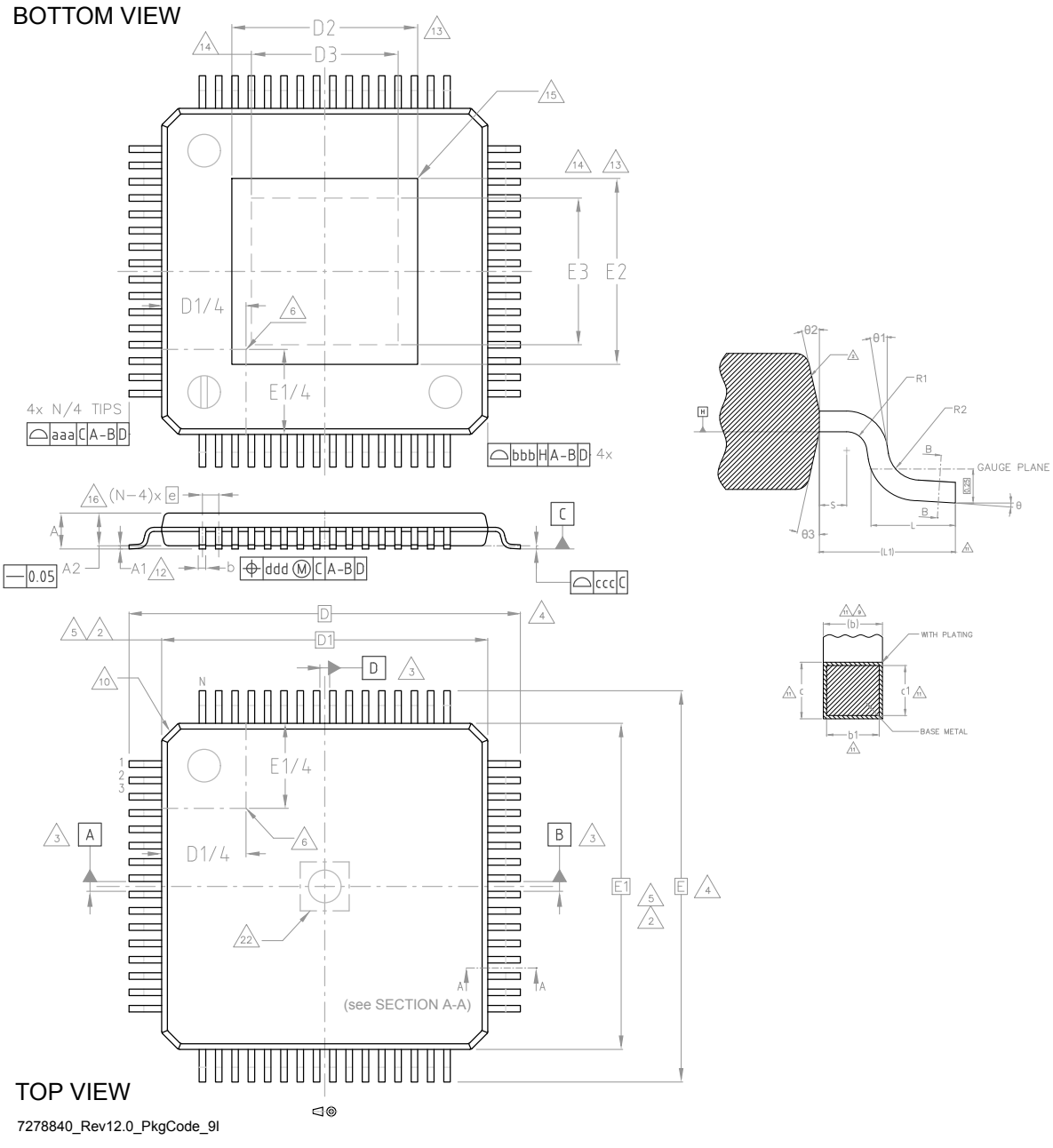


8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 TQFP 10x10 64L exposed pad down package information

Figure 59. TQFP 10x10 64L exposed pad down package outline



GADG091220191138PKG9I

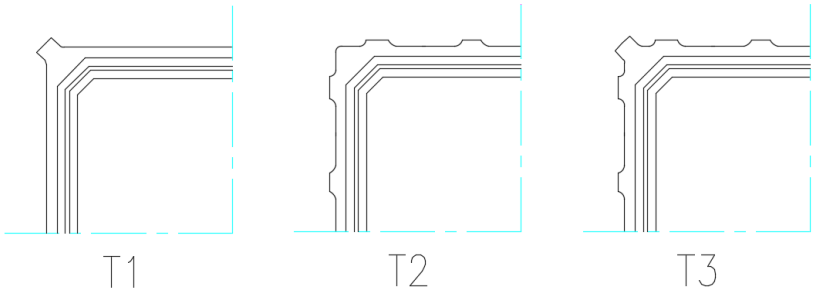
Table 89. **TQFP 10x10 64L exposed pad down package mechanical data**

Ref	Min.	Typ.	Max.	Note (see # in Notes below)
Θ	0°	3.5°	7°	-
Θ1	0°	-	-	-
Θ2	11°	12°	13°	-
Θ3	11°	12°	13°	-
A	-	-	1.2	15
A1	0.05	-	0.15	12
A2	0.95	1	1.05	15
b	0.17	0.22	0.27	9, 11
b1	0.17	0.2	0.23	11
c	0.09	-	0.2	11
c1	0.09	-	0.16	11
D	-	12.00 BSC	-	4
D1	-	10.00 BSC	-	2, 5
D2	See VARIATIONS			13
D3	See VARIATIONS			14
e	-	0.50 BSC	-	-
E	-	12.00 BSC	-	4
E1	-	10.00 BSC	-	2, 5
E2	See VARIATIONS			13
E3	See VARIATIONS			14
L	0.45	0.6	0.75	-
L1	-	1.00 REF	-	-
N	-	64	-	16
R1	0.08	-	-	-
R2	0.08	-	0.2	-
S	0.2	-	-	-
Tolerance of form and position				
aaa	-	0.20	-	1, 7, 19
bbb	-	0.20	-	
ccc	-	0.08	-	
ddd	-	0.08	-	
VARIATIONS				
Pad option 6.0 x 6.0 (T3)				
D2	-	-	6.40	13, 14
E2	-	-	6.40	
D3	4.80	-	-	
E3	4.80	-	-Notes	

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.

2. The Top package body size may be smaller than the bottom package size up to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. End user should verify D2 and E2 dimensions according to specific device application.



NOTE: number, dimensions and position of shown grooves are for reference only.

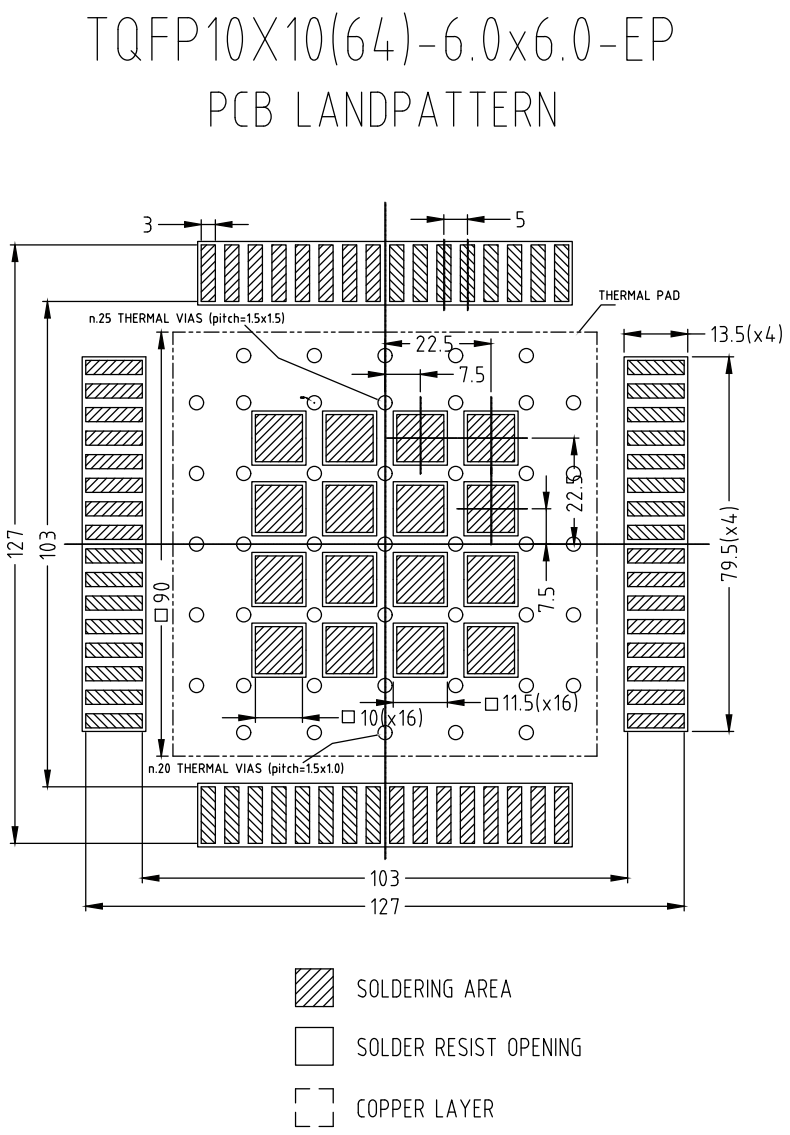
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.
17. For Tolerance of Form and Position see Table 89.
18. Critical dimensions:
    a. Stand-off
    b. Overall width
    c. Lead coplanarity

19. For Symbols, Recommended Values and Tolerances see Table below:

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension "e" as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".	This tolerance is normally compounded with tolerance zone defined by “b”.

20. Notch may be present in this area (MAX 1.5 mm square) if center top gate molding technology is applied. Resin gate residual not protruding out of package top surface.

Figure 60. Recommended footprint



NOTE:
This is a draft proposal only and it might be not in line with customer or pcb supplier design rules.

Note: Dimensions in the footprint of Figure 60 are mm.

Parts marked as ES are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Revision history

Table 90. **Document revision history**

Date	Version	Changes
11-Feb-2021	1	Initial release.
04-Mar-2021	2	Updated *Table 6. Power Management*.
09-Apr-2021	3	Added Note in *Table 39. Cell voltage ADC electrical characteristics*. Updated *Table 19. SPI protocol: single access addressed frame (write and read)*.
11-Jun-2021	4	Minor text changes in: • *Table 83. NTC analog front end BOM for single ended measurement (updated C_{FIL} value)*; • *Table 84. NTC analog front end BOM for differential measurement (updated C_{FIL} value)*.
05-Jul-2021	5	Updated *Table 42. Balancing FSM*.
22-Nov-2021	6	Updated *Figure 54. Maximum wire length according to wire insulator and operating frequency*.
13-Dec-2021	7	Typo corrections.
17-Jan-2022	8	Typo correction: changed hyperlink to "Table 2" in *Section 4.1.4 Power up sequence*.
04-Mar-2022	9	Updated *Figure 57. Hotplug paths*. Minor text changes in *Section 4.1.4 Power up sequence*.
30-Mar-2022	10	Updated "Equation 17" in *Section 4.13.1 Coulomb counting*.
23-Sep-2022	11	Updated *Section 6.10.1.3 Unmounted cells*. Minor text changes in *Section 4.11.5 PCB open diagnostic*.
21-Nov-2022	12	Minor text changes in Table 2. Operating ranges.

Contents

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