S-8269B Series

OVERCURRENT MONITORING IC FOR MULTI-SERIAL-CELL PACK

The S-8269B Series is an overcurrent monitoring IC for multi-serial-cell pack including high-accuracy voltage detection circuits and delay circuits.
By using an external overcurrent detection resistor, the S-8269B Series realizes high-accuracy overcurrent protection with less effect from temperature change.

■ Features

- High-accuracy voltage detection circuit
  - Discharge overcurrent detection voltage 1: 0.0030 V to 0.1000 V (0.5 mV step) Accuracy ±1.5 mV
  - Discharge overcurrent detection voltage 2: 0.010 V to 0.100 V (1 mV step) Accuracy ±3 mV
  - Load short-circuiting detection voltage: 0.020 V to 0.100 V (1 mV step) Accuracy ±5 mV
  - Charge overcurrent detection voltage: −0.1000 V to −0.0030 V (0.5 mV step) Accuracy ±1.5 mV
- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary)
- Discharge overcurrent control function
  - Release condition of discharge overcurrent status: Load disconnection
  - Release voltage of discharge overcurrent status: V_{DIOV1}, V_{RIOV} = V_{DD} × 0.8 (typ.)
- High-withstand voltage: VM pin and CO pin: Absolute maximum rating 28 V
- Low current consumption
  - During operation: 2.0 µA typ., 4.0 µA max. (Ta = +25°C)
- Wide operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Package

- SNT-6A

■ Block Diagram

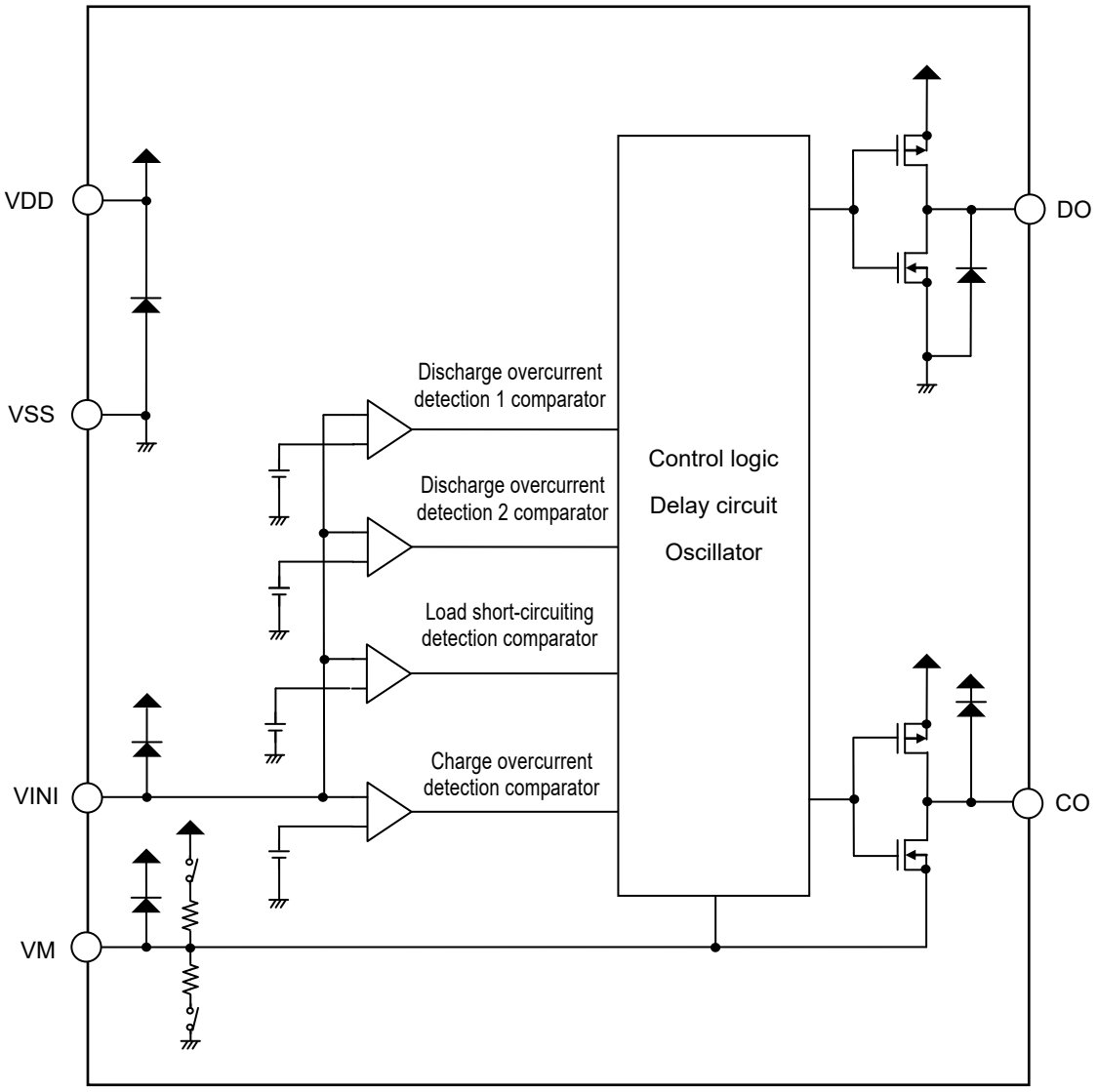


Figure 1

■ Product Name Structure

1. Product name

S-8269B xx - I6T1 U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications*1
I6T1: SNT-6A, Tape

Serial code*2
Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

Table 2

Product Name	Discharge Overcurrent Detection Voltage 1 [V_{DIOV1}]	Discharge Overcurrent Detection Voltage 2 [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]	Discharge Overcurrent Detection Delay Time1 [t_{DIOV1}]	Discharge Overcurrent Detection Delay Time2 [t_{DIOV2}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]	Release Voltage of Discharge Overcurrent Status*1, 2
S-8269BAA-I6T1U	0.0300 V	0.060 V	0.100 V	−0.0300 V	4.0 s	8 ms	280 µs	8 ms	V_{RIOV}
S-8269BAB-I6T1U	0.0600 V	0.080 V	0.100 V	−0.0150 V	512 ms	128 ms	530 µs	128 ms	V_{DIOV1}
S-8269BAC-I6T1U	0.0300 V	0.050 V	0.075 V	−0.0050 V	256 ms	8 ms	280 µs	128 ms	V_{DIOV1}
S-8269BAD-I6T1U	0.0350 V	0.055 V	0.100 V	−0.015 V	2.0 s	32 ms	280 µs	128 ms	V_{RIOV}

***1.** Release voltage of discharge overcurrent status: V_{DIOV1}, $V_{RIOV} = V_{DD} \times 0.8$ (typ.)
***2.** Refer to **Caution 3** of "**4. External components list**" in "**■ Examples of Application Circuit Added the Discharge Overcurrent Protection Function**" for details.

Remark Please contact our sales representatives for products other than the above.

Table 3

Delay Time	Symbol	Selection Range						Remark
Discharge overcurrent detection delay time 1	t_{DIOV1}	8 ms	16 ms	32 ms	64 ms	128 ms	256 ms	Select a value from the left.
		512 ms	1.0 s	2.0 s	3.0 s	3.75 s	4.0 s	
Discharge overcurrent detection delay time 2	t_{DIOV2}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.
Load short-circuiting detection delay time	t_{SHORT}	280 µs	530 µs	–	–	–	–	Select a value from the left.
Charge overcurrent detection delay time	t_{CIOV}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	Select a value from the left.

Remark The delay times can be changed within the range listed in **Table 3**. For details, please contact our sales representatives.

■ Pin Configuration

1. SNT-6A

Top view

Figure 2

Table 4

Pin No.	Symbol	Description
1	VM	Input pin for external negative voltage
2	CO	Connection pin of charge control FET gate (CMOS output)
3	DO	Connection pin of discharge control FET gate (CMOS output)
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	VINI	Overcurrent detection pin

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 6	V
VINI pin input voltage	V_{VINI}	VINI	V_{DD} – 6 to V_{DD} + 0.3	V
VM pin input voltage	V_{VM}	VM	V_{DD} – 28 to V_{DD} + 0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS} – 0.3 to V_{DD} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{DD} – 28 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SNT-6A	Board A	–	224	–	°C/W
			Board B	–	176	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Ta = +25°C

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Discharge overcurrent detection voltage 1	V_{DIOV1}	–	V_{DIOV1} – 0.0015	V_{DIOV1}	V_{DIOV1} + 0.0015	V	1
Discharge overcurrent detection voltage 2	V_{DIOV2}	–	V_{DIOV2} – 0.003	V_{DIOV2}	V_{DIOV2} + 0.003	V	1
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} – 0.005	V_{SHORT}	V_{SHORT} + 0.005	V	1
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.0015	V_{CIOV}	V_{CIOV} + 0.0015	V	1
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	V_{DD} × 0.77	V_{DD} × 0.80	V_{DD} × 0.83	V	1
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	500	1250	2500	kΩ	2
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.4 V, V_{VM} = 1.0 V	5	10	15	kΩ	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	2.0	4.0	μA	2
Output Resistance							
CO pin resistance "H"	R_{COH}	–	5	10	20	kΩ	3
CO pin resistance "L"	R_{COL}	–	5	10	20	kΩ	3
DO pin resistance "H"	R_{DOH}	–	5	10	20	kΩ	3
DO pin resistance "L"	R_{DOL}	–	1	2	4	kΩ	3
Delay Time							
Discharge overcurrent detection delay time 1	t_{DIOV1}	–	t_{DIOV1} × 0.75	t_{DIOV1}	t_{DIOV1} × 1.25	–	4
		Ta = –20°C to +60°C*1	t_{DIOV1} × 0.65	t_{DIOV1}	t_{DIOV1} × 1.35	–	4
Discharge overcurrent detection delay time 2	t_{DIOV2}	–	t_{DIOV2} × 0.7	t_{DIOV2}	t_{DIOV2} × 1.3	–	4
Load short-circuiting detection delay time	t_{SHORT}	–	t_{SHORT} × 0.7	t_{SHORT}	t_{SHORT} × 1.3	–	4
Charge overcurrent detection delay time	t_{CIOV}	–	t_{CIOV} × 0.7	t_{CIOV}	t_{CIOV} × 1.3	–	4

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

2. Ta = –40°C to +85°C*1

Table 8

(Ta = –40°C to +85°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Discharge overcurrent detection voltage 1	V_{DIOV1}	–	V_{DIOV1} – 0.002	V_{DIOV1}	V_{DIOV1} + 0.002	V	1
Discharge overcurrent detection voltage 2	V_{DIOV2}	–	V_{DIOV2} – 0.003	V_{DIOV2}	V_{DIOV2} + 0.003	V	1
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} – 0.005	V_{SHORT}	V_{SHORT} + 0.005	V	1
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.002	V_{CIOV}	V_{CIOV} + 0.002	V	1
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	V_{DD} × 0.77	V_{DD} × 0.80	V_{DD} × 0.83	V	1
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	250	1250	3500	kΩ	2
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.4 V, V_{VM} = 1.0 V	3.5	10	20	kΩ	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	2.0	5.0	μA	2
Output Resistance							
CO pin resistance "H"	R_{COH}	–	2.5	10	30	kΩ	3
CO pin resistance "L"	R_{COL}	–	2.5	10	30	kΩ	3
DO pin resistance "H"	R_{DOH}	–	2.5	10	30	kΩ	3
DO pin resistance "L"	R_{DOL}	–	0.5	2	6	kΩ	3
Delay Time							
Discharge overcurrent detection delay time 1	t_{DIOV1}	–	t_{DIOV1} × 0.4	t_{DIOV1}	t_{DIOV1} × 1.6	–	4
Discharge overcurrent detection delay time 2	t_{DIOV2}	–	t_{DIOV2} × 0.4	t_{DIOV2}	t_{DIOV2} × 1.6	–	4
Load short-circuiting detection delay time	t_{SHORT}	–	t_{SHORT} × 0.4	t_{SHORT}	t_{SHORT} × 1.6	–	4
Charge overcurrent detection delay time	t_{CIOV}	–	t_{CIOV} × 0.4	t_{CIOV}	t_{CIOV} × 1.6	–	4

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Discharge overcurrent detection voltage 1, discharge overcurrent release voltage (Test circuit 1)

1. 1 Release voltage of discharge overcurrent status "V_{DIOV1}"

Discharge overcurrent detection voltage 1 (V_{DIOV1}) is defined as the voltage V5 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent detection delay time 1 (t_{DIOV1}) when the voltage V5 is increased from the starting conditions of V1 = 3.4 V, V2 = 1.4 V, V5 = 0 V. V_{DO} goes from "L" to "H" when setting V2 = 3.4 V and when the voltage V2 is then gradually decreased to V_{DIOV1} typ. or lower.

1. 2 Release voltage of discharge overcurrent status "V_{RIOV}"

V_{DIOV1} is defined as the voltage V5 whose delay time for changing V_{DO} from "H" to "L" is t_{DIOV1} when the voltage V5 is increased from the starting conditions of V1 = 3.4 V, V2 = 1.4 V, V5 = 0 V. Discharge overcurrent release voltage (V_{RIOV}) is defined as the voltage V2 at which V_{DO} goes from "L" to "H" when setting V2 = 3.4 V and when the voltage V2 is then gradually decreased.

2. Discharge overcurrent detection voltage 2 (Test circuit 1)

Discharge overcurrent detection voltage 2 (V_{DIOV2}) is defined as the voltage V5 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent detection delay time 2 (t_{DIOV2}) when the voltage V5 is increased after setting V1 = 3.4 V, V2 = 1.4 V, V5 = 0 V.

3. Load short-circuiting detection voltage (Test circuit 1)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V5 whose delay time for changing V_{DO} from "H" to "L" is load short-circuiting detection delay time (t_{SHORT}) when the voltage V5 is increased after setting V1 = 3.4 V, V2 = 1.4 V, V5 = 0 V.

4. Charge overcurrent detection voltage (Test circuit 1)

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V5 whose delay time for changing V_{CO} from "H" to "L" is charge overcurrent detection delay time (t_{CIOV}) when the voltage V5 is decreased after setting V1 = 3.4 V, V2 = V5 = 0 V.

5. Current consumption during operation (Test circuit 2)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) after setting V1 = 3.4 V, V2 = V5 = 0 V.

6. Resistance between VDD pin and VM pin (Test circuit 2)

R_{VMD} is the resistance between VDD pin and VM pin under the set conditions of V1 = 1.8 V, V2 = V5 = 0 V.

7. Resistance between VM pin and VSS pin (Test circuit 2)

R_{VMS} is the resistance between VM pin and VSS pin when the voltage V5 is decreased to 0 V after setting V1 = 3.4 V, V2 = V5 = 1.0 V.

8. CO pin resistance "H"
(Test circuit 3)

The CO pin resistance "H" (R_{COH}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V, V3 = 3.0 V.

9. CO pin resistance "L"
(Test circuit 3)

The CO pin resistance "L" (R_{COL}) is the resistance between VM pin and CO pin under the set conditions of V1 = 4.7 V, V2 = V5 = 0 V, V3 = 0.4 V.

10. DO pin resistance "H"
(Test circuit 3)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V, V4 = 3.0 V.

11. DO pin resistance "L"
(Test circuit 3)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V2 = V5 = 0 V, V4 = 0.4 V.

12. Discharge overcurrent detection delay time 1
(Test circuit 4)

Increase the voltage V5 after setting V1 = 3.4 V, V2 = 1.4 V, V5 = 0 V. The discharge overcurrent detection delay time 1 (t_{DIOV1}) is the time period from when the voltage V5 exceeds V_{DIOV1} until V_{DO} goes to "L".

13. Discharge overcurrent detection delay time 2
(Test circuit 4)

Increase the voltage V5 after setting V1 = 3.4 V, V2 = 1.4 V, V5 = 0 V. The discharge overcurrent detection delay time 2 (t_{DIOV2}) is the time period from when the voltage V5 exceeds V_{DIOV2} until V_{DO} goes to "L".

14. Load short-circuiting detection delay time
(Test circuit 4)

Increase the voltage V5 after setting V1 = 3.4 V, V2 = 1.4 V, V5 = 0 V. The load short-circuiting detection delay time (t_{SHORT}) is the time period from when the voltage V5 exceeds V_{SHORT} until V_{DO} goes to "L".

15. Charge overcurrent detection delay time
(Test circuit 4)

Decrease the voltage V5 after setting V1 = 3.4 V, V2 = V5 = 0 V. The charge overcurrent detection delay time (t_{CIOV}) is the time period from when the voltage V5 falls below V_{CIOV} until V_{CO} goes to "L".

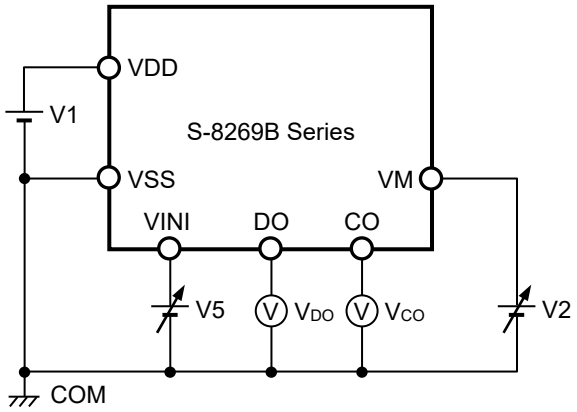


Figure 3 Test Circuit 1

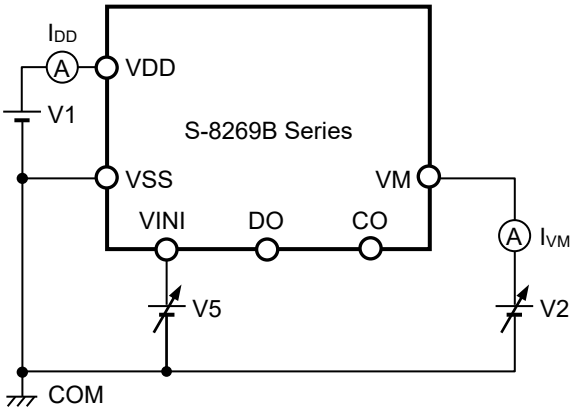


Figure 4 Test Circuit 2

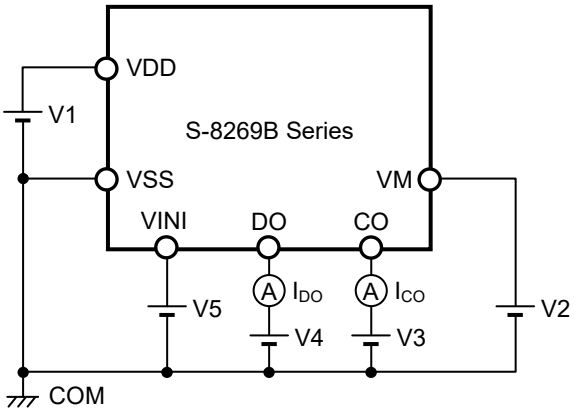


Figure 5 Test Circuit 3

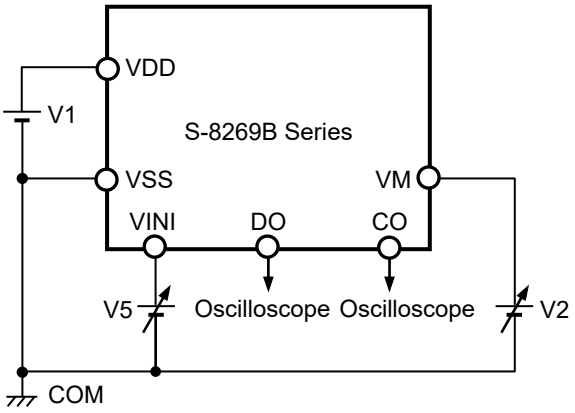


Figure 6 Test Circuit 4

■ Operation

Remark Refer to "**Examples of Application Circuit Added the Discharge Overcurrent Protection Function**".

1. Normal status

The S-8269B Series monitors the voltage between VINI pin and VSS pin to control charging and discharging. When the VINI pin voltage is in the range from charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent detection voltage 1 (V_{DIOV1}), the S-8269B Series turns both the charge and discharge control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.
The resistance between VDD pin and VM pin (R_{VMD}), and the resistance between VM pin and VSS pin (R_{VMS}) are not connected in the normal status.

Caution After the battery is connected, discharging may not be carried out. In this case, the S-8269B Series returns to the normal status by connecting a charger.

2. Discharge overcurrent status (discharge overcurrent 1, discharge overcurrent 2, load short-circuiting)

When a battery in the normal status is in the status where the VINI pin voltage is equal to or higher than V_{DIOV1} because the discharge current is equal to or higher than the specified value and the status lasts for the discharge overcurrent detection delay time 1 (t_{DIOV1}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

2. 1 Release voltage of discharge overcurrent status "V_{DIOV1}"

Under the discharge overcurrent status, VM pin and VSS pin are shorted by R_{VMS} in the S-8269B Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, VM pin voltage returns to the VSS pin voltage. When the VM pin voltage returns to V_{DIOV1} or lower, the S-8269B Series releases the discharge overcurrent status.
R_{VMD} is not connected in the discharge overcurrent status.

2. 2 Release voltage of discharge overcurrent status "V_{RIOV}"

Under the discharge overcurrent status, VM pin and VSS pin are shorted by R_{VMS} in the S-8269B Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, VM pin voltage returns to the VSS pin voltage. When the VM pin voltage returns to V_{RIOV} or lower, the S-8269B Series releases the discharge overcurrent status.
R_{VMD} is not connected in the discharge overcurrent status.

3. Charge overcurrent status

When a battery in the normal status is in the status where the VINI pin voltage is equal to or lower than V_{CIOV} because the charge current is equal to or higher than the specified value and the status lasts for the charge overcurrent detection delay time (t_{CIOV}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.
The S-8269B Series releases the charge overcurrent status when the discharge current flows and the VM pin voltage is 0.35 V typ. or higher by removing the charger.

Under the charge overcurrent status, VDD pin and VM pin are shorted by R_{VMD} in the S-8269B Series. The VM pin is pulled up by R_{VMD}.
R_{VMS} is not connected in the charge overcurrent status.

4. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV1}, t_{DIOV2} and t_{SHORT} start when V_{DIOV1} is detected. When V_{DIOV2} or V_{SHORT} is detected over t_{DIOV2} or t_{SHORT} after the detection of V_{DIOV1}, the S-8269B Series turns the discharge control FET off within t_{DIOV2} or t_{SHORT} of each detection.

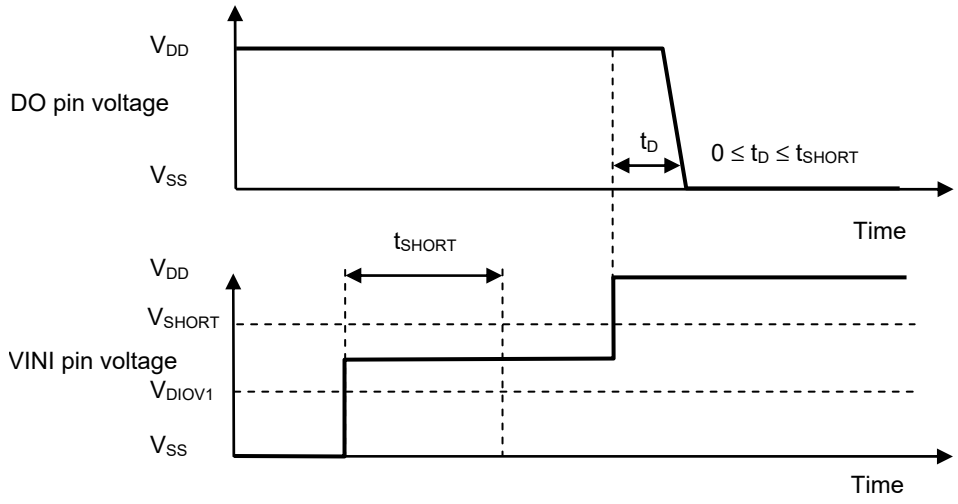
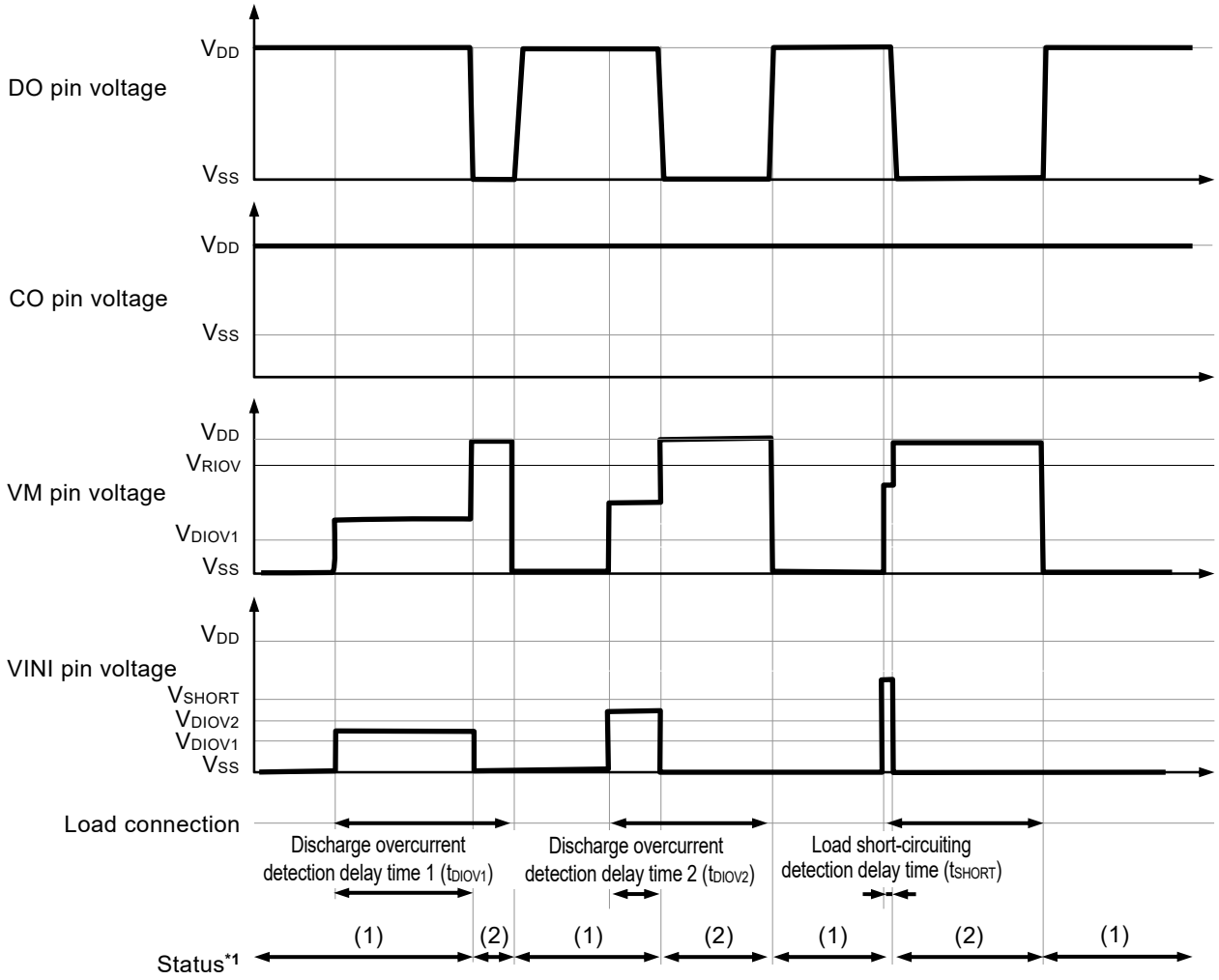


Figure 7

■ Timing Charts

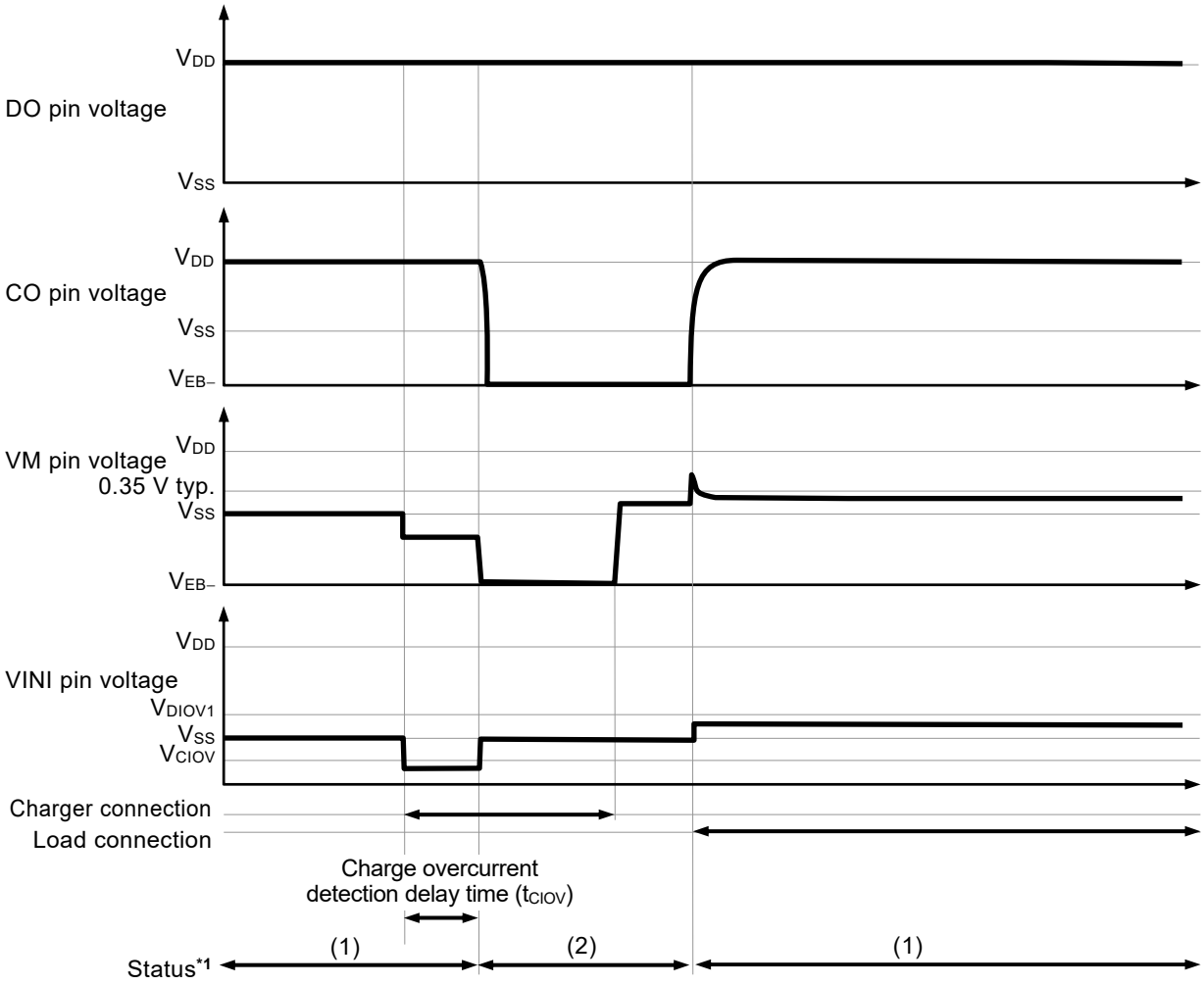
1. Discharge overcurrent detection



***1.** (1): Normal status
(2): Discharge overcurrent status

Figure 8

2. Charge overcurrent detection

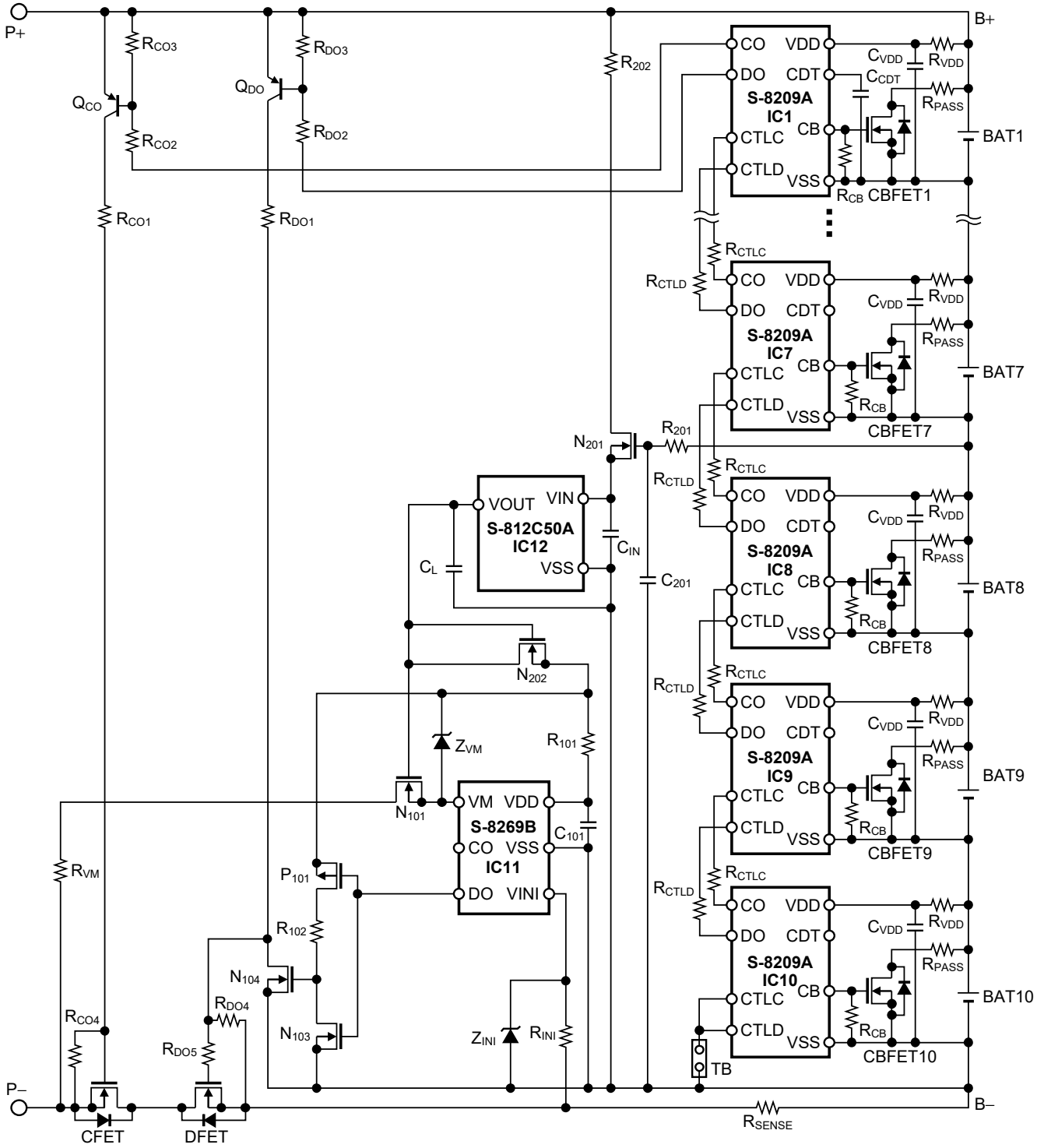


***1.** (1): Normal status
(2): Charge overcurrent status

Figure 9

■ Examples of Application Circuit Added the Discharge Overcurrent Protection Function

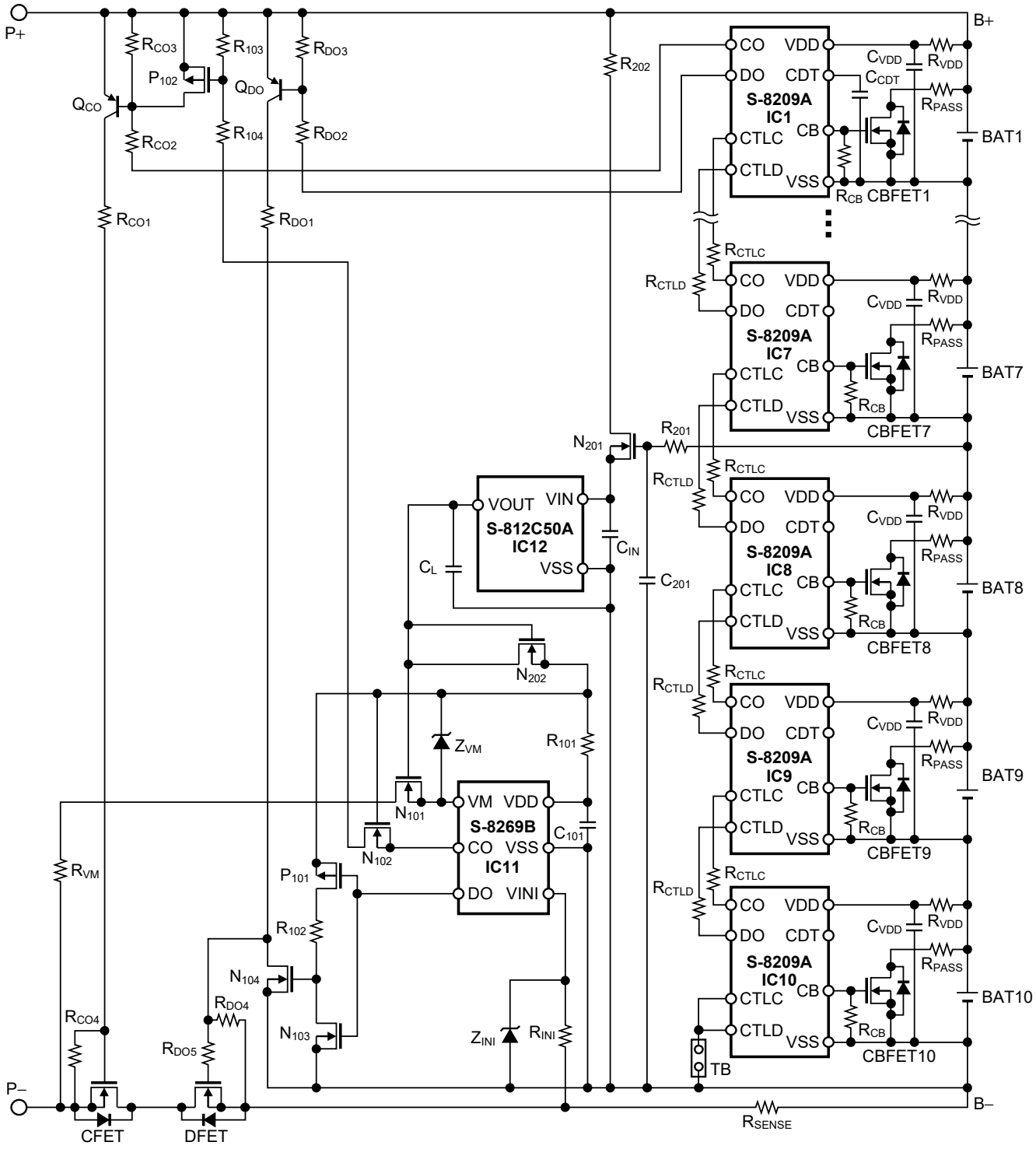
1. 10-serial cell protection circuit added the discharge overcurrent protection function (Charge pin and discharge pin are integrated, S-8269B Series)



Remark Refer to "**4. External components list**" for constants of external components.

Figure 10

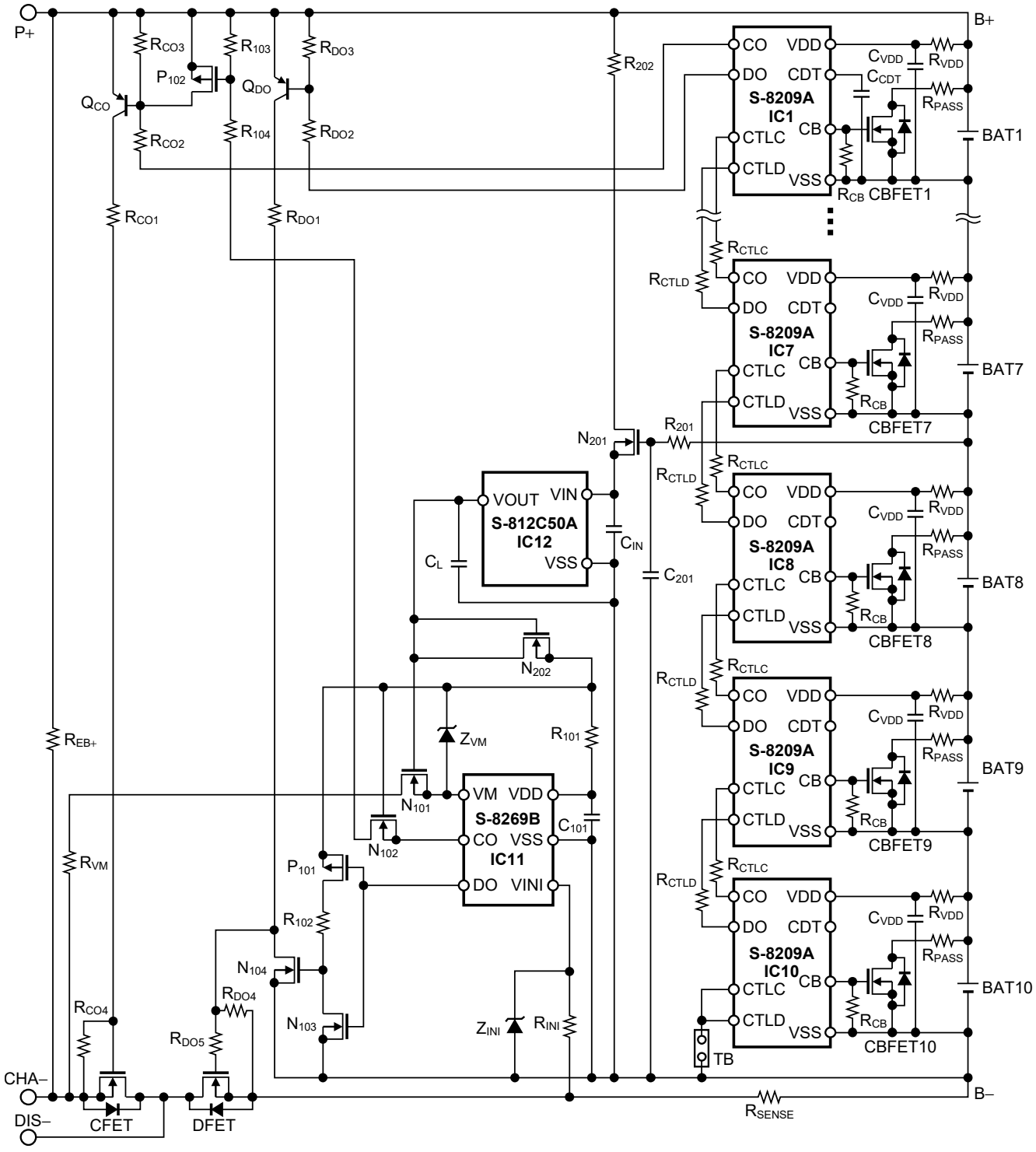
2. 10-serial cell protection circuit added the charge and discharge overcurrent protection functions (Charge pin and discharge pin are integrated, S-8269B Series)



Remark Refer to "**4. External components list**" for constants of external components.

Figure 11

3. 10-serial cell protection circuit added the charge and discharge overcurrent protection functions (Charge pin and discharge pin are separated, S-8269B Series)



Remark Refer to "**4. External components list**" for constants of external components.

Figure 12

4. External components list

Table 9 shows external components used in the connection examples in **Figure 10** to **Figure 12**.

Table 9

Symbol	Typical	Unit	Components name	Maker	Remark
IC1 to IC10	–	–	S-8209A	ABLIC Inc.	Necessary
IC11	–	–	S-8269B*1	ABLIC Inc.	Necessary
IC12	–	–	S-812C50A	ABLIC Inc.	Necessary
CBFET1 to CBFET10	–	–	–	–	User setting
CFET	–	–	–	–	User setting
DFET	–	–	–	–	User setting
C_{CDT}	–	–	–	–	User setting
C_{IN}	0.1	μF	GRM188	Murata Manufacturing Co., Ltd.	User setting
C_L	0.1	μF	GRM188	Murata Manufacturing Co., Ltd.	User setting
C_{VDD}	0.1	μF	GRM188	Murata Manufacturing Co., Ltd.	Recommended
C_{101}	0.1	μF	–	–	Recommended
C_{201}*2	1	μF	–	–	Recommended
N_{101}	–	–	SSM3K7002KF	Toshiba Electronic Devices & Storage Corporation	Recommended
N_{102}	–	–	SSM3K7002KF	Toshiba Electronic Devices & Storage Corporation	Recommended
N_{103}	–	–	SSM3K7002KF	Toshiba Electronic Devices & Storage Corporation	Recommended
N_{104}	–	–	SSM3K7002KF	Toshiba Electronic Devices & Storage Corporation	Recommended
N_{201}	–	–	SSM3K7002KF	Toshiba Electronic Devices & Storage Corporation	Recommended
N_{202}	–	–	SSM3K7002KF	Toshiba Electronic Devices & Storage Corporation	Recommended
P_{101}	–	–	SSM3J168F	Toshiba Electronic Devices & Storage Corporation	Recommended
P_{102}	–	–	SSM3J168F	Toshiba Electronic Devices & Storage Corporation	Recommended
Q_{CO}	PNP	–	2SB1198K	ROHM CO., LTD.	Recommended
Q_{DO}	PNP	–	2SB1198K	ROHM CO., LTD.	Recommended
R_{CB}	10	MΩ	MCR03	ROHM CO., LTD.	Recommended
R_{CO1}*3	–	–	–	–	User setting
R_{CO2}	510	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{CO3}	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R_{CO4}	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R_{CTLC}*4	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{CTLD}*4	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{DO1}*3	–	–	–	–	User setting
R_{DO2}	510	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{DO3}	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R_{DO4}	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R_{DO5}	–	–	–	–	User setting
R_{EB+}	10	MΩ	MCR03	ROHM CO., LTD.	Recommended
R_{INI}	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{PASS}*5	–	–	–	–	User setting
R_{SENSE}*5	–	–	–	–	User setting
R_{VDD}	470	Ω	MCR03	ROHM CO., LTD.	Recommended
R_{VM}	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{101}	470	Ω	MCR03	ROHM CO., LTD.	Recommended
R_{102}	5.1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{103}	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R_{104}	510	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{201}*2	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R_{202}	100	Ω	MCR03	ROHM CO., LTD.	Recommended
TB*6	–	–	–	–	User setting
Z_{INI}	–	–	UFZV3.6B	ROHM CO., LTD.	Recommended
Z_{VM}*7	–	–	1SMB5930B	Diodes Incorporated	User setting

***1.** Select this product according to the overcurrent detection voltage that you will use.

***2.** At the moment when the S-8269B Series detects the overcurrent and turns off DFET, a spike voltage generated in BAT8 may result in transient change of the power supply of the S-8269B Series through N_{201} and cause the S-8269B Series to malfunction for overcurrent detection. This phenomenon can be prevented by setting C_{201} and R_{201}.
The constant of C_{201} and R_{201} is normally 1 $\mu F \times 1\ k\Omega$ = 1 $mF \times \Omega$. However, since the spike voltage generated in BAT8 differs depending on each application, perform thorough evaluation about the power supply transient change and overcurrent protection function of the S-8269B Series using the actual application to set C_{201} and R_{201}.

***3.** Set the resistance with attention to VGS rated value of FET.

***4.** In order to prevent from damage when an overvoltage is applied to the IC, select R_{CTLC} and R_{CTLD} from 1 kΩ to 100 kΩ.

***5.** Pay attention to the rated electric powers.

***6.** TB: Thermal Breaker
When a TB is not necessary, connect the same protection resistor as R_{CTLC} or R_{CTLD}.

***7.** When building a protection circuit for 10-serial or more cells, connect Z_{VM} so that the VM pin voltage does not exceed the absolute maximum rating.

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

3. Set V_{VM} as follows to release the S-8269B Series from the discharge overcurrent status when a load is open.

- **"1. 10-serial cell protection circuit added the discharge overcurrent protection function (Charge pin and discharge pin are integrated, S-8269B Series)" or "2. 10-serial cell protection circuit added the charge and discharge overcurrent protection functions (Charge pin and discharge pin are integrated, S-8269B Series)"**

$$V_{VM} = V_{P+} \times \frac{R_{VMS}}{R_{CO1} + R_{CO4} + R_{VM} + R_{VMS}} \leq V_{RIOV} \text{ or } V_{DIOV1}$$

- **"3. 10-serial cell protection circuit added the charge and discharge overcurrent protection functions (Charge pin and discharge pin are separated, S-8269B Series)"**

$$V_{VM} = V_{P+} \times \frac{R_{VMS}}{\dfrac{R_{EB+} \times (R_{CO1} + R_{CO4})}{R_{EB+} + R_{CO1} + R_{CO4}} + R_{VM} + R_{VMS}} \leq V_{RIOV} \text{ or } V_{DIOV1}$$

Remark V_{P+}: P+ pin voltage

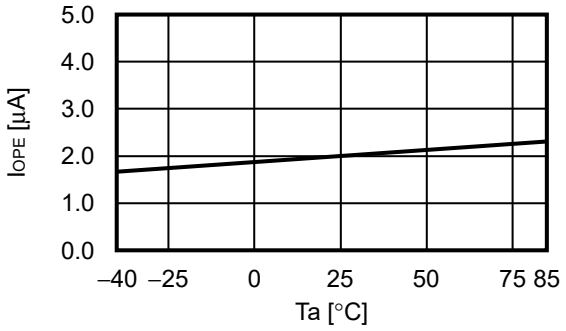
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

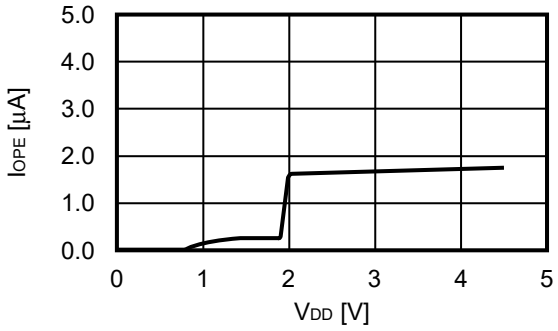
■ Characteristics (Typical Data)

1. Current consumption

1. 1 I_{OPE} vs. Ta

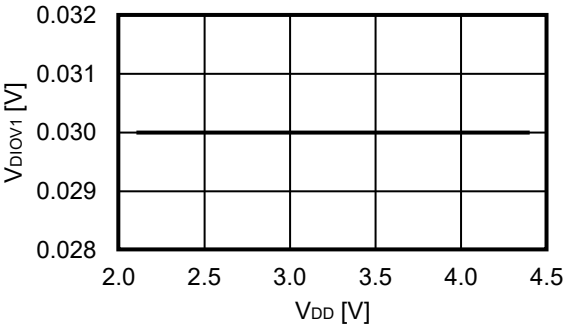


1. 2 I_{OPE} vs. V_{DD}

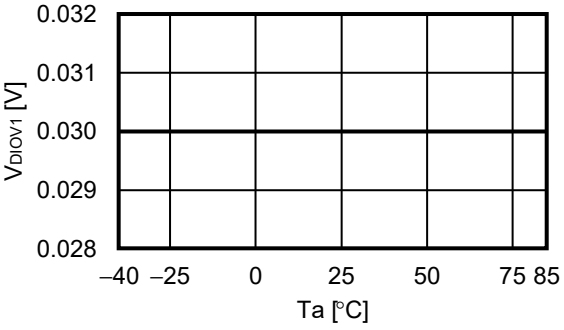


2. Detection voltage

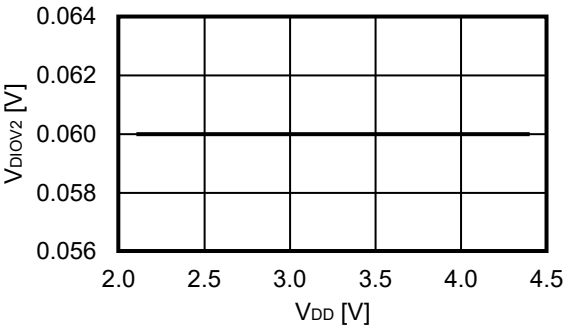
2. 1 V_{DIOV1} vs. V_{DD}



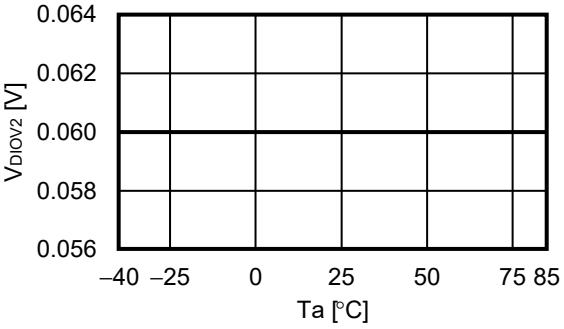
2. 2 V_{DIOV1} vs. Ta



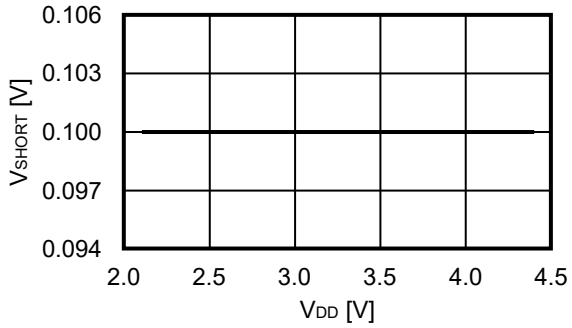
2. 3 V_{DIOV2} vs. V_{DD}



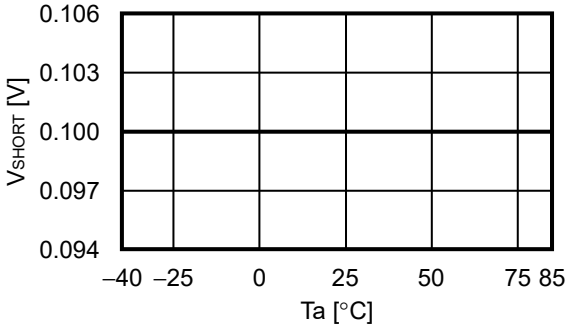
2. 4 V_{DIOV2} vs. Ta



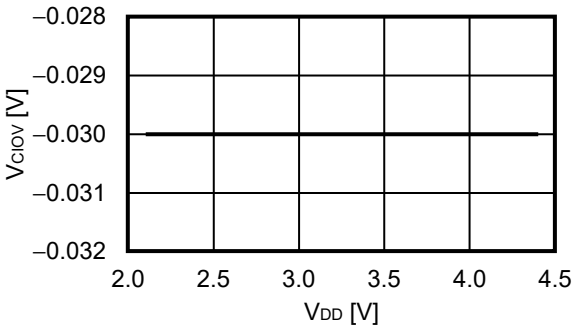
2. 5 V_{SHORT} vs. V_{DD}



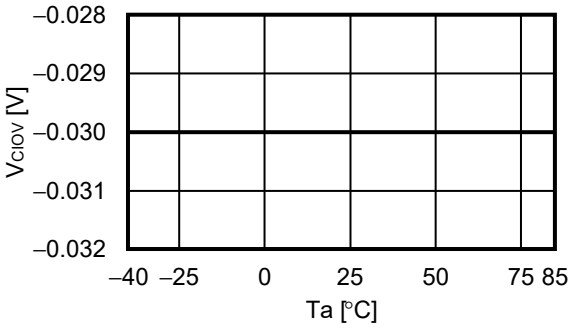
2. 6 V_{SHORT} vs. Ta



2. 7 V_{CIOV} vs. V_{DD}

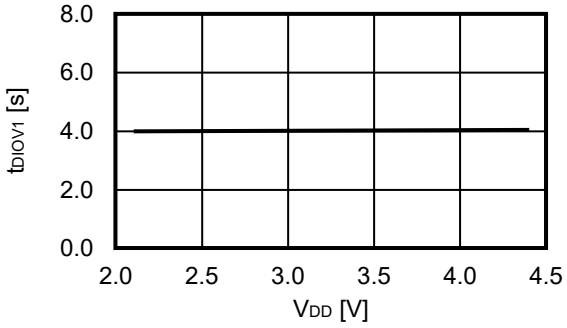


2. 8 V_{CIOV} vs. Ta

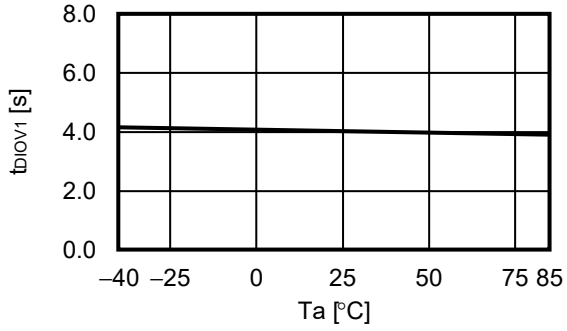


3. Delay time

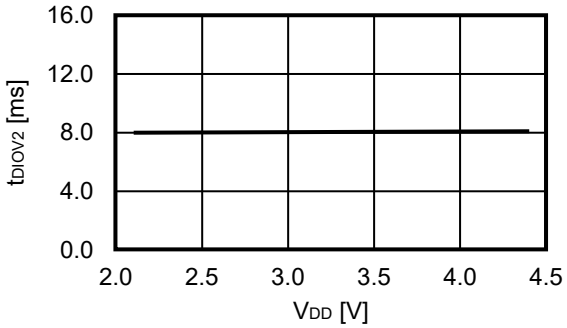
3. 1 t_{DIOV1} vs. V_{DD}



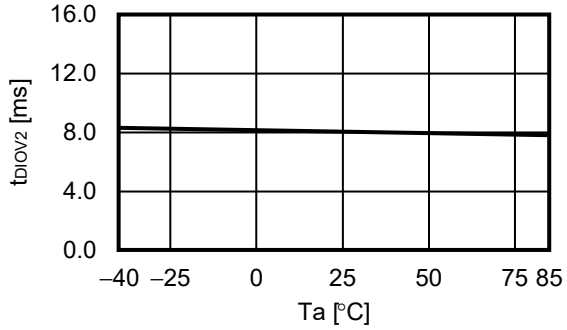
3. 2 t_{DIOV1} vs. Ta



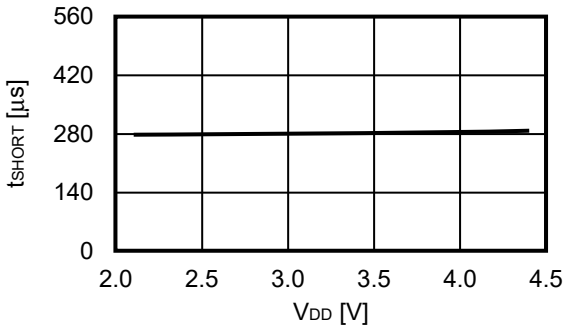
3. 3 t_{DIOV2} vs. V_{DD}



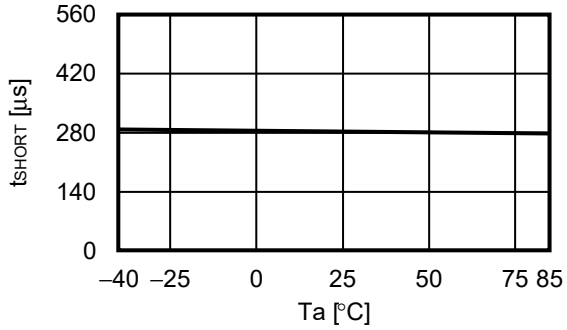
3. 4 t_{DIOV2} vs. Ta



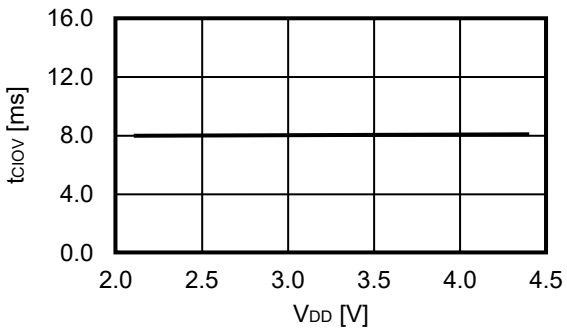
3. 5 t_{SHORT} vs. V_{DD}



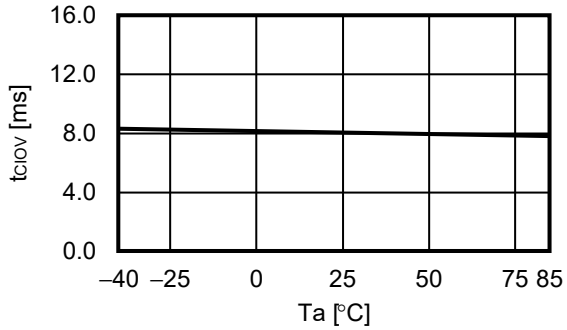
3. 6 t_{SHORT} vs. Ta



3. 7 t_{CIOV} vs. V_{DD}

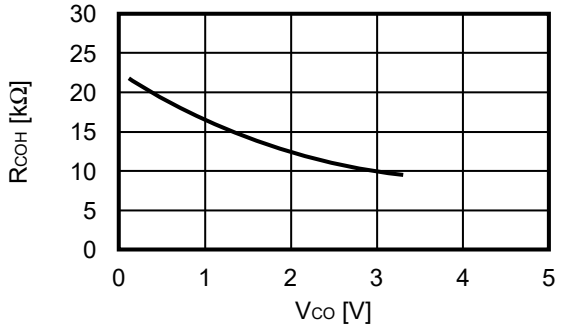


3. 8 t_{CIOV} vs. Ta

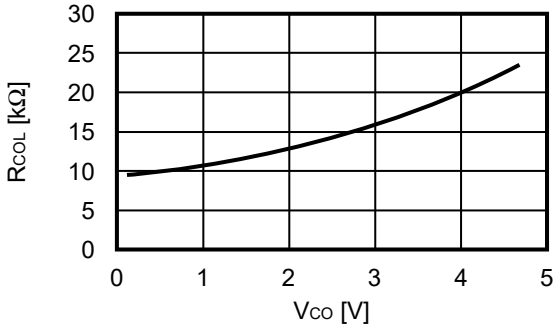


4. Output resistance

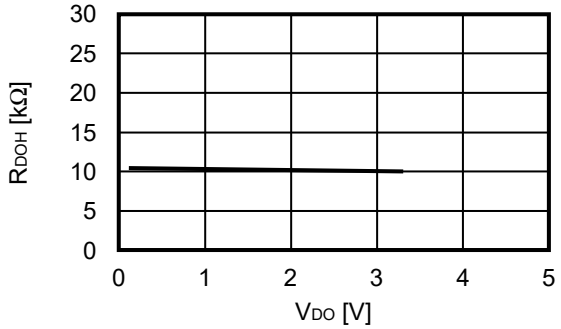
4. 1 R_{COH} vs. V_{CO}



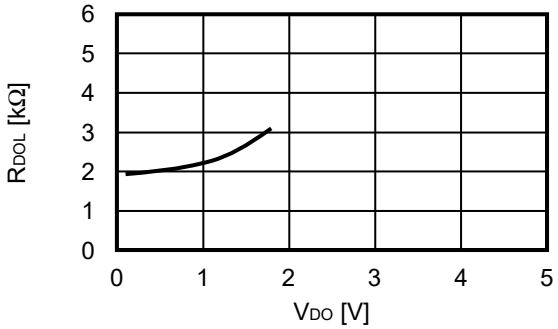
4. 2 R_{COL} vs. V_{CO}



4. 3 R_{DOH} vs. V_{DO}



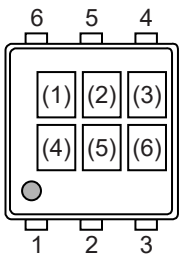
4. 4 R_{DOL} vs. V_{DO}



■ Marking Specifications

1. SNT-6A

Top view



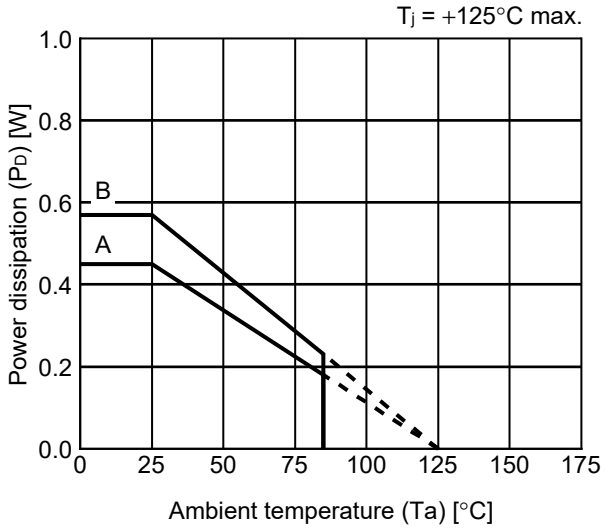
(1) to (3): Product code (refer to **Product name vs. Product code**)
(4) to (6): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8269BAA-I6T1U	7	8	A
S-8269BAB-I6T1U	7	8	B
S-8269BAC-I6T1U	7	8	C
S-8269BAD-I6T1U	7	8	D

■ Power Dissipation

SNT-6A

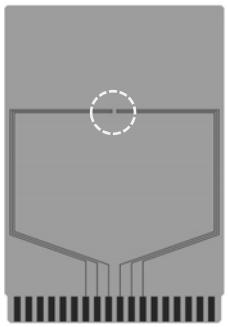


Board	Power Dissipation (P_D)
A	0.45 W
B	0.57 W
C	–
D	–
E	–

SNT-6A Test Board

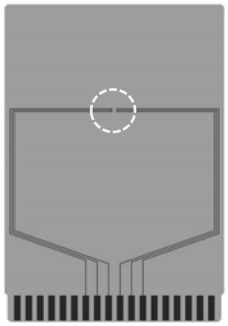
(1) Board A

IC Mount Area



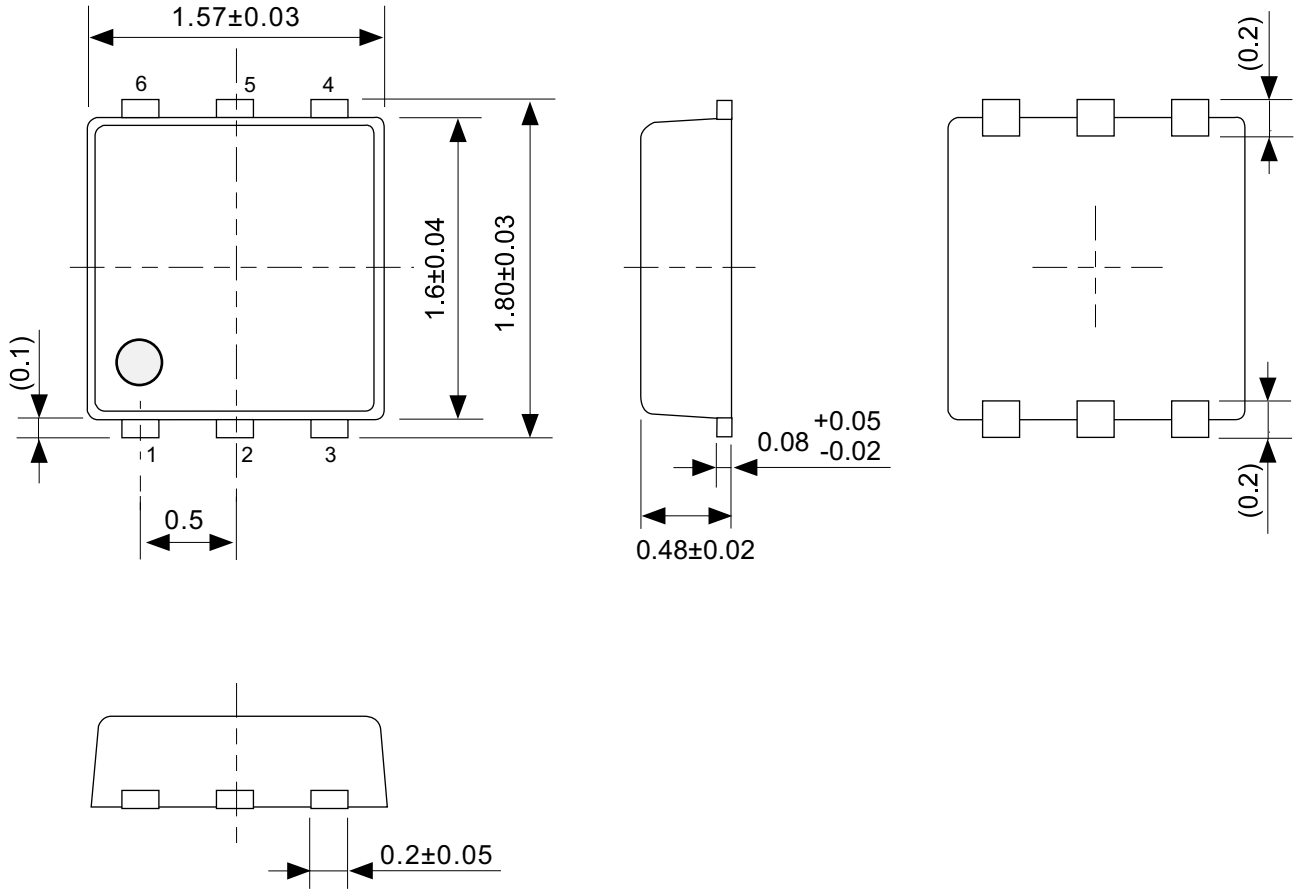
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



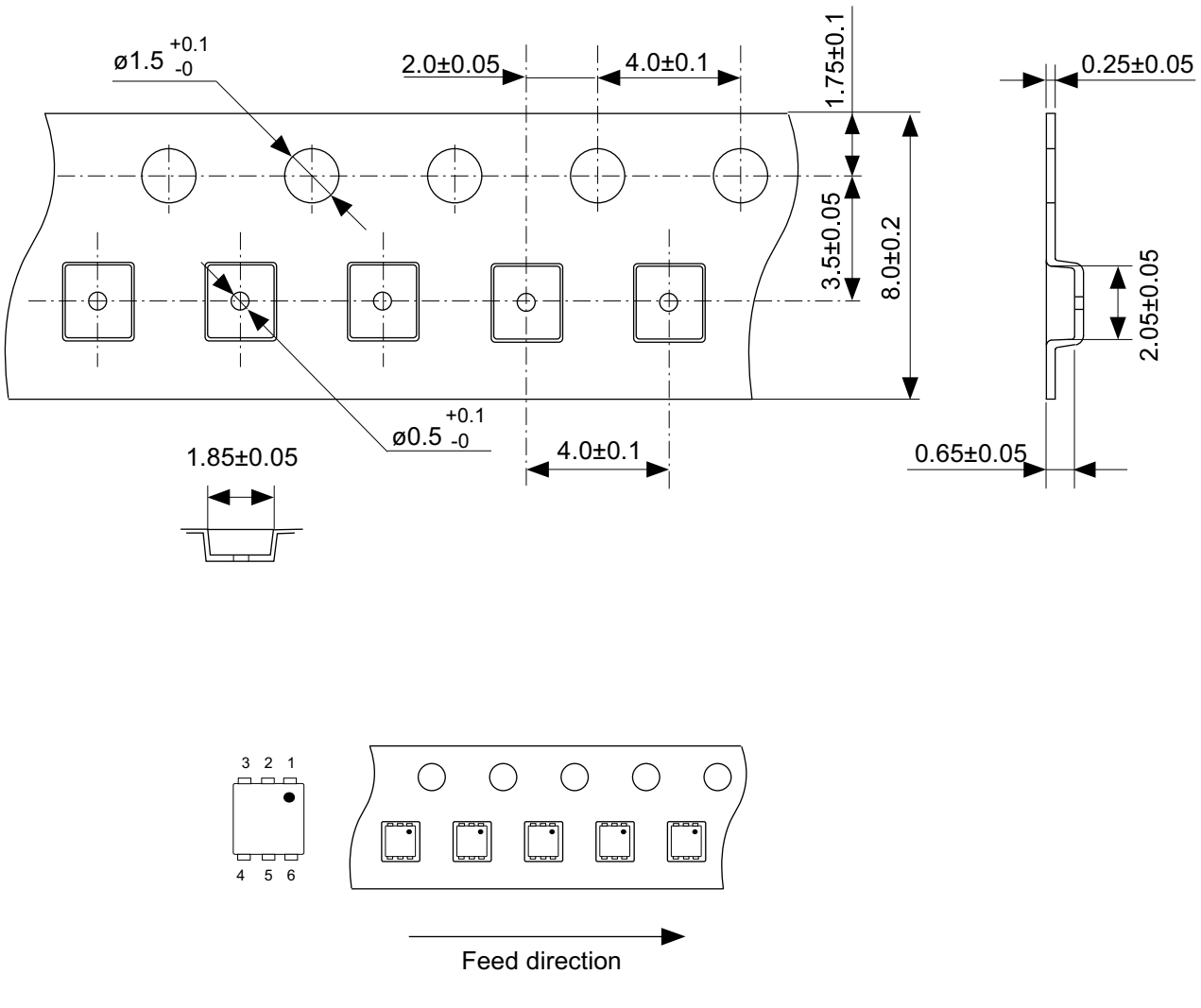
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SNT6A-A-Board-SD-1.0



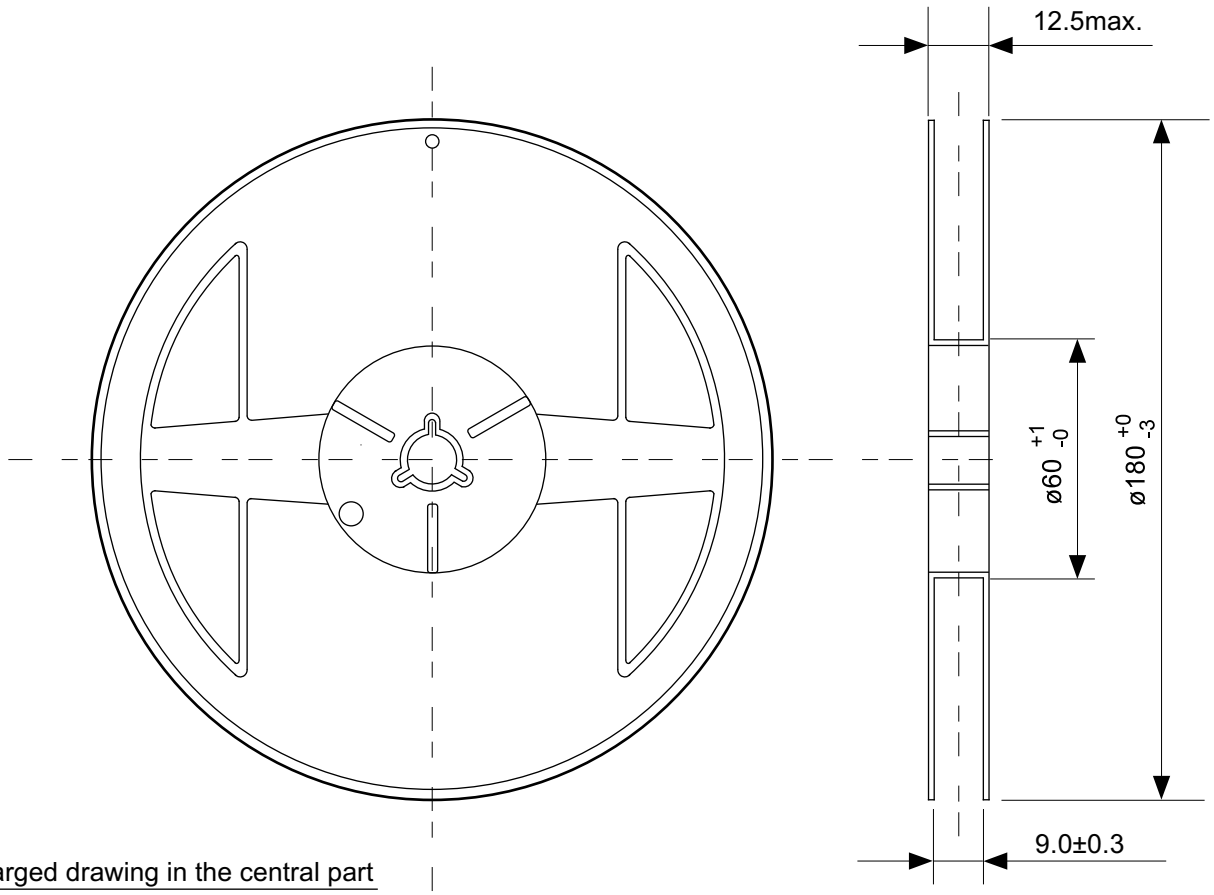
No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

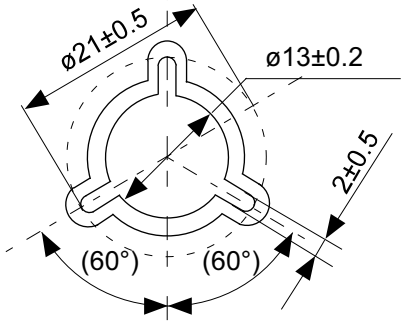


No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

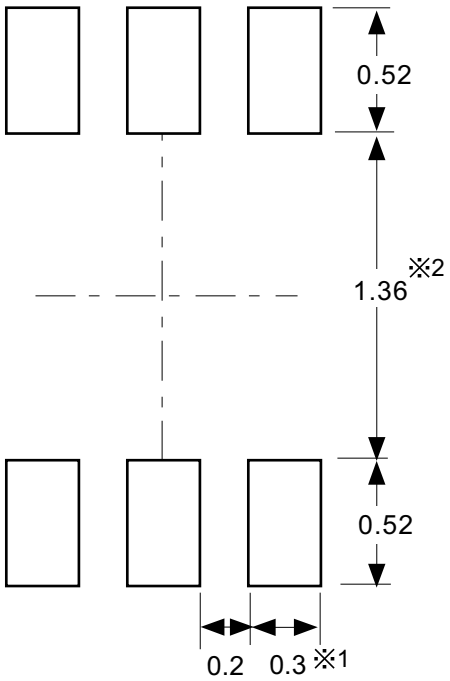


Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝**SNT**パッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07