

# MAX14657/MAX14658/ MAX14659

## Dual-Channel USB Host Adapter Emulators

### General Description

The MAX14657/MAX14658/MAX14659 are next-generation dual-channel USB 2.0 host-charger adapter emulators that combine USB Hi-Speed analog switches with a USB adapter emulator circuit.

The MAX14657 features an I<sup>2</sup>C interface to fully configure the charging behavior with different address options. The MAX14658/MAX14659 are controlled by two GPIO inputs (CB1\_/CB0\_) and support USB data and automatic charger mode. In charging downstream port (CDP) mode, the devices emulate the CDP function while supporting normal USB traffic. The MAX14657/MAX14658 have a CEN\_ output for an active-high CLS enable input, and the MAX14659 has a  $\overline{\text{CEN}}$  output for an active-low CLS enable input to restart the peripheral connected to the USB host.

The MAX14658/MAX14659 feature 2A high-current autodetect mode. The MAX14657 can be configured through I<sup>2</sup>C to support various dedicated charger modes such as Apple 1A/2A forced, or Apple or Samsung 1A/2A autodetect modes.

The MAX14657/MAX14658/MAX14659 support CDP and standard downstream port (SDP) charging while in the active state (S0), and support the dedicated charging port (DCP) charging while in the standby state (S3/S4/S5). All of the devices support low-speed remote wake-up by monitoring DM\_, and also support remote wakeup in sleep mode (S3).

The MAX14657/MAX14658/MAX14659 are available in a 16-pin (3mm x 3mm) TQFN-EP package and are specified over the -40°C to +85°C extended temperature range.

### Applications

- Laptop/Desktop Computers
- USB Hubs
- Universal Chargers Including iPod®/iPhone®/iPad®

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**Ordering Information and Typical Operating Circuit appear at end of data sheet.**

For related parts and recommended products to use with this part, refer to [www.maximintegrated.com/MAX14657.related](http://www.maximintegrated.com/MAX14657.related).

### Benefits and Features

- Integrated Dual Channels
  - More Convenient, High-Current USB Charging Ports for Users
  - Simple and Flexible Power-Management Control
  - Small TQFN Package Minimizes PCB Area
- Improved Charger Interoperability
  - USB (CDP) Emulation with Smart CDP and Fool-Proof CDP
  - Enhanced Automodes
  - Foolproof CDP
  - Meets New USB Battery Charging (BC) Revision 1.2 Specification
  - Backward Compatible with Previous USB BC Revisions
  - Meets China YD/T1591-2009 Charging Specification
  - Supports Standby-Mode Charging for USB BC Revision 1.2 Compatible Devices
- Provide Greater Application Flexibility
  - I<sup>2</sup>C Controls Multiple Modes (MAX14657)
  - A Slave Address Selection Input Offers Two Possible Slave Addresses for Each Emulator (MAX14657)
  - CB0\_ and CB1\_ Pins Control Multiple Automatic and Manual Charger States (MAX14658, MAX14659)
- Enhance Performance with High Level of Integrated Features
  - Supports Remote Wake-Up
  - Low-Capacitance USB 2.0 Hi-Speed Switch to Change Charging Modes
  - Automatic Current-Limit Switch Control
  - ±15kV ESD Protection on DP\_/DM\_

### Selector Guide

PART NUMBER	I/O MODE	CEN POLARITY	REMOTE WAKE-UP IN AM
MAX14657	I <sup>2</sup> C	Programmable (CEN default)	Programmable
MAX14658	GPIO	CEN	Yes
MAX14659	GPIO	$\overline{\text{CEN}}$	Yes



### Absolute Maximum Ratings

(All voltages referenced to GND.)

$V_{CC}$ , TDP\_, TDM\_, DP\_, DM\_, SDA,  
SCL, CB0\_, CB1\_, CEN\_,  $\overline{CEN}$ \_, SAS,  $\overline{INT}$  ..... -0.3V to +6V  
Continuous Current into Any Terminal .....  $\pm 30$ mA  
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
TQFN (derate 20.8mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 1666.7mW

Operating Temperature Range .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
Junction Temperature .....  $+150^\circ\text{C}$   
Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
Lead Temperature (soldering, 10s) .....  $+300^\circ\text{C}$   
Soldering Temperature (reflow) .....  $+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Package Thermal Characteristics (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....  $48^\circ\text{C}/\text{W}$   
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) .....  $10^\circ\text{C}/\text{W}$

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### Electrical Characteristics

( $V_{CC} = 3.0\text{V}$  to  $5.5\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0\text{V}$  and  $T_A = +25^\circ\text{C}$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
$V_{CC}$ Supply Voltage	$V_{CC}$	MAX14658 MAX14659 CB0_ = high/CB1_ = low (PM mode) CB0_ = low/CB1_ = high (FM mode)	3.0		5.5	V
		MAX14657 MODE_SEL[2:0] = 001 (PM mode) MODE_SEL[2:0] = 010 (FM mode)				
		MAX14658 MAX14659 CB0_ = low/CB1_ = low (AM2 mode) CB0_ = high/CB1_ = high (CM mode) (Note 3)	4.75		5.25	
		MAX14657 MODE_SEL[2:0] = XXX except: MODE_SEL[2:0] = 001 (PM mode) MODE_SEL[2:0] = 010 (FM mode) (Note 3)				

**Electrical Characteristics (continued)**

(V<sub>CC</sub> = 3.0V to 5.5V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +5.0V and T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V <sub>CC</sub> Supply Current	I <sub>CC</sub>	MAX14658 MAX14659	CB1_ = CB0_ = low (AM2 mode)		120	μA
			CB1_ = CB0_ = high (CM mode)		150	
			CB1_ = low/CB0_ = high (PM mode)		25	
		MAX14657	MODE_SEL[2:0] = 000 (AM2 mode)		120	
			MODE_SEL[2:0] = 011 (CM mode)		150	
			MODE_SEL[2:0] = 001 (PM mode)		25	
POR Delay	t <sub>POR</sub>			50		ms
<b>ANALOG SWITCHES (DP_, DM_, TDP_, TDM_)</b>						
Analog Signal Range	V <sub>DP</sub> , V <sub>DM</sub>	(Note 4)	0		V <sub>CC</sub>	V
TDP_/TDM_ On-Resistance	R <sub>ON</sub>	V <sub>CC</sub> = 3V, V <sub>IN</sub> = 0V, V <sub>CC</sub> , I <sub>IN</sub> = 10mA		3.5	6.5	Ω
TDP_/TDM_ On-Resistance Matching Between Channels	ΔR <sub>ON</sub>	V <sub>CC</sub> = 3V, V <sub>IN</sub> = 0V, V <sub>CC</sub> , I <sub>IN</sub> = 10mA		0.1		Ω
TDP_/TDM_ On-Resistance Flatness	R <sub>FLAT</sub>	V <sub>CC</sub> = 3V, V <sub>IN</sub> = 0V, V <sub>CC</sub> , I <sub>IN</sub> = 10mA		0.1		Ω
DP_/DM_ Short On-Resistance	R <sub>SHORT</sub>	V <sub>DP</sub> = 1V, R <sub>L</sub> = 20kΩ on DM_		70	130	Ω
Off-Leakage Current	I <sub>COM(OFF)</sub>	V <sub>CC</sub> = 3.6V, V <sub>DP</sub> = V <sub>DM</sub> = 0.3V, 3.3V; V <sub>TDP_</sub> = V <sub>TDM_</sub> = 0.3V, 3.3V	-1000		+1000	nA
On-Leakage Current	I <sub>COM(ON)</sub>	V <sub>CC</sub> = 3.6V, V <sub>DP_</sub> = V <sub>DM_</sub> = 0.3V, 3.3V	-1000	90	+1000	nA
<b>DYNAMIC PERFORMANCE</b>						
Turn-On Time	t <sub>ON</sub>	V <sub>TDP_</sub> or V <sub>TDM_</sub> = 1.5V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 1		10		μs
Turn-Off Time	t <sub>OFF</sub>	V <sub>TDP_</sub> or V <sub>TDM_</sub> = 1.5V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 1		10		μs
TDP_/TDM_ Propagation Delay	t <sub>PHL</sub> , t <sub>PLH</sub>	R <sub>L</sub> = R <sub>S</sub> = 50Ω, DP_ and DM_ connected to TDP_ and TDM_, Figure 2		60		ps
DP_/DM_ Output Skew	t <sub>SKEW</sub>	R <sub>L</sub> = R <sub>S</sub> = 50Ω, DP_ and DM_ connected to TDP_ and TDM_, Figure 2		40		ps
DP_/DM On-Capacitance (Connected to TDP_, TDM_)	C <sub>ON</sub>	f = 240MHz, V <sub>BIAS</sub> = 0V, V <sub>IN</sub> = 500mV <sub>P-P</sub>		5		pF
Bandwidth	BW	R <sub>L</sub> = R <sub>S</sub> = 50Ω, Figure 3		1000		MHz
Off-Isolation	V <sub>ISO</sub>	V <sub>IN</sub> = 0dBm, R <sub>L</sub> = R <sub>S</sub> = 50Ω, f = 250MHz, Figure 3		-20		dB
Crosstalk	V <sub>CT</sub>	V <sub>IN</sub> = 0dBm, R <sub>L</sub> = R <sub>S</sub> = 50Ω, f = 250MHz, Figure 3		-25		dB

### Electrical Characteristics (continued)

( $V_{CC} = 3.0V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0V$  and  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DCP BIAS VOLTAGES AND INTERNAL RESISTORS (Note 3)</b>						
DP_/DM_ Short Pulldown	$R_{PD}$		320	500	700	k $\Omega$
40% $V_{CC}$ Bias	$V_{AP1A(2A)_P(M)}$		39	40	41	% $V_{CC}$
40% $V_{CC}$ Bias Source Impedance	$R_{AP1A(2A)_P(M)}$		21	30	39	k $\Omega$
53.6% $V_{CC}$ Bias	$V_{AP1A(2A)_M(P)}$		52.6	53.6	54.6	% $V_{CC}$
53.6% $V_{CC}$ Bias Source Impedance	$R_{AP1A(2A)_M(P)}$		16.24	23.2	30.16	k $\Omega$
25% $V_{CC}$ Bias	$V_{SSG\_P/M}$		24	25	26	% $V_{CC}$
25% $V_{CC}$ Bias Source Impedance	$R_{SSG\_P/M}$		5.25	7.5	9.75	k $\Omega$
<b>CDP INTERNAL RESISTORS</b>						
DP Pulldown Resistor	$R_{DP\_CDP}$	CDP mode	14.25	19.53	24.80	k $\Omega$
DM Pulldown Resistor	$R_{DM\_CDP}$	CDP mode	14.25	19.53	24.80	k $\Omega$
<b>CDP HIGH-SPEED COMPARATORS (Note 3)</b>						
Detection Threshold Voltage	$V_{TH\_CDP}$		100	161	205	mV
<b>CDP LOW-SPEED COMPARATORS (Note 3)</b>						
$V_{DM\_SRC}$ Voltage	$V_{DM\_SRC}$	$I_{LOAD} = 0, 200\mu A$	0.5		0.7	V
$V_{DP\_REF}$ Voltage	$V_{DP\_REF}$		0.25		0.4	V
$V_{LGC}$ Voltage	$V_{LGC}$		0.8		2.0	V
$I_{DP\_SINK}$ Current	$I_{DP\_SINK}$	$V_{DP} = 0.15V, 3.6V$	50		150	$\mu A$
<b>LOGIC INPUTS (CB0_, CB1_, SDA, SCL, SAS)</b>						
Input Logic High Voltage	$V_{IH}$		1.4			V
Input Logic Low Voltage	$V_{IL}$				0.4	V
Input Leakage Current	$I_{IN}$	$V_{CC} = 5.5V; V_{IN} = 0V, V_{CC}$	-1		+1	$\mu A$
CB0_/CB1_ Debounce Time	$t_{DEB\_CB\_}$			250		$\mu s$
<b>OPEN-DRAIN LOGIC OUTPUTS (SDA, INT_, CEN_, CEN_)</b>						
$\overline{INT}$ , SDA, CEN_ Output Low Voltage	$V_{OL}$	Output asserted, $I_{SINK} = 4mA$			0.4	V
$\overline{INT}$ , SDA, CEN_ Output Leakage Current	$I_{OH}$	Output not asserted, $V_{CC} = V_{OUT} = 5.5V$			1	$\mu A$
$\overline{CEN}$ Output High Voltage	$V_{OH}$	Output asserted, $I_{SOURCE} = 4mA$	$V_{CC} - 0.4$			V
$\overline{CEN}$ Output Leakage Current	$I_{OL}$	Output not asserted, $V_{CC} = 5.5V, V_{CEN\_} = 0V$			1	$\mu A$
$V_{BUS}$ Toggle Time Accuracy	$t_{VBT}$			$\pm 10$		%

**Electrical Characteristics (continued)**

(V<sub>CC</sub> = 3.0V to 5.5V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +5.0V and T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>I<sup>2</sup>C TIMING CHARACTERISTICS (SEE FIGURE 4)</b>						
I <sup>2</sup> C Maximum Clock Frequency	f <sub>SCL</sub>				400	kHz
<b>ESD PROTECTION</b>						
ESD Protection	V <sub>ESD</sub>	Human Body Model	DP_ and DM_ pins	±15		kV
			All other pins	±2		

**Note 2:** All units are production tested at T<sub>A</sub> = +25°C. Specifications over temperature are guaranteed by design.

**Note 3:** The devices are operational from 3.0V to 5.5V. However, in order for the valid Apple/Samsung resistor-divider networks to function and to have the required DCP/CDP parameters accuracy, V<sub>CC</sub> must stay within the 4.75V to 5.25V range.

**Note 4:** Guaranteed by design, not production tested.

**Test Circuits/Timing Diagrams**

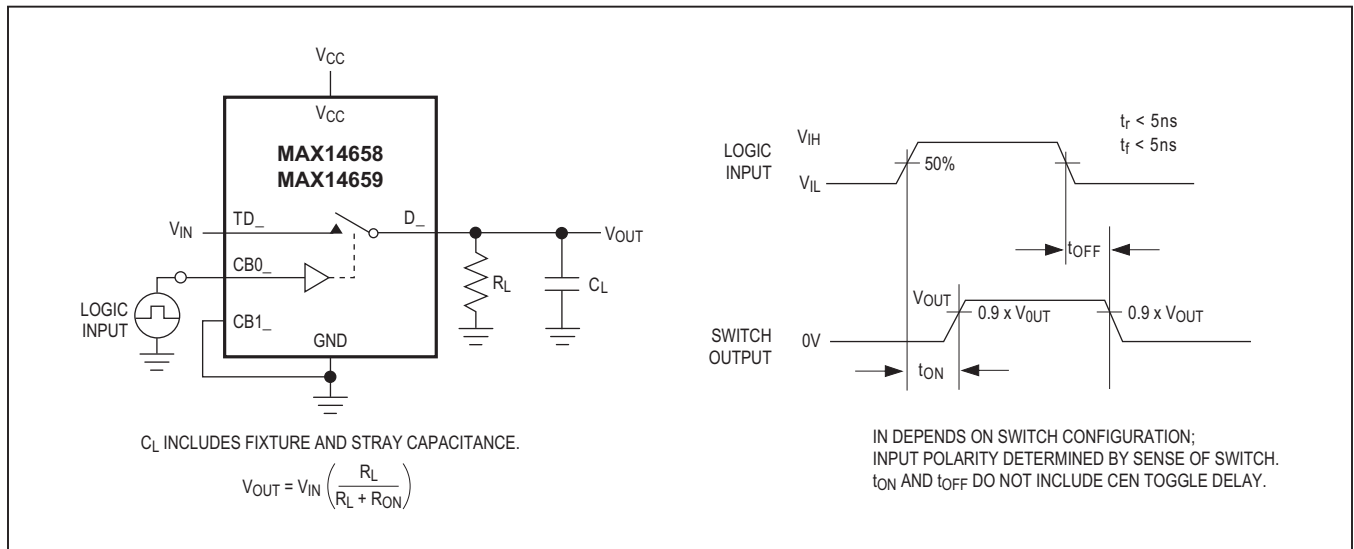


Figure 1. Switching Time

Test Circuits/Timing Diagrams (continued)

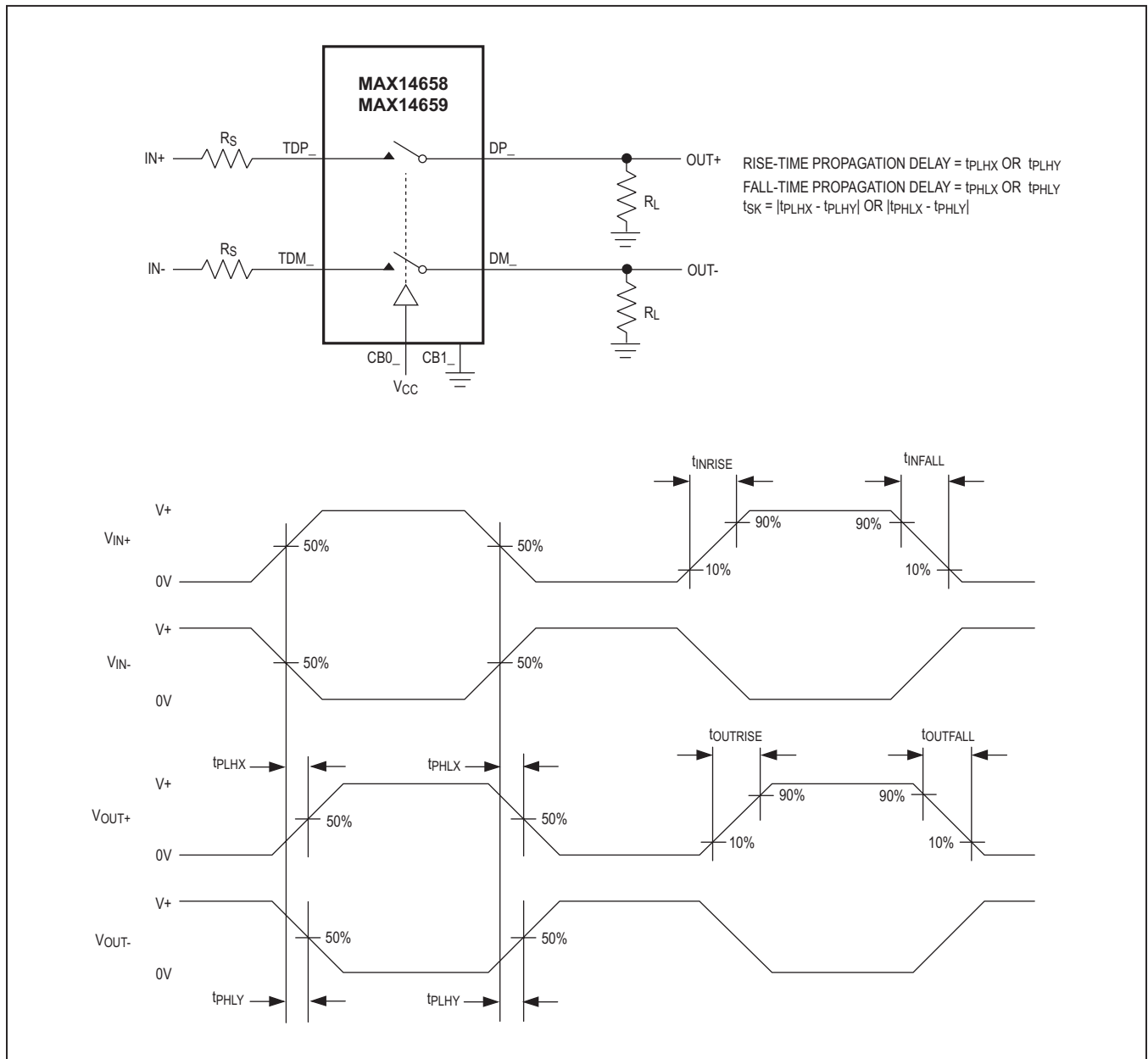


Figure 2. Propagation Delay and Output Skew

Test Circuits/Timing Diagrams (continued)

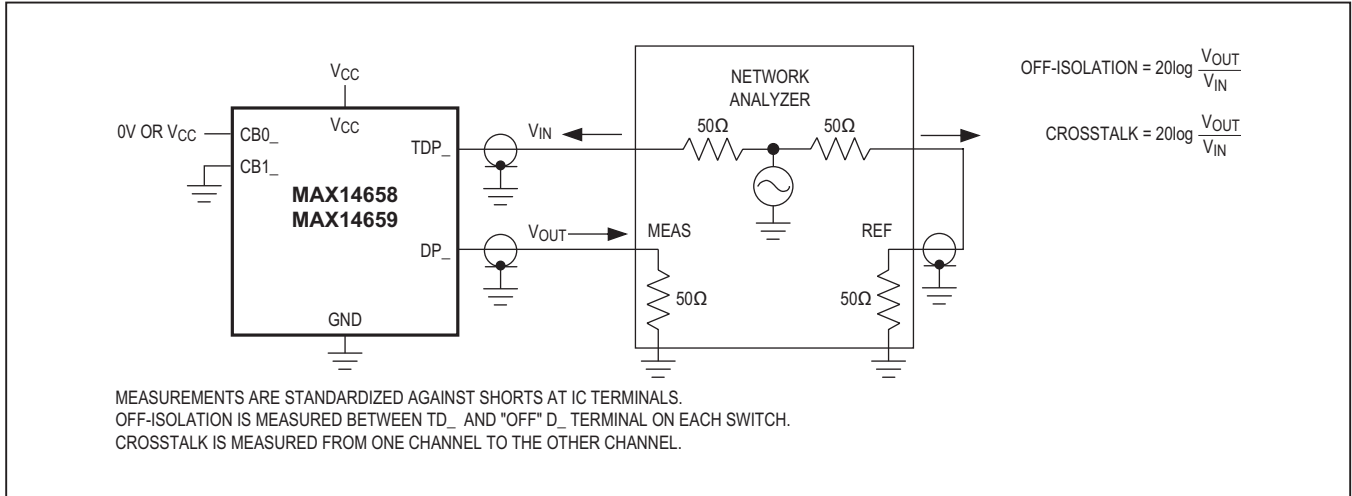


Figure 3. Bandwidth, Off-Isolation, and Crosstalk

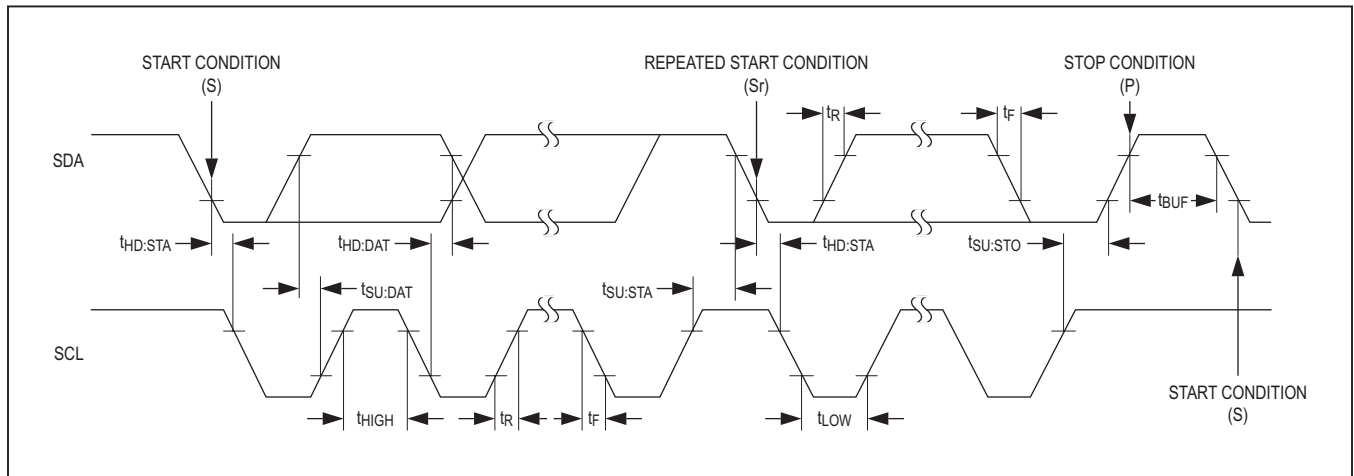
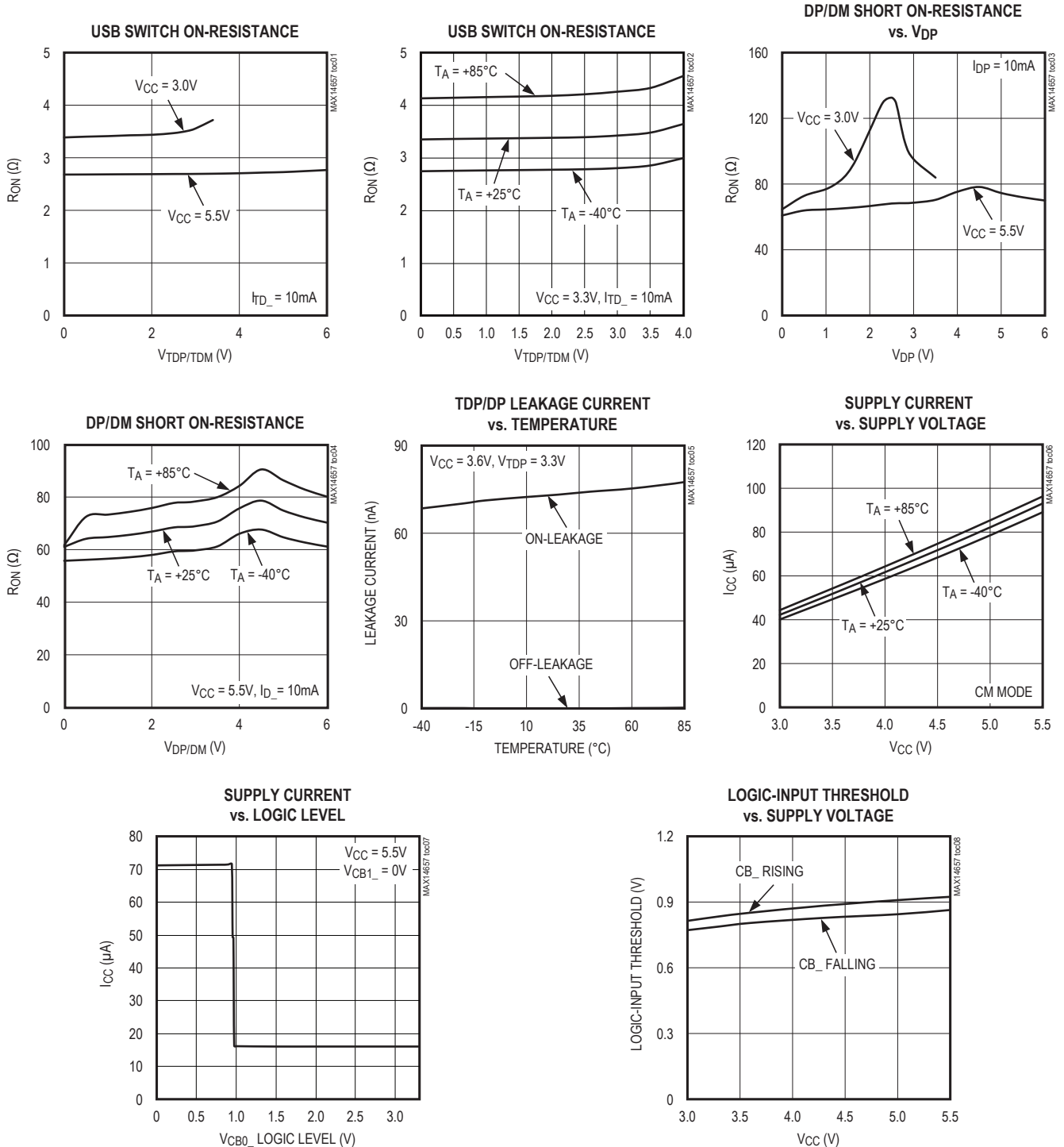


Figure 4. I<sup>2</sup>C Timing Diagram

Typical Operating Characteristics

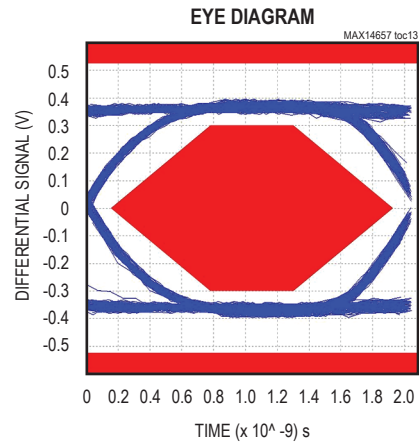
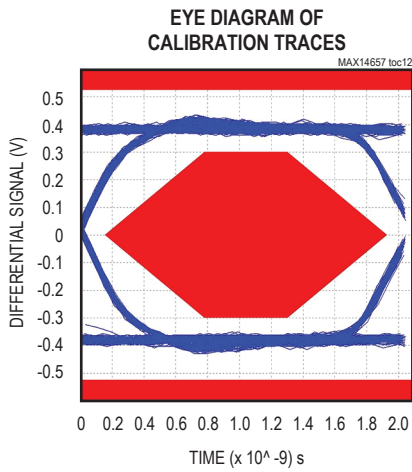
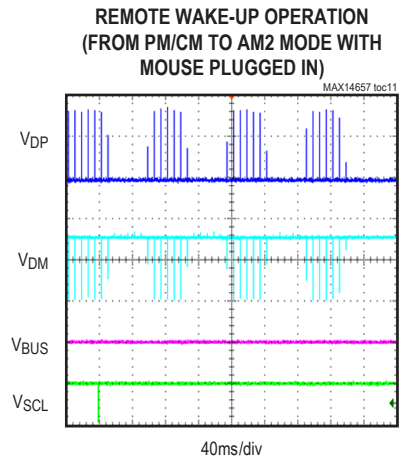
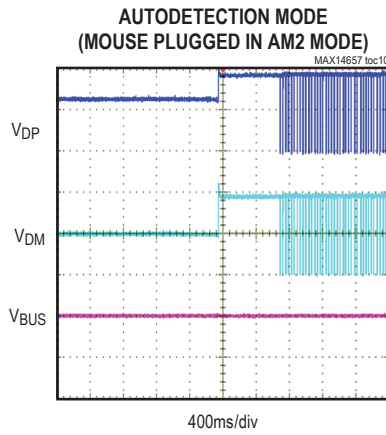
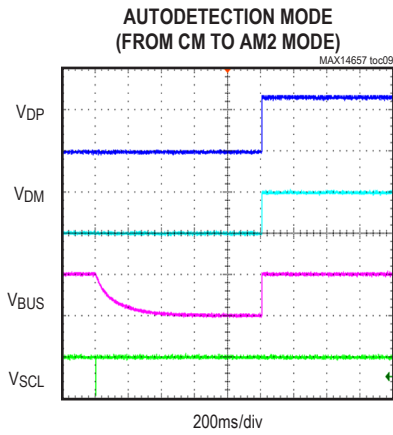
( $V_{CC} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



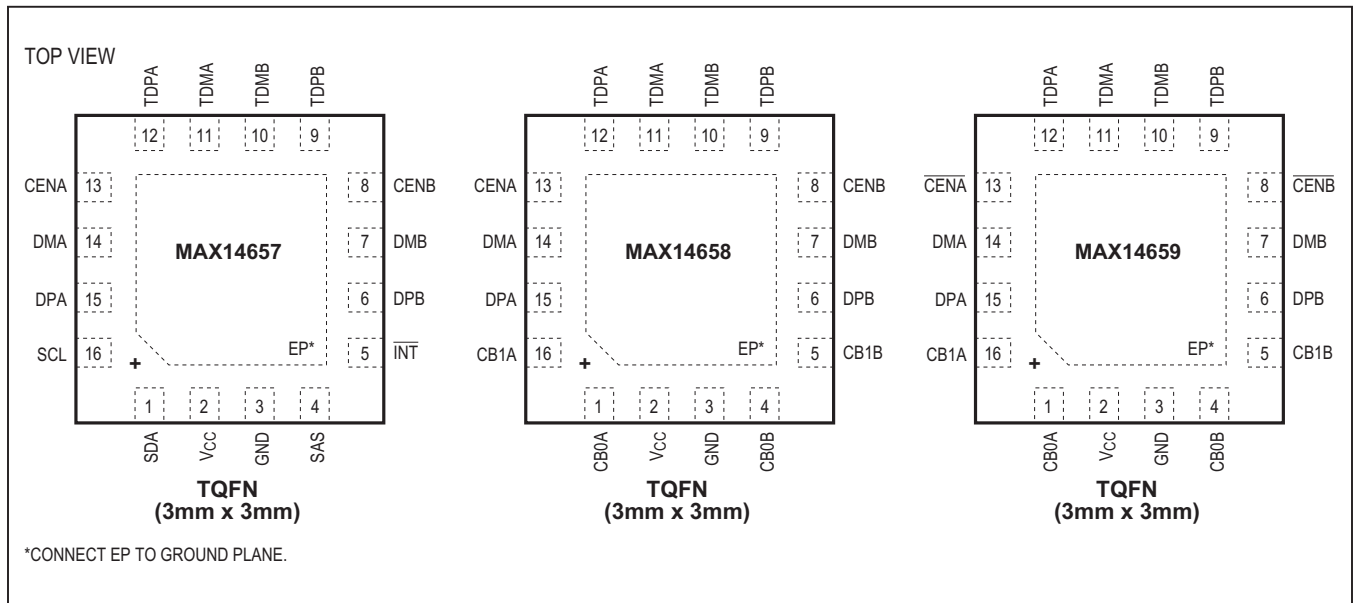


Typical Operating Characteristics (continued)

(TA = +25°C, unless otherwise noted.)



## Pin Configurations



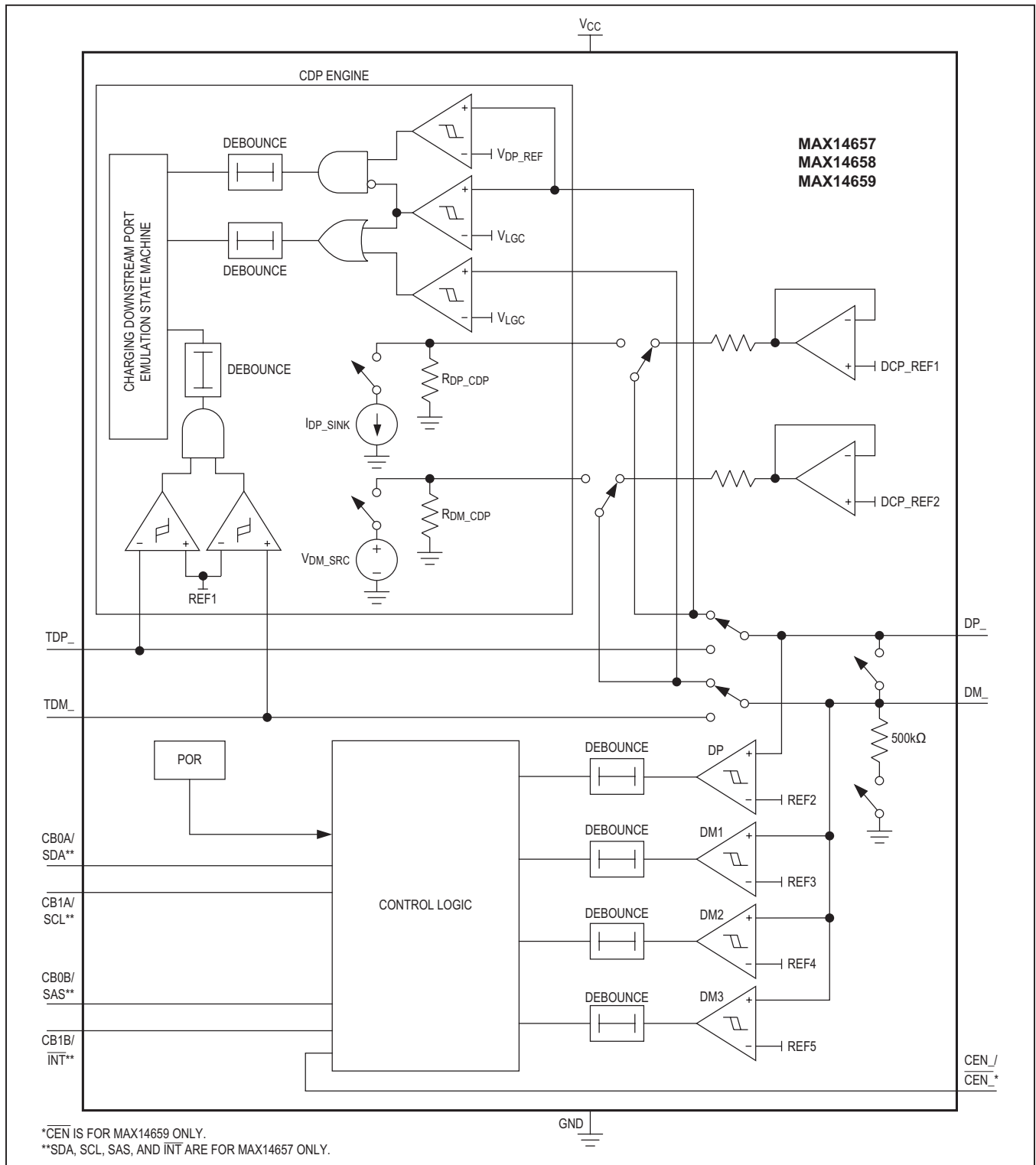
## Pin Descriptions

PIN			NAME	FUNCTION
MAX14657	MAX14658	MAX14659		
1	—	—	SDA	I <sup>2</sup> C Serial Data
—	1	1	CB0A	Switch Control Bit. See the switch control input table 1.
2	2	2	V <sub>CC</sub>	Power Supply. Connect a 0.1μF capacitor between V <sub>CC</sub> and GND as close as possible to the device.
3	3	3	GND	Ground
4	—	—	SAS	I <sup>2</sup> C Slave Address Selection Input
—	4	4	CB0B	Switch Control Bit. See the switch control input table 1.
5	—	—	$\overline{\text{INT}}$	Open-Drain Interrupt Output. $\overline{\text{INT}}$ asserts when interrupt happens.
—	5	5	CB1B	Switch Control Bit. See the switch control input table 1.
6	6	6	DPB	USB Connector D+ Connection
7	7	7	DMB	USB Connector D- Connection

Pin Description (continued)

PIN			NAME	FUNCTION
MAX14657	MAX14658	MAX14659		
8	8	—	CENB	Current-Limit Switch (CLS) Control Output. n-MOSFET open-drain pulldown output disables the CLS with active-high EN.
—	—	8	$\overline{\text{CENB}}$	Current-Limit Switch (CLS) Control Output. p-MOSFET open-drain pullup output disables the CLS with active-low $\overline{\text{EN}}$ .
9	9	9	TDPB	Host USB Transceiver D+ Connection
10	10	10	TDMB	Host USB Transceiver D- Connection
11	11	11	TDMA	Host USB Transceiver D- Connection
12	12	12	TDPA	Host USB Transceiver D+ Connection
13	13	—	CENA	Current-Limit Switch (CLS) Control Output. n-MOSFET open-drain pulldown output disables the CLS with active-high EN.
—	—	13	$\overline{\text{CENA}}$	Current-Limit Switch (CLS) Control Output. p-MOSFET open-drain pullup output disables the CLS with active-low $\overline{\text{EN}}$ .
14	14	14	DMA	USB Connector D- Connection
15	15	15	DPA	USB Connector D+ Connection
16	—	—	SCL	I <sup>2</sup> C Serial Clock
—	16	16	CB1A	Switch Control Bit. See the switch control input table 1.
—	—	—	EP	Exposed Pad. Connect EP to the ground plane.

Functional Diagram



## Detailed Description

The MAX14657/MAX14658/MAX14659 adaptor emulator devices have Hi-Speed USB analog switches that support USB hosts by identifying the USB port as a charger when the USB host is in a low-power mode and cannot enumerate USB devices. The devices feature low 4pF (typ) on-capacitance and low 3Ω (typ) on-resistance when the USB switches are connected. DP\_ and DM\_ are capable of handling signals between 0V and 5.5V over the entire 3.0V to 5.5V supply range.

The MAX14657 are controlled by an I<sup>2</sup>C interface, while the MAX14658/MAX14659 are controlled by the CB0\_ and CB1\_ logic inputs. The I<sup>2</sup>C interface allows further customization over which mode the MAX14657 operates in, and can be used to read back connection information.

Improvements over the MAX14600 USB detector family include support for some smart phones that do not connect after applying 0.6V in charging downstream port (CDP) mode. The devices also support high-current charging of Apple devices while in sleep mode.

### Enhanced Automode

The ICs feature an enhanced automode (AM1, AM2) that allows full charging for Apple devices, USB-compliant devices, and Samsung Galaxy tablets.

## Resistor-Dividers

The internal voltage buffers with series resistors emulate equivalent resistor-divider networks on the data lines to provide support for Apple/Samsung devices. The voltage buffers are disconnected while not in use to minimize the supply current. The voltage buffers are not connected in pass-through mode. [Table 1](#) summarizes the equivalent resistor values connected to DP\_/DM\_ in different charging modes.

## Switch Control

### Digital Controls

Each channel of the MAX14658/MAX14659 features two digital select inputs, CB0\_ and CB1\_, for mode selection. [Table 2](#) shows how the CB1\_/CB0\_ inputs can be used to enter Apple 2A auto-detection charger mode (AM2), pass-through mode (PM), forced charger mode (FM), and pass-through mode with CDP emulation (CM).

In CDP emulation mode, the peripheral device with CDP detection capability draws charging current up to 1.5A immediately without USB enumeration.

**Table 1. DP\_/DM\_ Resistor-Dividers**

CHARGING MODE	DP_ PULLUP	DP_ PULLDOWN	DM_ PULLUP	DM_ PULLDOWN
AM1	75kΩ	49.9kΩ	43.2kΩ	49.9kΩ
AM2	43.2kΩ	49.9kΩ	75kΩ	49.9kΩ

**Table 2. Digital Input State Table for MAX14658/MAX14659**

CB1A/B	CB0A/B	CHARGER/USB	MODE	STATUS
0	0	CHARGER	AM2	2A Autodetection Charger Mode. For Apple, Samsung Galaxy tablets, and USB-compliant devices. Voltage buffers emulating Apple 2A resistor-dividers are connected to DP_/DM_.
0	1	USB	PM	USB Pass-Through Mode. DP_/DM_ are connected to TDP_/TDM_.
1	0	CHARGER	FM	Forced Dedicated Charger Mode. DP_ and DM_ are shorted.
1	1	USB	CM	USB Pass-Through Mode with CDP Emulation. Autoconnects DP_/DM_ to TDM_/TDM_ depending on CDP detection status.

**I<sup>2</sup>C Controls**

The MAX14657 mode is controlled by the MODE\_SEL[2:0] bits. Table 3 shows how these bits control the device. In addition to being configurable in all modes, the MAX14657 can be configured for the Apple (AP1 and AP2 modes), Samsung Galaxy (SS mode) devices, and Automodes (AM1 and AM2).

**Legacy D+/D- Detect**

The devices support charging devices that use a D+/D- short to indicate it is ready for charging. This is done by monitoring the voltage at both the DP\_ and DM\_ terminals and triggering when they are both higher than their comparator thresholds.

**Auto Peripheral Reset**

The MAX14658/MAX14659 feature an autocurrent limit switch control output. This feature resets the peripheral

connected to VBUS in the event the USB host switches to or from standby mode. CEN\_ or CEN\_ are pulsed for 1s (typ) on the rising or falling edge of CB0\_ or CB1\_ (Figure 5 and Figure 6).

**Pass-Through Mode**

When the ICs are configured in pass-through mode (PM), TDP\_/TDM\_ are always connected to DP\_/DM\_ and no resistor-dividers or power sources are applied to DP\_/DM\_.

**Forced Charger Modes**

The ICs can be configured in different forced dedicated charging port (DCP) modes; VBUS is enabled and DP\_ and DM\_ are shorted (FM mode) or connected to the voltage buffers emulating resistor-dividers (all other modes). Table 4 summarizes the equivalent resistor-divider values in each forced mode.

**Table 3. Digital Input State Table for MAX14657**

MODE_SEL_A/B			CHARGER/USB	MODE	STATUS
[2]	[1]	[0]			
0	0	0	AUTOMODE CHARGER	AM2	2A Autodetection Charger Mode. For Apple, Samsung Galaxy tablets, and USB-compliant devices. Voltage buffers emulating Apple 2A resistor-dividers are connected to DP_/DM_.
0	0	1	USB	PM	USB Pass-Through Mode. DP_/DM_ are connected to TDP_/TDM_.
0	1	0	FORCED CHARGER	FM	Forced Dedicated Charger Mode. DP_ and DM_ are shorted.
0	1	1	USB	CM	USB Pass-Through Mode with CDP Emulation. Autoconnects DP_/DM_ to TDP_/TDM_ depending on CDP detection status.
1	0	0	AUTOMODE CHARGER	AM1	1A Autodetection Charger Mode. For Apple, Samsung Galaxy tablets, and USB-compliant devices. Voltage buffers emulating Apple 1A resistor-dividers are connected to DP_/DM_.
1	0	1	FORCED CHARGER	AP1	Forced 1A Charger Mode for Apple Devices. Voltage buffers emulating Apple 1A resistor-dividers are connected to DP_/DM_.
1	1	0	FORCED CHARGER	AP2	Forced 2A Charger Mode for Apple Devices. Voltage buffers emulating Apple 2A resistor-dividers are connected to DP_/DM_.
1	1	1	FORCED CHARGER	SS	Forced 2A Charger Mode for Samsung Galaxy Tablets. Voltage buffers emulating Samsung resistor-dividers are connected to DP_/DM_ and DP_ and DM_ are shorted.

**Table 4. Forced Charging Modes**

CHARGING MODE	DP_ PULLUP	DP_ PULLDOWN	DM_ PULLUP	DM_ PULLDOWN
FM	N/A	N/A	N/A	N/A
SS	30kΩ	10kΩ	30kΩ	10kΩ
AP1	75kΩ	49.9kΩ	43.2kΩ	49.9kΩ
AP2	43.2kΩ	49.9kΩ	75kΩ	49.9kΩ

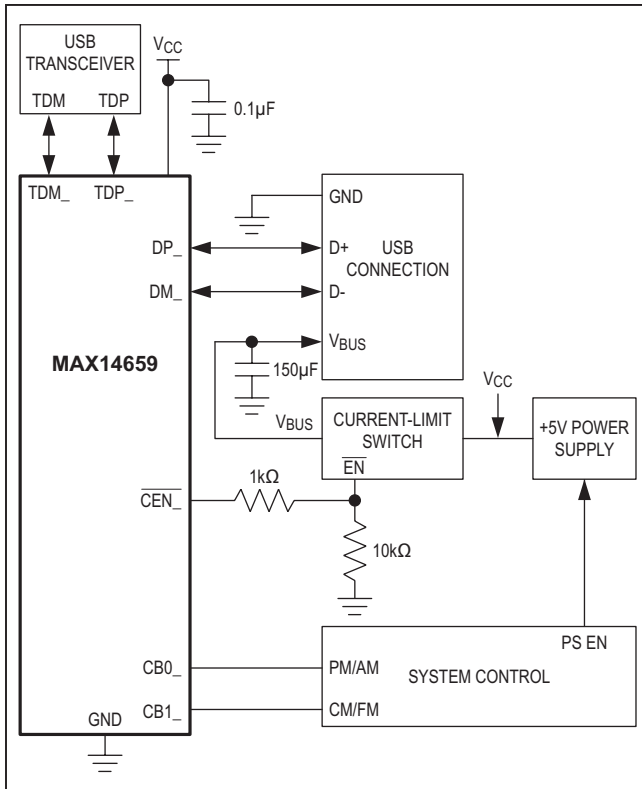


Figure 5. MAX14659 Peripheral Reset Applications Diagram (CEN is CEN for MAX14658)

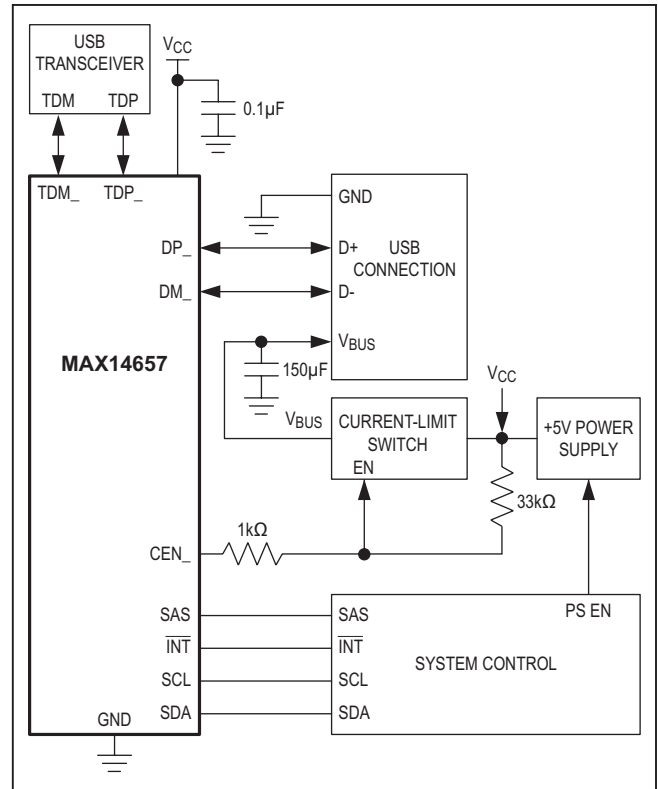


Figure 6. MAX14657 Peripheral Reset Applications Diagram

Table 5. USB Host Power States

STATE	DESCRIPTION
S0	System On
S1	Power to the CPU(s) and RAM is maintained; devices that do not indicate they must remain on may be powered down.
S2	CPU is Powered Off
S3	Standby (Suspend to Ram): System memory context is maintained, all other system context is lost.
S4	Hibernate: Platform context is maintained.
S5	Soft-Off

### Automatic Detection with Remote Wakeup Support

The devices feature automatic detection charger mode (AM1/AM2) for dedicated chargers and USB masters. In automatic detection charger mode, the device monitors

the voltages on DM\_ and DP\_ with voltage buffers connected to determine the type of device attached.

If a USB-compliant device is connected, DP\_ and DM\_ are shorted together to commence charging. Once the charging device is removed, the short between DP\_ and DM\_ is disconnected and the voltage buffer is applied. A pull-down resistor on the shorted DP\_/DM\_ node ensures that a disconnect is detected.

### USB Pass-Through Mode with CDP Emulation

The ICs feature a pass-through mode with CDP emulation (CM). This is to support the higher charging current capability during the pass-through mode in normal USB operation (S0 state). The peripheral device equipped with CDP detection capability can draw a charging current as defined in USB battery charger specification 1.2 when the charging host supports the CDP mode. This is a useful feature since most host USB transceivers do not have the CDP function. Table 5 summarizes the USB host power states.

**Table 6. Register Map/Register Descriptions**

REGISTER	ADDR	TYPE	POR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DeviceID	0x00	R	0x11	CHIPID[3:0]				CHIPREV[3:0]			
Control1	0x01	R/W	0xA7	FUO	FUO	FUO	FUO	FUO	FUO	FUO	FUO
Control2	0x02	R/W	0x50	LOW_PWR	FUO	FUO	FUO	FUO	FUO	DIS_CDP	FUO
Control3	0x03	R/W	0xE9	CEN_CNT[1:0]			CEN_DEL[2:0]		MODE_SEL[2:0]		
Control4	0x04	R/W	0x00	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Control5	0x05	R/W	0x6B	INT_EN	USB_SW[1:0]		FUO	CEN_POL	FUO	RWU_DFT	RWU_LS
INT	0x06	R	0x00	CDP_DEVi	BYPASS_CDPi	CDP_CN_TMRi	RFU	USB_XFRi	RWUi	CEN_TOG_STi	CEN_TOG_SPi
STATUS	0x07	R	0x00	CDP_DEVs	BYPASS_CDPs	CDP_CN_TMRs	RFU	USB_XFRs	RWUs	RFU	CEN_TOG_Ss
MASK	0x08	R/W	0x00	CDP_DEVm	BYPASS_CDPm	CDP_CN_TMRm	RFU	USB_XFRm	RWUm	CEN_TOG_STm	CEN_TOG_SPm

FUO = Factory use only. Do not change from POR values.

RFU = Reserved for future use. Do not change from POR values.

**Table 7. Device ID Register**

<b>ADDRESS:</b>		<b>0x00</b>							
<b>MODE:</b>		<b>Read Only</b>							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>	
<b>NAME</b>	CHIPID[3:0]				CHIPREV[3:0]				
<b>RESET</b>	0	0	0	1	0	0	0	1	
<b>CHIPID[3:0]</b>	The CHIPID[3:0] bits show information about the version of the MAX14657.								
<b>CHIPREV[3:0]</b>	The CHIPREV[3:0] bits show information about the revision of the MAX14657 silicon.								

**Table 8. Control 1 Register**

<b>ADDRESS:</b>		<b>0x01</b>							
<b>MODE:</b>		<b>Read/Write</b>							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>	
<b>NAME</b>	FUO	FUO	FUO	FUO	FUO	FUO	FUO	FUO	
<b>RESET</b>	1	0	1	0	0	1	1	1	
<b>FUO</b>	Factory Use Only. Do not modify from reset values.								

**Table 9. Control 2 Register**

<b>ADDRESS:</b>		<b>0x02</b>							
<b>MODE:</b>		<b>Read/Write</b>							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>	
<b>NAME</b>	LOW_PWR	FUO	FUO	FUO	FUO	FUO	DIS_CDP	FUO	
<b>RESET</b>	0	1	0	1	0	0	0	0	
<b>LOW_PWR</b>	Low-Power Mode 0 = MAX14657 is in normal operation 1 = MAX14657 is in low-power mode. All circuitry other than the I <sup>2</sup> C interface is disabled.								
<b>DIS_CDP</b>	Disable CDP Signal 0 = CDP signaling enabled 1 = CDP signaling disabled								
<b>FUO</b>	Factory Use Only. Do not modify from reset values.								



**Table 10. Control 3 Register**

ADDRESS:		0x03						
MODE:		Read/Write						
BIT	7	6	5	4	3	2	1	0
NAME	CEN_CNT[1:0]		CEN_DEL[2:0]			MODE_SEL[2:0]		
RESET	1	1	1	0	1	0	0	1
<b>CEN_CNT[1:0]</b>	CEN_State Control. Directly controls the CEN_ output independent of automatic cycling. 00 = CEN_ asserted 01 = FUIO 10 = CEN_ deasserted (intend to turn on current-limit switch) 11 = CEN_ controlled by CDP/DCP/AM modes							
<b>CEN_DEL[2:0]</b>	CEN_ Pulse Delay. Controls how long V <sub>BUS</sub> toggles last outside of AM mode. 000 = 125ms 001 = 250ms 010 = 350ms 011 = 500ms 100 = 750ms 101 = 1.0s 110 = 1.5s 111 = 2s							
<b>MODE_SEL[2:0]</b>	Operating Mode Control. 000 = AM2 001 = PM 010 = FM 011 = CM 100 = AM1 101 = AP1 110 = AP2 111 = SS							

**Table 11. Control 4 Register**

ADDRESS:		0x04						
MODE:		Read/Write						
BIT	7	6	5	4	3	2	1	0
NAME	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
RESET	0	0	0	0	0	0	0	0
RFU	Reserved for Future Use							

**Table 12. Control 5 Register**

ADDRESS:		0x05						
MODE:		Read/Write						
BIT	7	6	5	4	3	2	1	0
NAME	INT_EN	USB_SW[1:0]		FUO	CEN_POL	FUO	RWU_DFT	RWU_LS
RESET	0	1	1	0	1	0	1	1
<b>INT_EN</b>	Interrupt Enable. 0 = Interrupt disabled 1 = Interrupt enabled							
<b>USB_SW[1:0]</b>	USB DPDT Switch Control. When the USB switch is forced open (00) or closed (01), the state machine and CEN_output are disabled. 00 = DP_/DM_ in High-Z 01 = DP_/DM_ connected to TDP_/TDM_ 10 = DP_/DM_ controlled by CDP/DCP/AM circuitry 11 = DP_/DM_ controlled by CDP/DCP/AM circuitry							
<b>FUO</b>	Factory Use Only. Do not modify from reset value.							
<b>CEN_POL</b>	CEN Polarity Select. Controls the polarity of the CEN output. 0 = CEN output is active-low $\overline{\text{CEN}}$ 1 = CEN output is active-high CEN							
<b>FUO</b>	Factory Use Only. Do not modify from reset value.							
<b>RWU_DFT</b>	Remote Wake-Up Default 0 = Remote wake-up is off 1 = Remote wake-up is on							
<b>RWU_LS</b>	Remote Wake-Up for Low-Speed Only Select 0 = Remote wake-up for both FS/HS and LS USB devices 1 = Remote wake-up for only LS devices							

**Table 13. Interrupt Register**

ADDRESS:		0x06						
MODE:		Read Only						
BIT	7	6	5	4	3	2	1	0
NAME	CDP_DEVi	BYPASS_CDPi	CDP_CNi	RFU	USB_XFRi	RWUi	CEN_TOG_STi	CEN_TOG_SPi
RESET	0	0	0	0	0	0	0	0
<b>CDP_DEVi</b>	CDP Device Detect Status Interrupt. CDP_DEVi is set when a CDP device is detected following the CDP handshake procedure in CM mode. 0 = No interrupt 1 = Interrupt							
<b>BYPASS_CDPi</b>	Bypass CDP Running Status Interrupt. BYPASS_CDPi is set when the CDP handshake procedure is bypassed. 0 = No interrupt 1 = Interrupt							
<b>CDP_CNi</b>	CDP Connect Status Interrupt. CDP_CNi is set whenever a CDP connection check is in progress. 0 = No interrupt 1 = Interrupt							
<b>RFU</b>	Reserved for Future Use							
<b>USB_XFRi</b>	USB Session Interrupt. USB_XFRi is set when there is USB data detected in CM mode and DP_/DM_ are connected to TDP/TDM. 0 = No interrupt 1 = Interrupt							
<b>RWUi</b>	Remote Wake-Up Status Interrupt. RWUi is set whenever a remote wake-up is performed in AM mode. 0 = No interrupt 1 = Interrupt							
<b>CEN_TOG_STi</b>	CEN_Toggle Start Monitor Interrupt. CEN_TOG_STi is set at the start of a V <sub>BUS</sub> toggle, when V <sub>BUS</sub> is first disabled. 0 = No interrupt 1 = Interrupt							
<b>CEN_TOG_SPi</b>	CEN_Toggle Stop Monitor Interrupt. CEN_TOG_SPi is set at the end of a V <sub>BUS</sub> toggle, when V <sub>BUS</sub> is no longer disabled. 0 = No interrupt 1 = Interrupt							

**Table 14. Status Register**

ADDRESS:		0x07						
MODE:		Read Only						
BIT	7	6	5	4	3	2	1	0
NAME	CDP_DEVs	BYPASS_CDPs	CDP_CNs	RFU	USB_XFRs	RWUs	RFU	CEN_TOGs
RESET	0	0	0	0	0	0	0	0
<b>CDP_DEVs</b>	CDP Device Detect Status. CDP_DEVs is set when a CDP device is detected following the CDP handshake procedure in CM mode and cleared when it is disconnected. 0 = CDP device not detected 1 = CDP device detected							
<b>BYPASS_CDPs</b>	Bypass CDP Running Status. BYPASS_CDPs is set when the CDP handshake procedure is bypassed. 0 = CDP signaling used 1 = CDP signaling bypassed							
<b>CDP_CNs</b>	CDP Connect Status. CDP_CNs is set while a CDP connection attempt is in progress. 0 = No CDP connection check in progress 1 = CDP connection check in progress							
<b>RFU</b>	Reserved for Future Use							
<b>USB_XFRs</b>	USB Session Status. USB_XFRs is set while there is USB data detected in CM mode and DP_/DM_ are connected to TDP/TDM. 0 = No USB session in progress 1 = USB session in progress							
<b>RWUs</b>	Remote Wake-Up Status. RWUs is set while a remote wake-up is in progress in AM mode. 0 = Not waiting for RWU 1 = Waiting for RWU							
<b>CEN_TOGs</b>	CEN_Toggle Status. CEN_TOGs is cleared at the start of a V <sub>BUS</sub> toggle and set at the end of the V <sub>BUS</sub> toggle. 0 = V <sub>BUS</sub> toggle in progress 1 = V <sub>BUS</sub> toggle not in progress							

**Table 15. Mask Register**

ADDRESS:		0x08						
MODE:		Read/Write						
BIT	7	6	5	4	3	2	1	0
NAME	CDP_DEV <sub>m</sub>	BYPASS_CDP <sub>m</sub>	CDP_CN <sub>m</sub>	RFU	USB_XFR <sub>m</sub>	RWU <sub>m</sub>	CEN_TOG_ST <sub>m</sub>	CEN_TOG_SP <sub>m</sub>
RESET	0	0	0	0	0	0	0	0
<b>CDP_DEV<sub>m</sub></b>	CDP Device Detect Status Interrupt Mask. Prevents an interrupt from being generated in CDP_DEV <sub>i</sub> when CDP_DEV <sub>s</sub> is set to 1. 0 = Masked 1 = Not masked							
<b>BYPASS_CDP<sub>m</sub></b>	Bypass CDP Running Status Interrupt Mask. Prevents an interrupt from being generated in BYPASS_CDP <sub>i</sub> when BYPASS_CDP <sub>s</sub> is set to 1. 0 = Masked 1 = Not masked							
<b>CDP_CN<sub>m</sub></b>	CDP Connect Status Interrupt Mask. Prevents an interrupt from being generated in CDP_CN <sub>i</sub> when CDP_CN <sub>s</sub> is set to 1. 0 = Masked 1 = Not masked							
<b>RFU</b>	Reserved for Future Use							
<b>USB_XFR<sub>m</sub></b>	USB Session Interrupt Mask. Prevents an interrupt from being generated in USB_XFR <sub>i</sub> when USB_XFR <sub>s</sub> is set to 1. 0 = Masked 1 = Not masked							
<b>RWU<sub>m</sub></b>	Remote Wake-Up Status Interrupt Mask. Prevents an interrupt from being generated in RWU <sub>i</sub> when RWU <sub>s</sub> is set to 1. 0 = Masked 1 = Not masked							
<b>CEN_TOG_ST<sub>m</sub></b>	CEN_Toggle Start Monitor Interrupt Mask. Prevents an interrupt from being generated in CEN_TOG_ST <sub>i</sub> when CEN_TOG_ST <sub>s</sub> is set to 1. 0 = Masked 1 = Not masked							
<b>CEN_TOG_SP<sub>m</sub></b>	CEN_Toggle Stop Monitor Interrupt Mask. Prevents an interrupt from being generated in CEN_TOG_SP <sub>i</sub> when CEN_TOG_SP <sub>s</sub> is set to 1. 0 = Masked 1 = Not masked							

## Applications Information

### I<sup>2</sup>C Interface

The MAX14657 contain an I<sup>2</sup>C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

### Start, Stop, and Repeated Start Conditions

When writing to the MAX14657 using I<sup>2</sup>C, the master sends a START condition (S) followed by the MAX14657 I<sup>2</sup>C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a Repeated START condition (Sr) to communicate to another I<sup>2</sup>C slave. See [Figure 7](#).

### Slave Address

The MAX14657 is the I<sup>2</sup>C version that has different slave addresses for each port ([Table 16](#)). Set the Read/Write bit high to configure the MAX14657 to read mode. Set the Read/Write bit low to configure the MAX14657 to write mode. Further, two possible slave addresses can be configured for each port through the Slave Address Selection (SAS) input (see [Table 16](#)), allowing up to two MAX14657 devices to share the same interface bus. The address is the first byte of information sent to the MAX14657 after the START condition.

### Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the [Start, Stop, and Repeated Start Conditions](#) section). Both SDA and SCL remain high when the bus is not active.

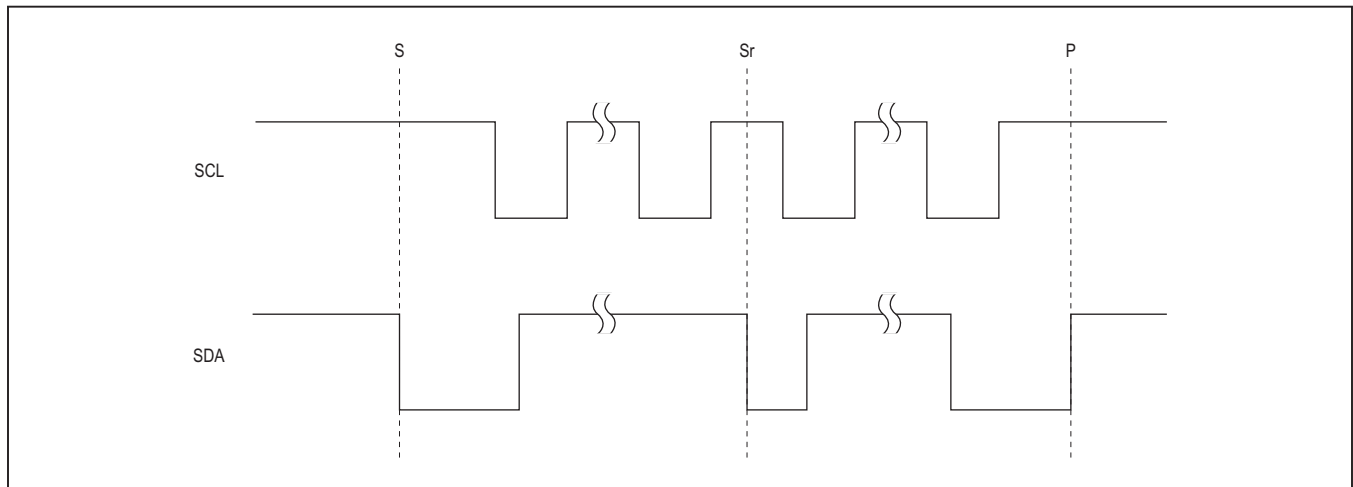


Figure 7. I<sup>2</sup>C START, STOP, and REPEATED START Conditions

Table 16. MAX14657 I<sup>2</sup>C Slave Addresses

SAS	Port	A6	A5	A4	A3	A2	A1	A0	R/W	READ ADDR	WRITE ADDR
GND	A	0	1	0	0	1	0	0	1/0	0x49	0x48
	B	0	1	0	1	1	0	0	1/0	0x59	0x58
V <sub>CC</sub>	A	0	1	0	0	1	0	1	1/0	0x4B	0x4A
	B	0	1	0	1	1	0	1	1/0	0x5B	0x5A

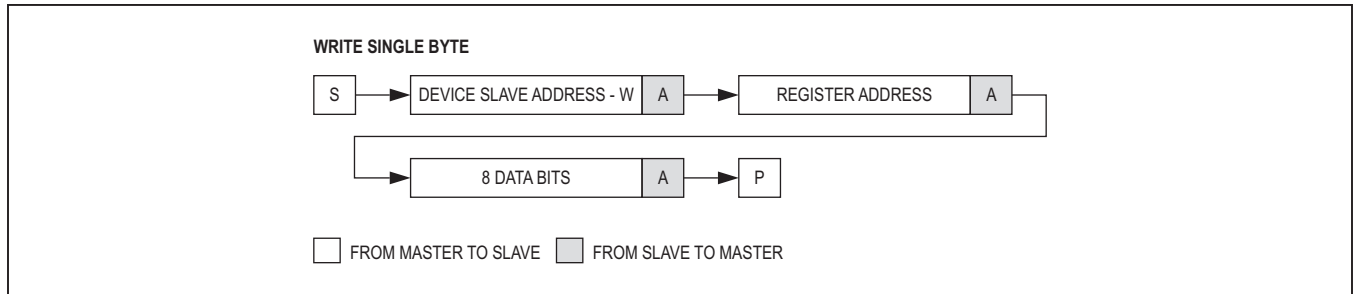


Figure 8. Write Byte Sequence

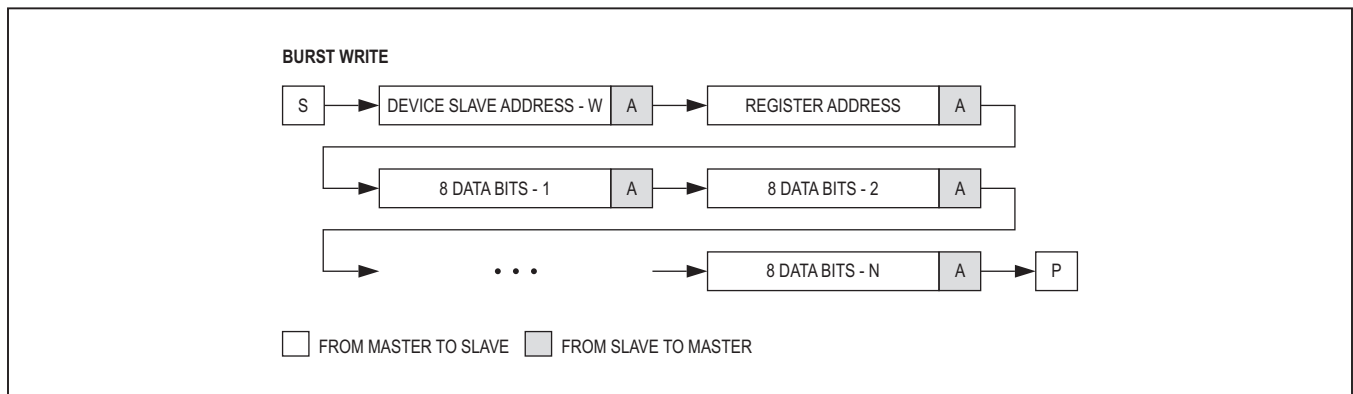


Figure 9. Burst Write Sequence

### Single Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 8). The following procedure describes the single byte write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends 8 data bits
- 7) The slave asserts an ACK on the data line
- 8) The master generates a STOP condition

### Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 9). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends 8 data bits
- 7) The slave asserts an ACK on the data line
- 8) Repeat 6 and 7 (N-1) times
- 9) The master generates a STOP condition

**Single Byte Read**

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 10). The following procedure describes the single byte read operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7) The master sends the 7-bit slave address plus a read bit (high)
- 8) The addressed slave asserts an ACK on the data line
- 9) The slave sends 8 data bits

10) The master asserts a NACK on the data line

11) The master generates a STOP condition

**Burst Read**

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 11). The following procedure describes the burst byte read operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7) The master sends the 7-bit slave address plus a read bit (high)

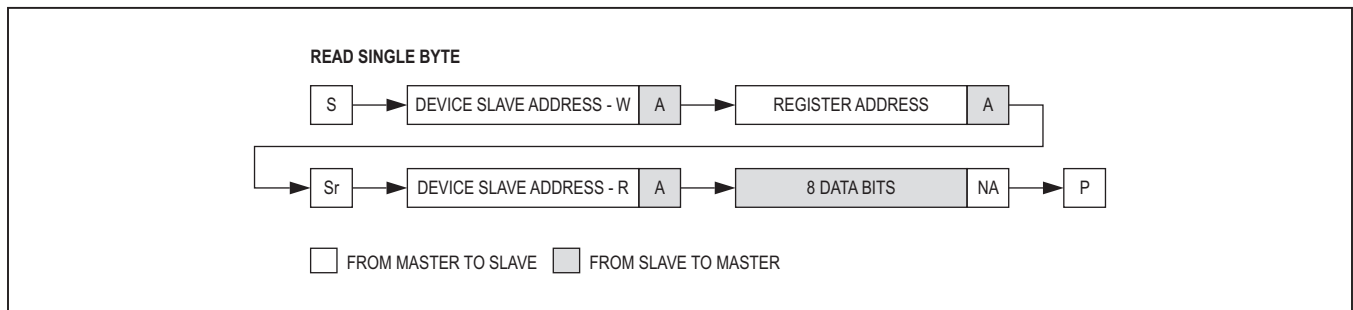


Figure 10. Read Byte Sequence

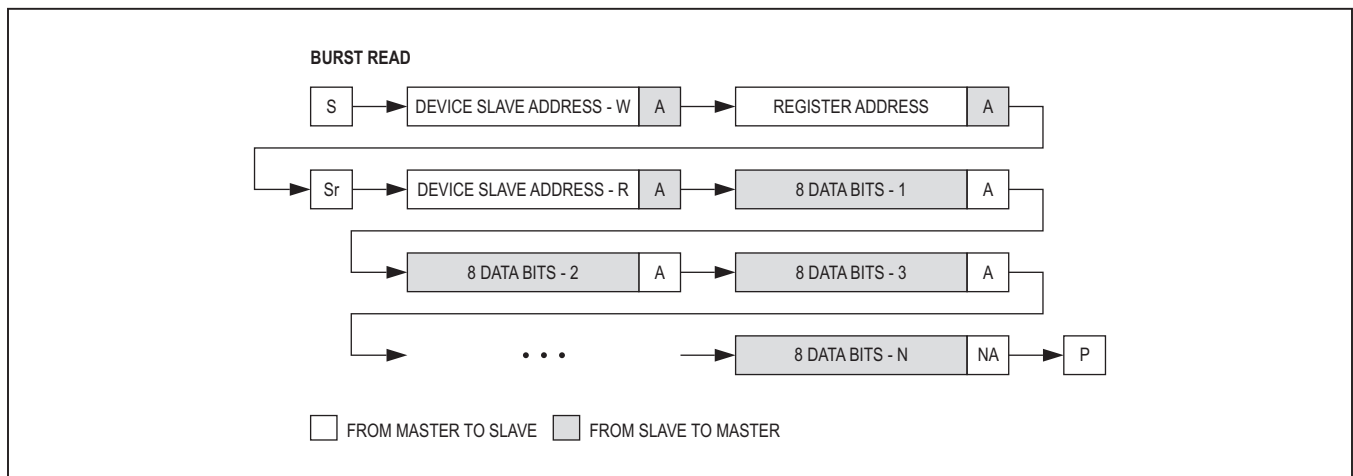


Figure 11. Burst Read Sequence



- 8) The slave asserts an ACK on the data line
- 9) The slave sends 8 data bits
- 10) The master asserts an ACK on the data line
- 11) Repeat 9 and 10 (N-2) times
- 12) The slave sends the last 8 data bits
- 13) The master asserts a NACK on the data line
- 14) The master generates a STOP condition

**Acknowledge Bits**

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14657 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see [Figure 12](#)). To generate a NACK,

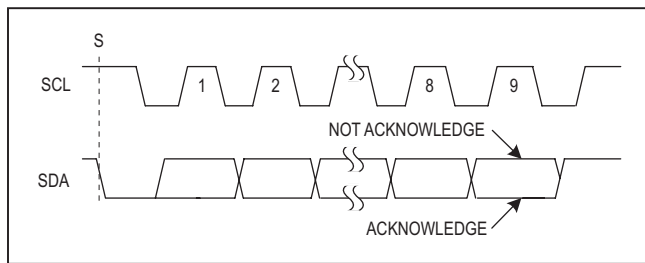


Figure 12. Acknowledge

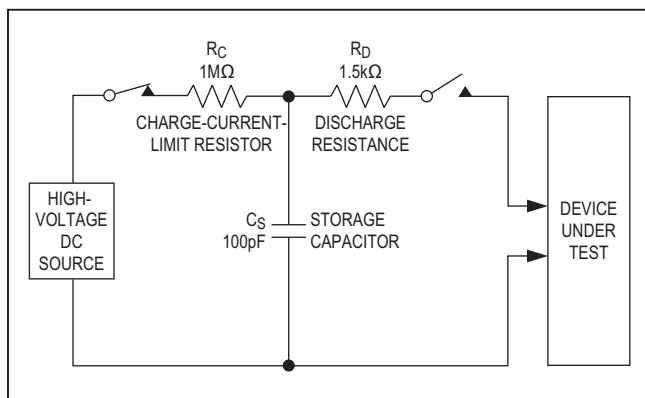


Figure 13. Human Body ESD Test Model

leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

**High ESD Protection**

Electrostatic discharge (ESD) protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly. DP<sub>-</sub> and DM<sub>-</sub> are further protected against high ESD up to ±15kV (HBM) without damage. These ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the IC continues to function without latchup.

**ESD Test Conditions**

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

**Human Body Model**

[Figure 13](#) shows the Human Body Model. [Figure 14](#) shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

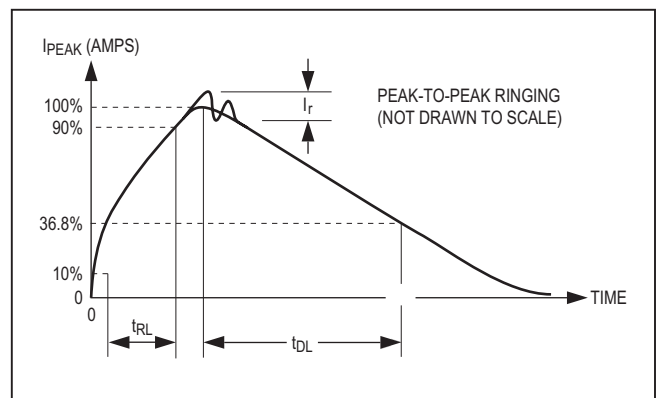
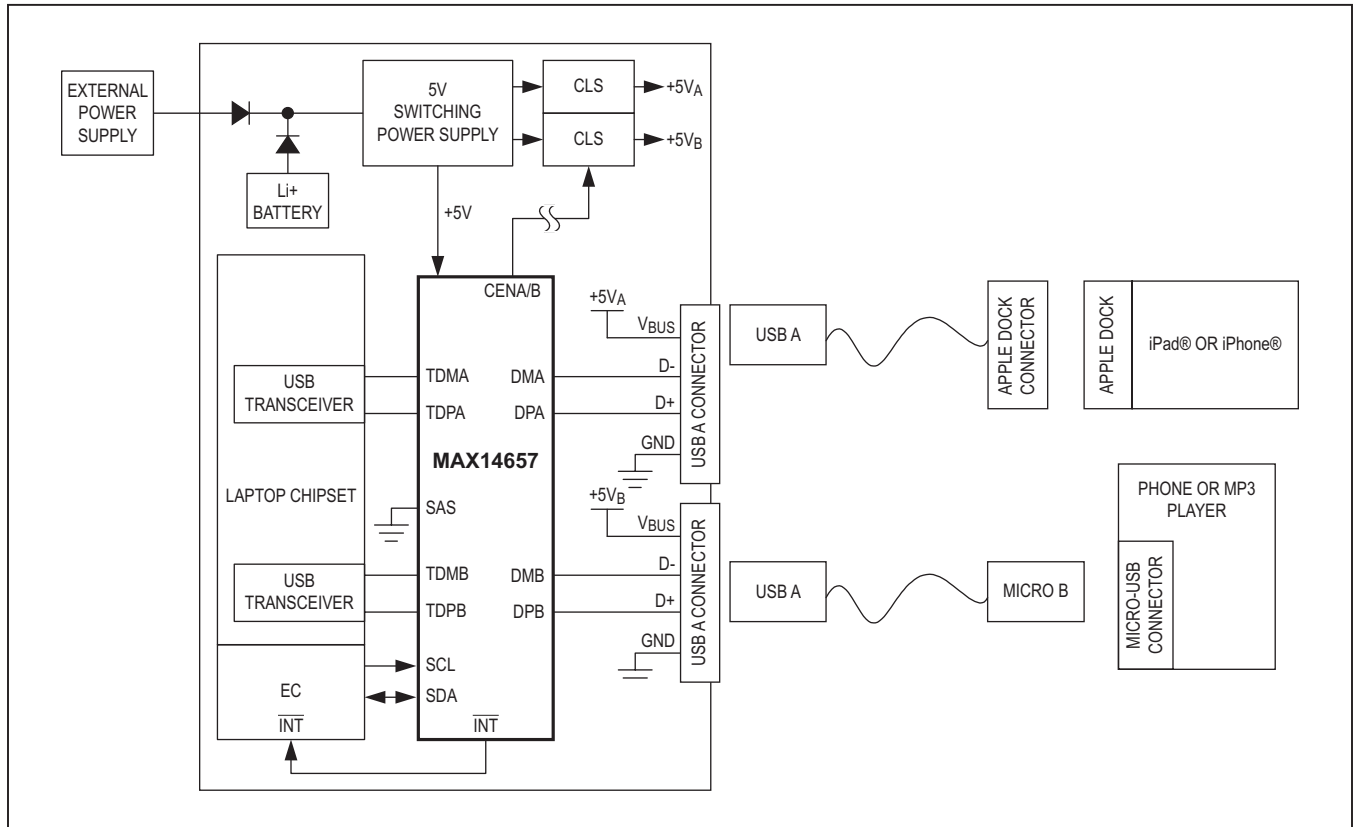


Figure 14. Human Body Current Waveform

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14657ETE+T	-40°C to +85°C	16 TQFN-EP*
MAX14658ETE+T	-40°C to +85°C	16 TQFN-EP*
MAX14659ETE+T	-40°C to +85°C	16 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1633+5	<a href="#">21-0136</a>	<a href="#">90-0032</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/13	Initial release	—
1	8/13	Updated <i>Ordering Information</i>	26

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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