

### Features

- Single differential LVPECL output
- Supports the following output frequencies: 125MHz or 133MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz – 20MHz): 0.3ps (typical)
- Full 3.3V or 2.5V supply modes
- Commercial and industrial ambient operating temperature
- Available in lead-free package: 8-TSSOP

### Applications

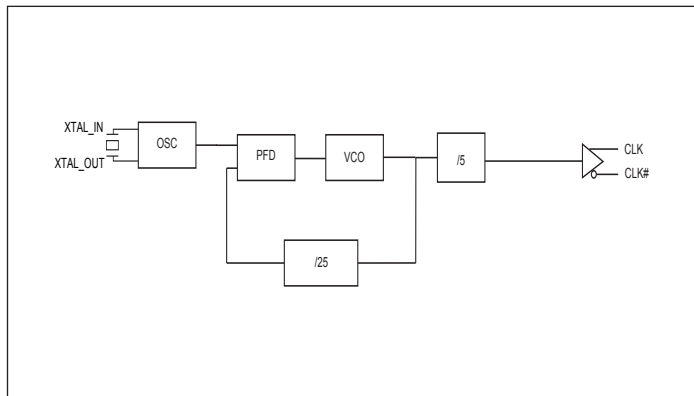
- Networking systems

### Description

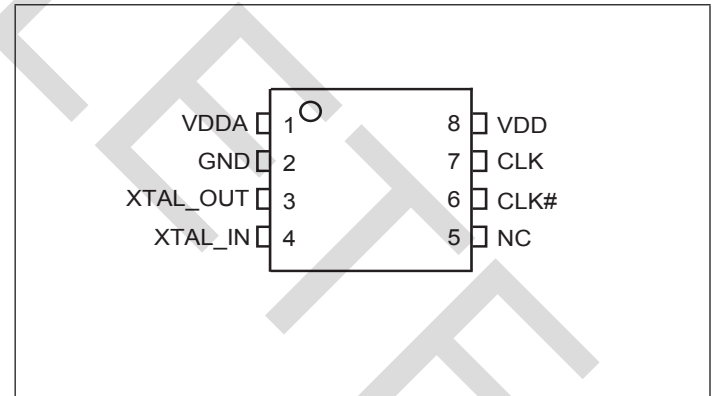
The PI6LC48P21 is a single output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies and is a member of Pericom's HiFlex family of high performance clock solutions. Using a 25MHz or 26.6MHz crystal, it can generate 125MHz or 133MHz output frequencies.

The PI6LC48P21 uses Pericom's proprietary low phase noise PLL technology to achieve ultra low phase jitter, so it is ideal for Ethernet interface in all kind of systems.

### Block Diagram



### Pin Configuration



### Pinout Table

Pin No.	Pin Name	I/O Type	Description
1	VDDA	Power	Analog Power Supply
2	GND	Power	Ground
3, 4	XTAL_OUT, XTAL_IN	Crystal	Crystal Input and Output
5	NC		No Connect
6, 7	CLK#, CLK	Output	Output Clock
8	VDD	Power	Core Power Supply

### Output Frequency Table

Xtal Frequency (MHz)	Output Frequency (MHz)
25	125
26.6	133

### Typical Crystal Requirement

Parameter	Minimum	Typical	Maximum	Units
Mode of Oscillation	Fundamental			
Frequency	22.4	25	28	MHz
Equivalent Series Resistance (ESR)			50	$\Omega$
Shunt Capacitance			7	pF
Drive Level			1	mW

### Recommended Crystal Specification

Pericom recommends:

a) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm  
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

b) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)

**Maximum Ratings** (Over operating free-air temperature range)

Storage Temperature.....	-65°C to +155°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
3.3V Analog Supply Voltage.....	-0.5 to +3.6V
ESD Protection (HBM) .....	2000V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics**

**Power Supply DC Characteristics**, ( $V_{DD} = V_{DDA}$ ,  $T_A = -40$  to  $85^\circ\text{C}$ )

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD}, V_{DDA}$	Core, Analog Supply Voltage		3.0	3.3	3.6	V
$V_{DD}, V_{DDA}$	Core, Analog Supply Voltage		2.375	2.5	2.625	V
GND	Power Supply Current				85	mA
$I_{DDA}$	Analog Supply Current				25	mA

**LVPECL DC Electrical Characteristics**

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output High Voltage <sup>(1)</sup>	$V_{DD} = 3.3\text{V}$	1.9		2.4	V
		$V_{DD} = 2.5\text{V}$	1.1		1.6	
$V_{OL}$	Output Low Voltage <sup>(1)</sup>	$V_{DD} = 3.3\text{V}$	1.2		1.6	V
		$V_{DD} = 2.5\text{V}$	0.4		0.8	

**Note:** 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

**LVPECL AC Electrical Characteristics**

LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

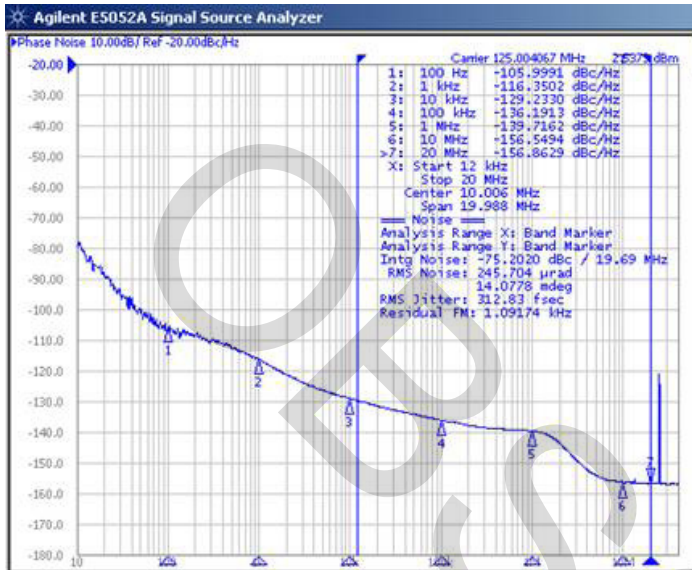
Symbol	Parameter	Condition	Min.	Typ.	Max	Units
$f_{OUT}$	Output Frequency		112	125	140	MHz
$t_{jit(\omega)}$	RMS Phase Jitter, (Random) <sup>(1)</sup>	125MHz, (1.875MHz - 20MHz)		0.15		ps
		125MHz, (12kHz - 20MHz)		0.3		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%			400	ps
$\sigma_{DC}$	Output Duty Cycle		48		52	%

**Note:**

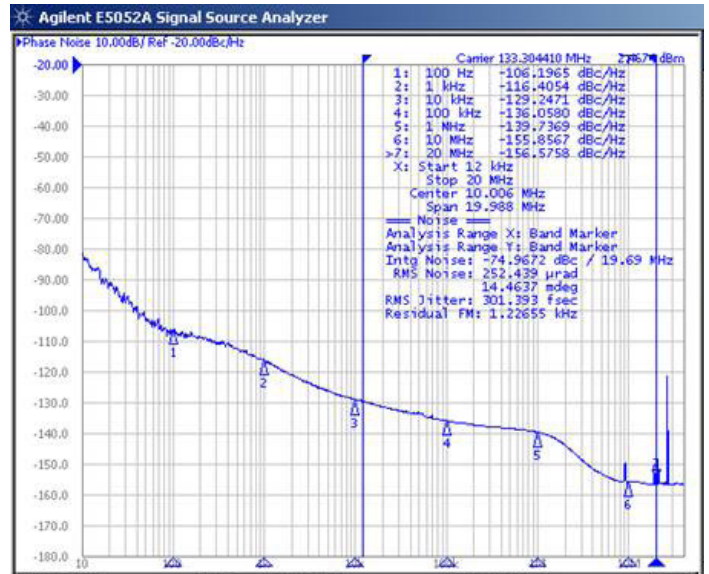
1. Please refer to the Phase Noise Plots.

**Phase Noise Plot**

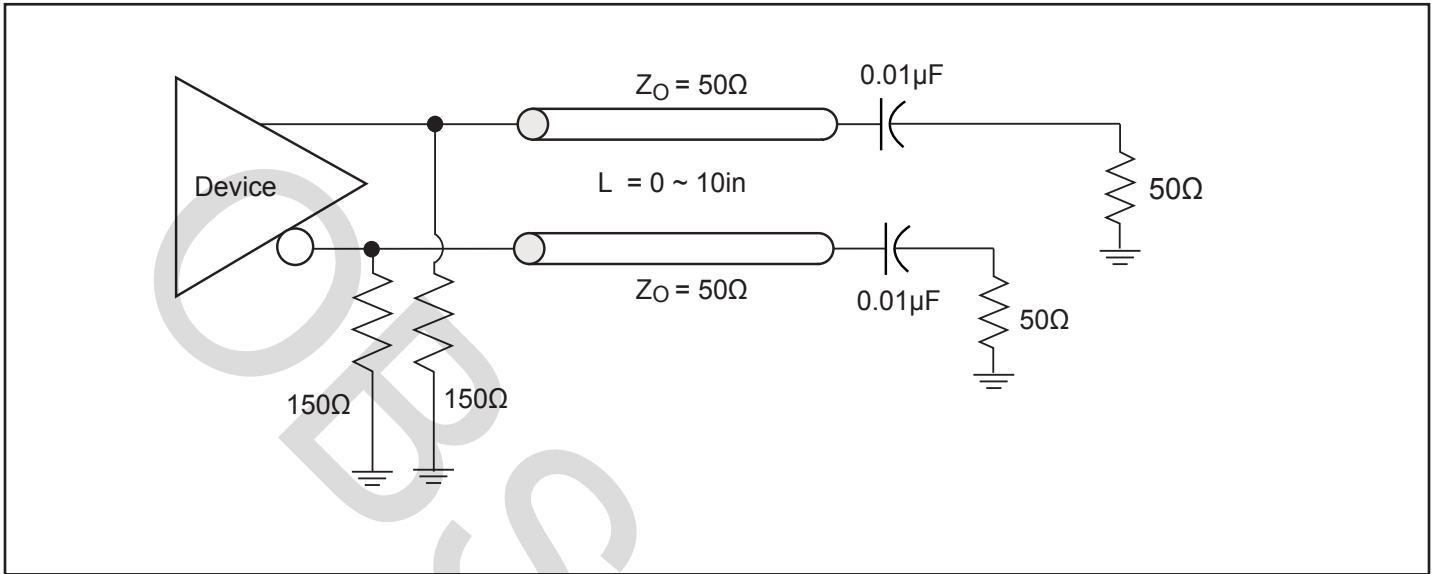
125MHz Output



133MHz Output

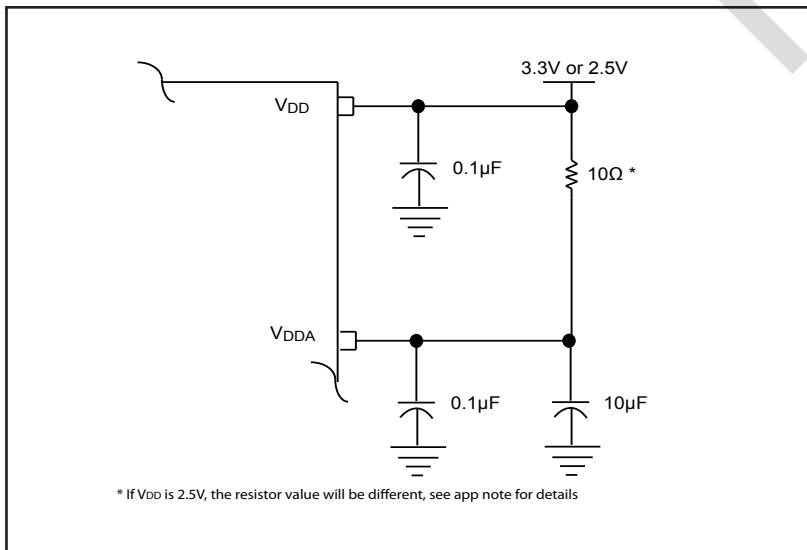


**LVPECL Test Circuit**



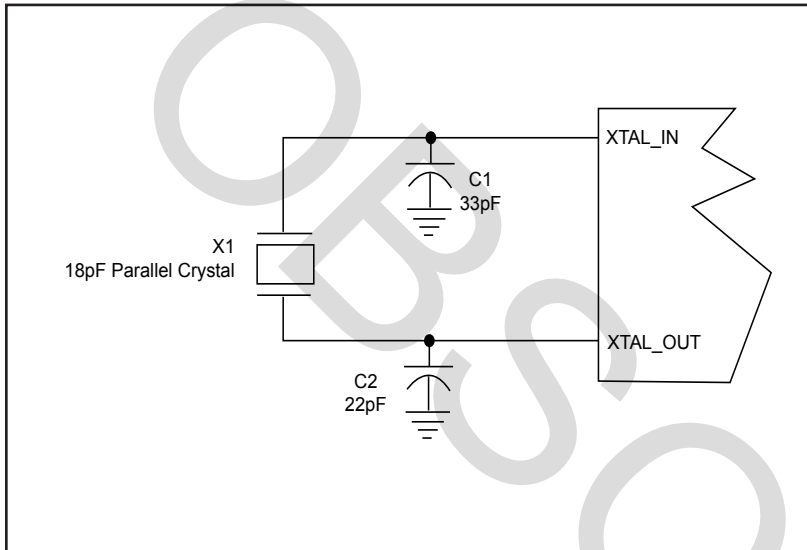
**Power Supply Filtering Techniques**

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$  and  $V_{DDA}$  should be individually connected to the power supply plane through vias, and  $0.1\mu\text{F}$  bypass capacitors should be used for each pin. Figure below illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.



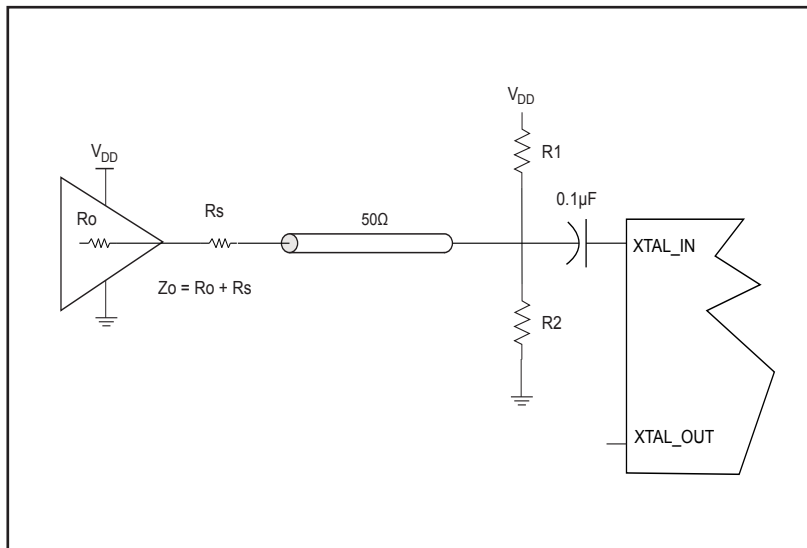
### Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

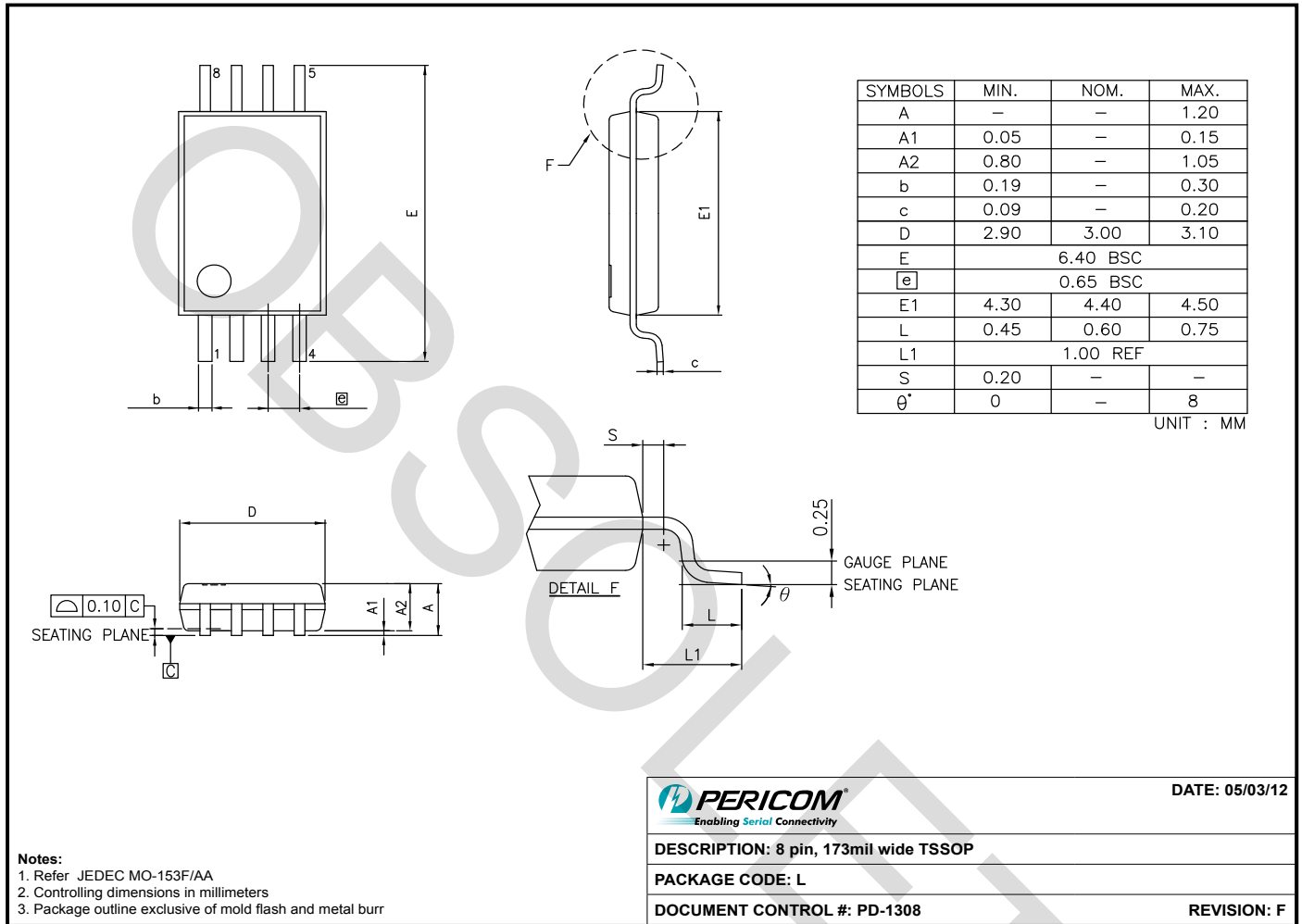


### LVC MOS to XTAL Interface

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



### Packaging Mechanical: 8-Contact TSSOP (L)



**Notes:**  
 1. Refer JEDEC MO-153F/AA  
 2. Controlling dimensions in millimeters  
 3. Package outline exclusive of mold flash and metal burr

<b>PERICOM</b> Enabling Serial Connectivity	DATE: 05/03/12
<b>DESCRIPTION: 8 pin, 173mil wide TSSOP</b>	
<b>PACKAGE CODE: L</b>	
<b>DOCUMENT CONTROL #: PD-1308</b>	<b>REVISION: F</b>

12-0370

### Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6LC48P21LE	L	Pb-free & Green, 8-pin TSSOP	Commercial
PI6LC48P21LIE	L	Pb-free & Green, 8-pin TSSOP	Industrial

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging