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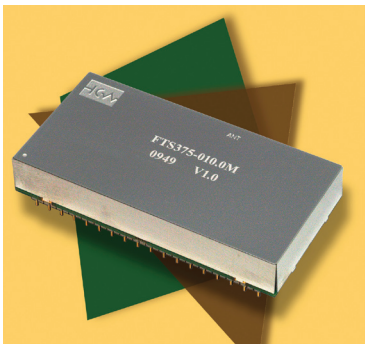
DATA SHEET

125 Series FTS375
Disciplined Reference and Synchronous Clock Generator

CONNOR WINFIELD



Connor-Winfield's GPS Disciplined Oscillators (GPSDOs) were created specifically for all precision timing and synchronization applications requiring higher end, cost sensitive solutions. By combining our uniquely designed GPS timing receivers with our high-quality oscillators, Connor-Winfield is able to offer a wide variety of superior, cost-effective GPS timing solutions. The 125 Series modules provide customer applications with the precise timing capabilities needed to optimize critical system performance.

General Description

The FTS375 module is a GPS driven, mixed-signal phase lock loop, providing a 1 PPS CMOS output from a Connor-Winfield GPS timing receiver. The FTS375 generates a 10 MHz CMOS and a 10 MHz SINE output from an intrinsically low jitter voltage controlled crystal oscillator. The FTS375 can lock to a 10 MHz reference derived from the on-board GPS receiver or an external 10 MHz reference or to an external 1 PPS reference. Alarms are provided to indicate Loss-of-Lock, Holdover, and Antenna Fault. The on-board GPS receiver requires an outdoor mounted GPS antenna for the best stability and consistent performance.

The mode control inputs are used to manually switch between references and/or holdover. The user application should monitor the alarm outputs and manually switch modes as needed.

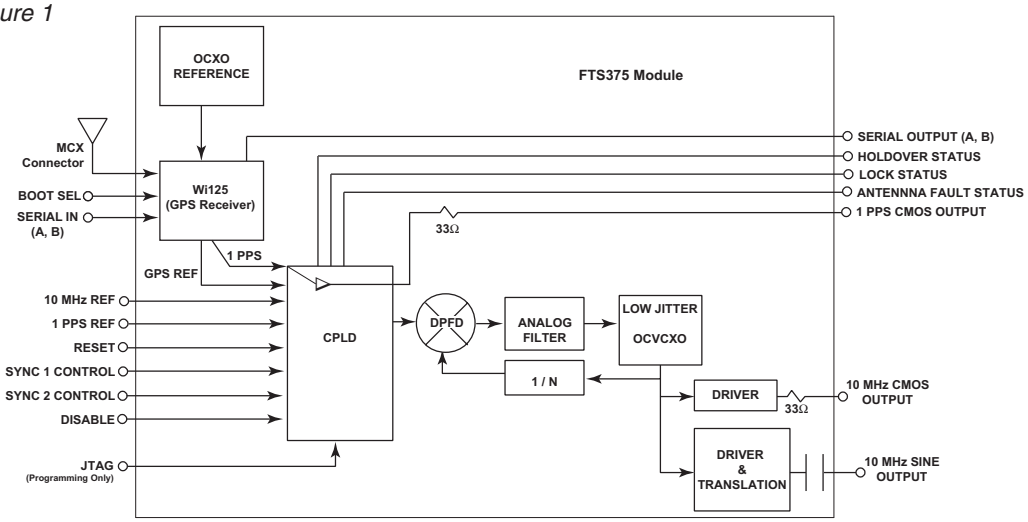
Serial I/O lines provide access to the NMEA messages from the GPS receiver (referenced in the Connor-Winfield's Wi125 User Manual. Contact Connor-Winfield Sales for a copy). The serial I/O lines can be used to access GPS timestamp information, or to verify that the receiver has recovered from an alarm condition. The reset is used to reset the GPS receiver (if needed).

Features

- Phase locked 10 MHz output
- 1 PPS output
- 3 selectable references: GPS, External 10 MHz or External 1 PPS
- Holdover
- Three alarm outputs. (Loss-of-Lock, Holdover and Antenna Fault)
- Serial input and output ports (GPS receiver)
- Master reset
- +3.3 Volt power supply
- Commercial Temp (0-70° C)
- Mechanical Dimensions: 3.937" x 1.969" x 0.708" (100mm x 50mm x 17.98mm)
- Package: 36-pin Through-Hole
- Fixed Position Unit

Functional Block Diagram

Figure 1



Bulletin	SG174
Revision	03
Date	20 Oct 16

Pin Description

Table 1

Pin #	Pin Name	Description	Note
1	1 PPS Ref Input	Externally provided LVCMOS 1 PPS reference	
2	GND	Ground	
3	10 MHz Ref Input	Externally provided LVCMOS 10 MHz reference	
4	No Connect	Used for factory programming	
5	10 MHz CMOS Output	10 MHz low jitter CMOS output	
6	GND	Ground	
7	10 MHz Sine Output	10 MHz AC coupled low jitter SINE output	
8	No Connect	Used for factory programming	
9	No Connect	Used for factory programming	
10	No Connect	Used for factory programming	
11	*Reset	Pull low to reset GPS receiver	
12	TXA	RS-232 transmit signal for UART0	
13	TXB	RS-232 transmit signal for UART1	
14	GND	Ground	
15	RXA	RS-232 receive signal for UART0	
16	RXB	RS-232 receive signal for UART1	
17	GND	Ground	
18	*Bootsel	Normally high. Pull low to reprogram the GPS receiver	
19	GND	Ground	
20	Antenna Supply Voltage	Antenna Supply voltage. Limit continuous current to 45mA	
21	Vcc1	3.3V supply voltage for the GPS circuitry	
22	GND	Ground	
23	Unused	Spare CPLD connection	
24	Unused	Spare CPLD connection	
27	Antenna Fault Status	High = A fault has been detected on pin 20 (Ant Supply Voltage)	
28	1 PPS Out	1 PPS CMOS output	
29	Lock Status	High = Unit is locked to the selected reference	
30	Holdover Status	High = Unit is in holdover	
31	SYNC2 Control	Lock mode control signal	
32	SYNC1 Control	Lock mode control signal	
33	Unused	Spare CPLD connection	
34	*Disable	Pull low to disable the 10 MHz CMOS and SINE outputs	
35	GND	Ground	
36	Vcc2	3.3V supply voltage for PLL and interfacing circuitry	

Note: Vcc1 and Vcc2 should not be connected; otherwise phase noise performance will degrade.

Absolute Maximum Rating

Table 2

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	-0.3	3.7	Volts	1
V_{IN}	Input Voltage	-0.3	4.6	Volts	1
V_{PREAMP}	Antenna Supply Voltage	2.7	13.2	Volts	1
T_S	Storage Temperature	-30	80	°C	1

Operating Specifications

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
$V_{CC}1$	Supply Voltage 1	3.135	3.3	3.465	V	
$I_{CC}1$	Supply Current 1		.480	1.2	A	
$V_{CC}2$	Supply Voltage 2	3.135	3.3	3.465	V	2
$I_{CC}2$	Supply Current 2		.380	1.0	A	
T_O	Temperature Range	0		70	°C	
t_{JTOL}	Input Jitter Tolerance	30			ns	
t_{AQ_GPS}	GPS Input Acquisition Time		150		sec	3
t_{AQ_EXT}	External Input Acquisition Time		120		sec	3
			Oscillator Performance			
F_{CAP}	Capture/Pull-in Range		±45 ppb			
F_{BW}	Jitter Filter Bandwidth		0.1 Hz Typ.			
DC	Duty Cycle		45/55%			
RMS	RMS Phase Noise					
	10 Hz - 2 MHz		1 ps Typ.			
	12 kHz - 2 MHz		0.6 ps Typ.			
			Holdover/Wander Generation Performance			4
T_{STA}	Temperature Stability		±20 ppb			
V_{STA}	Vcc Stability		±5 ppb			
A_{DAILY}	Daily Aging		2 ppb			
A_{YEARLY}	Yearly Aging		80 ppb			
	Wander Generation Specification		ETSI-PRC			

NOTES:

1. *Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the module. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Operating Specifications" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.*
2. *Requires external regulation and supply decoupling.*
3. *Cold Power-up.*
4. *Holdover will be re-calculated with each successful lock. Yearly aging represents 1 continuous year in Holdover.*

Mode Control Table

Table 4

SYNC 1	SYNC 2	Operating Mode
0	0	Force Holdover
0	1	Lock to External 10 MHz reference*
1	0	Lock to External 1 PPS reference
1	1	(Default) Lock to GPS Signal

* Note: Holdover is not supported in this mode; loss of the 10 MHz reference will rail the PLL output until the reference returns or another mode is selected

Input And Output Characteristics

Table 5

LVCMOS Inputs and Outputs

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IH}	High Level Input Voltage	1.7	4.0	V	
V_{IL}	Low Level Input Voltage	-0.5	0.8	V	
V_{OH}	High Level Output Voltage	2.4		V	
V_{OL}	Low Level Output Voltage		0.4	V	
C_O	Output Capacitance		10	pF	

10MHz Sine Output

Symbol	Parameter	Typical	Units	Notes
	Load	50	ohms	
	Output Power	9	dB_m	
	Total Harmonic Distortion	2.2	%	

GPS Receiver Specifications

Table 6

Parameter		Specifications	Notes
Acquisition/Tracking Sensitivity		-155dBm/-156dBm	
Acquisition Time:			
	Hot Start w/ Network Assist	Outdoor: <2 sec Indoor: (-148dBm) <5 sec	
	Stand Alone	Cold: <45 sec Warm: <38 sec Hot: <5 sec Re-acquisition: <1sec (90% confidence)	
Supported Protocols		Network Assist, NMEA 0183	

Reset Generation (I/O pin 11 - RESET)

The power-on-reset for the FTS375 is generated on-board. If it is desired to extend the power-on-reset signal or provide a manual reset of the GPS receiver, pull this signal low.

Antenna Requirements

Table 7

Parameter	Notes
The FTS375 antenna connector is an MCX (female)	
The antenna supply voltage provided to Pin 20 must be within the range of 2.7 to 13.2V (AMR); the antenna must be able to operate at this voltage	
The antenna's continuous current draw must be <=45mA	
The antenna must have a full sky view for optimal receiver performance	
An active antenna with a minimum 10dB gain (including cable loss) should be used	

Standard 125 Series models are designed for fixed position operation only. Contact Connor-Winfield Sales for mobile application model offerings

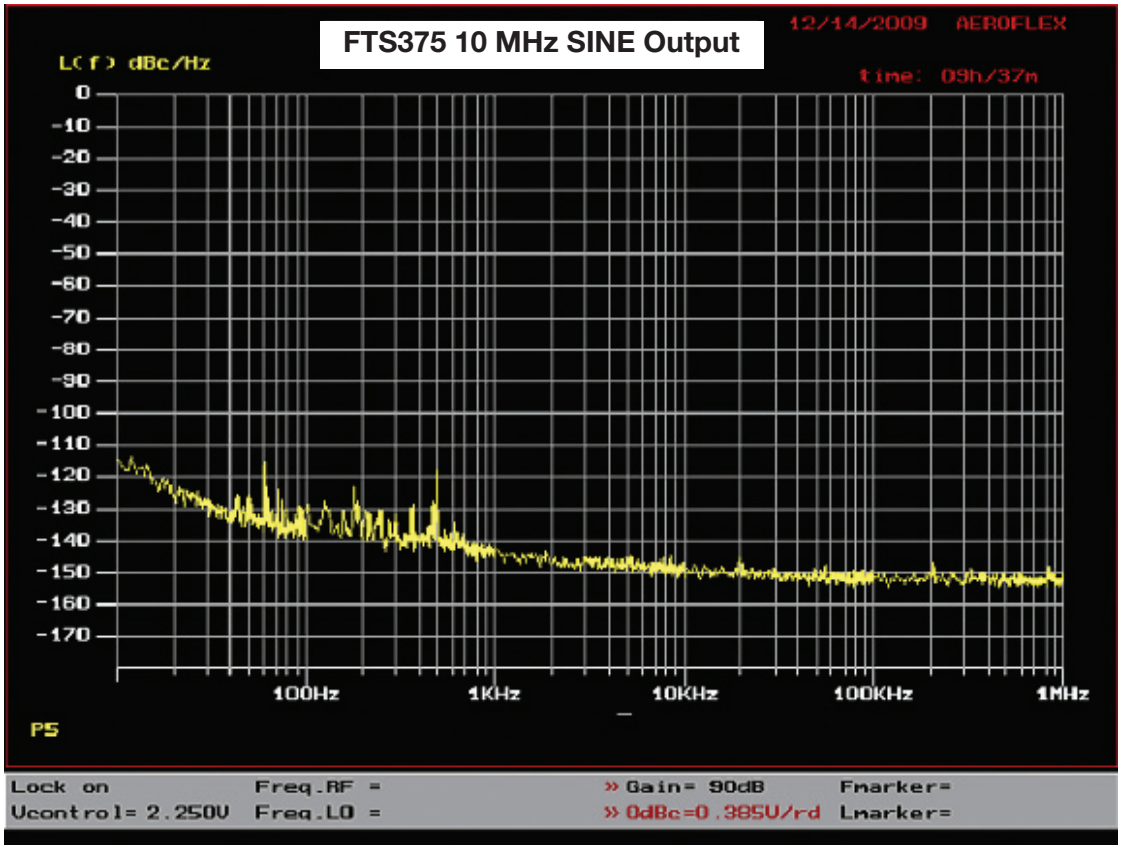
Phase Noise

Figure 2

Phase Noise:

Offset Frequency (Hz)	Typical (dBc / Hz)
10	-115
100	-135
1k	-143
10k	-148
100k	-152
1M	-153

FTS375 Lock to GPS, Sine Output

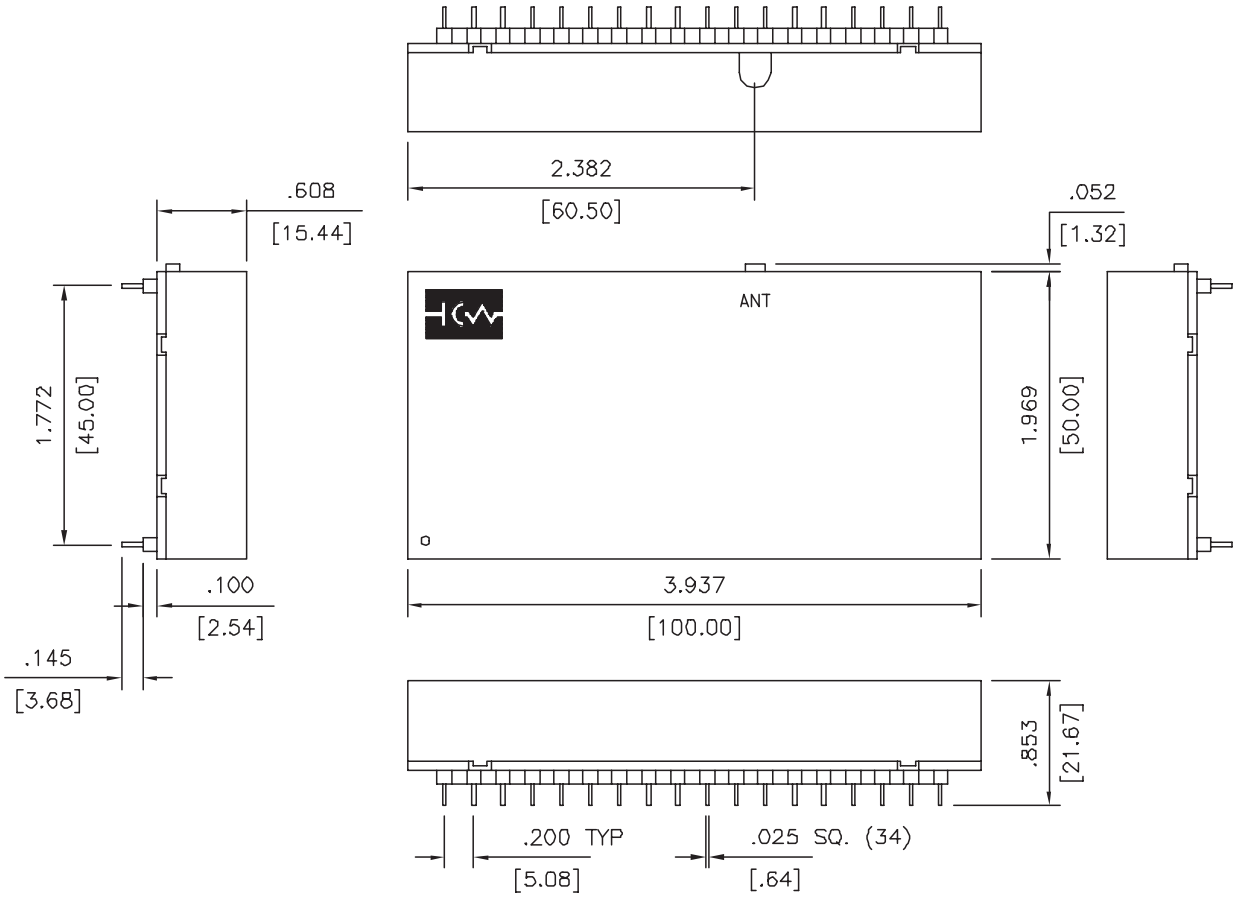


Soldering and Cleaning Recommendations

Hand solder, leaded wave solder, and lead-free wave solder processes are recommended for attaching the FTS375 after reflow processes are complete. Since the FTS375 does not have hermetic enclosure, hand cleaning the leads is recommended and the module should not be completely immersed.

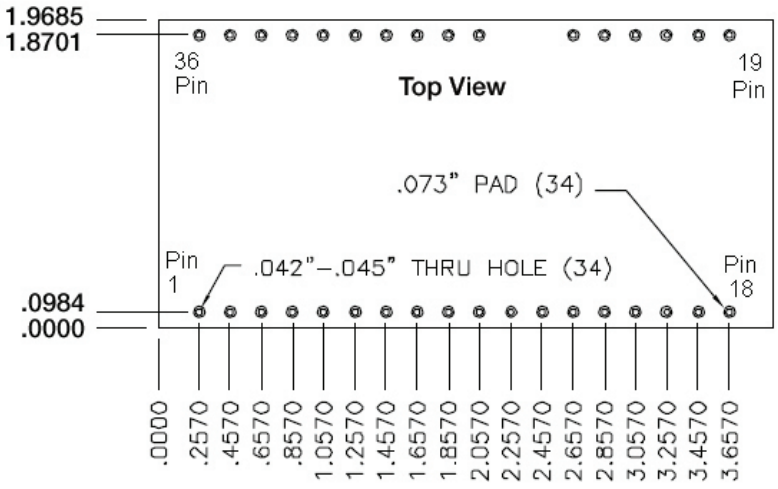
Package Dimensions

Figure 3



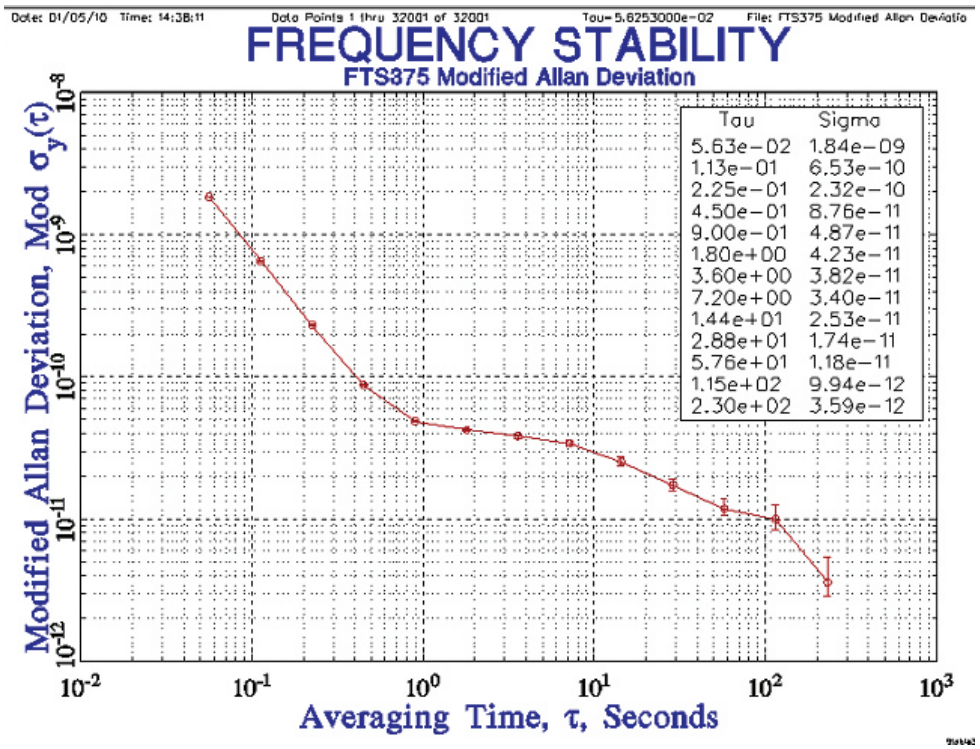
Package Dimensions Top View and Keep out Area

Figure 4



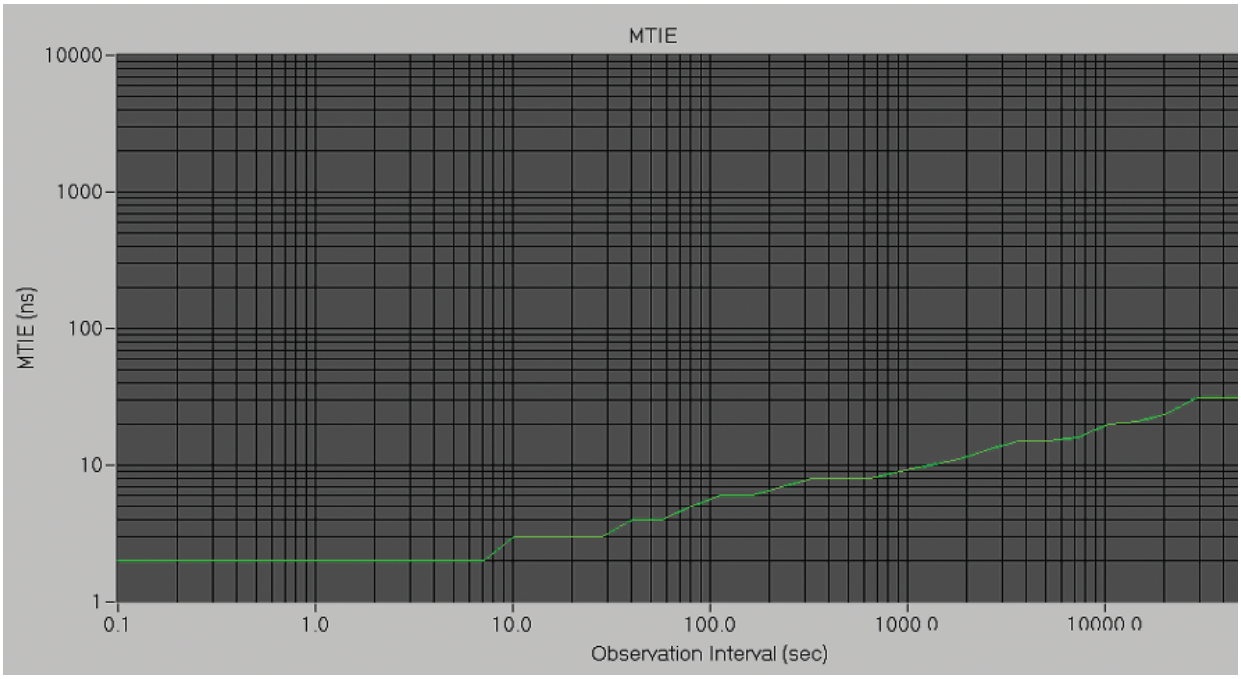
FTS375 Modified Allan Deviation

Figure 5



FTS375 Wander Generation Plot

Figure 6



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Ordering Information

FTS375	-010.0M
	Output Frequency

Revision	Date	Note
P00	1/06/10	Preliminary Release
00	06/16/10	125 Series Update and revise to release
01	05/27/11	Updated Block Diagram with Wi125 Receiver & Soldering Recommendation
02	01/03/12	Added Package Information to Features
03	10/20/16	Added pin numbers to package dimension drawing.