an Intel company

2.5 Gbit/s Clock and Data Recovery GD16547

General Description

The GD16547 is a high performance monolithic integrated *Clock and Data Recovery* (CDR) device applicable for optical communication systems including:

- SDH STM-16
- SONET OC-48

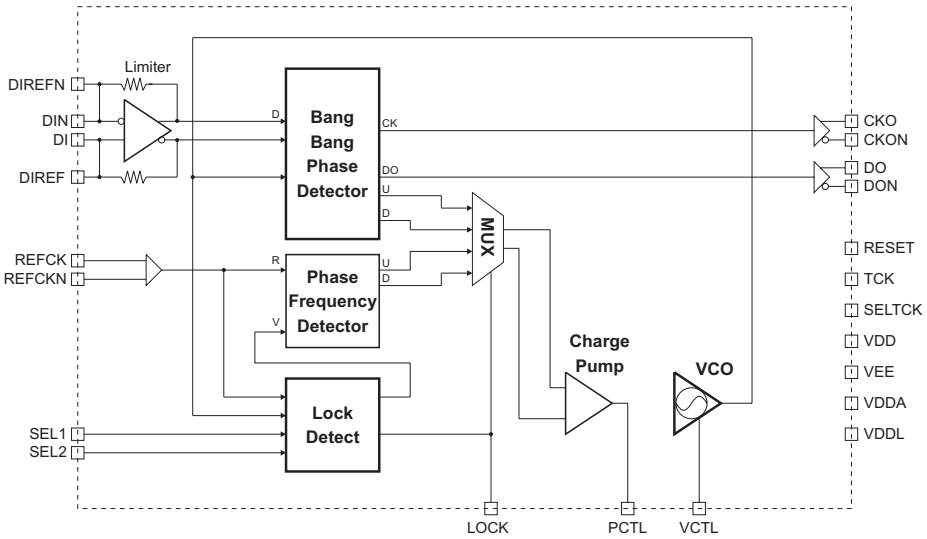
The CDR contains all circuits needed for reliable acquisition and lock of the VCO phase to the incoming data-stream.

The electrical input sensitivity is better than 8 mV (BER <10^{-10}). Optical receivers with sensitivity better than -34 dBm have been obtained without optical pre-amplifiers.

The device meets all ITU-T jitter requirements when used with the recommended loop filter (jitter tolerance, -transfer and -generation).

The 2.5 GHz output clock is maintained within 500 ppm tolerance even in absence of data.

The GD16547 is available in a 48 lead 7 × 7 mm TQFP power enhanced plastic package.



Features

- Clock and Data Recovery for 2.488 Gbit/s.
- SDH STM-16, SONET OC-48 compatible.
- Differential Data inputs with 8 mV sensitivity.
- Differential ECL Data and Clock outputs.
- Acquisition time: < 500 μs.
- Few external passive components needed.
- 50 Ω Loop-through data inputs for higher sensitivity.
- Single supply operation: -5 V.
- Power dissipation: less than 1 W.
- Available in a 48 lead 7 × 7 mm TQFP plastic package

Applications

- Clock and Data Recovery for optical communication systems including:
  - SDH STM-16
  - SONET OC-48

Functional Details

The main application of the GD16547 is as a receiver for:

- SDH STM-16
- SONET OC-48 optical communication systems.

It integrates:

- a Voltage Controlled Oscillator (VCO)
- a Lock Detect Circuit
- a Frequency Detector (PFD)
- a Bang-Bang Phase Detector

into a *Phase Locked Loop* (PLL) - based clock and data recovery circuit with differential ECL data and clock outputs.

VCO

The VCO is a low noise LC-type differential oscillator with a tuning range from 2.3 to 2.7 GHz. Tuning is done by applying a voltage to the VCTL pin.

Lock Detect Circuit

The lock detect circuit continuously monitors the difference between the reference clock and the divided VCO clock. If the reference clock and the divided VCO frequency differs by more than 500 ppm (or 2000 ppm, selectable), it switches the PFD into the PLL in order to pull the VCO back inside the lock-in range. This mode is called **the acquisition mode**.

The PFD is used to ensure predictable lock up conditions for the GD16547 by locking the VCO to an external reference clock source. It is only used during acquisition and pulls the VCO into the lock range where the Bang-Bang phase detector is capable of acquiring lock. The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic.

Once the VCO is inside the lock-range the lock-detection circuit switches the Bang-Bang phase detector into the PLL in order to lock to the data signal. This mode is called **CDR mode**.

The reference clock input, REFCK, to the PFD is at 1/64 of the data rate.

Bang-Bang Phase Detector

The Bang-Bang phase detector is used in **CDR mode** as a true digital type detector, producing a binary output. It samples the incoming data twice each bit period: once in the transition of the (previous) bit period and once in the middle of the bit period. When a transition occurs between 2 consecutive bits - the value of the sample in the transition between the bits will show whether the VCO clock leads or lags the data. Hence the PLL is controlled by the bit transition point, thereby ensuring that data is sampled in the middle of the eye, once the system is in CDR mode. The external loop filter components control the characteristics of the PLL.

The binary output of either the PFD or the Bang-Bang phase detector (depending of the mode of the lock-detection circuit) is fed to a charge pump capable of sinking or sourcing current or tristating. The output of the charge pump is filtered through the loop filter and controls the tune-voltage of the VCO.

As a result of the continuous monitoring lock-detect circuit the VCO frequency never deviates more than 500 ppm (2000 ppm) from the reference clock before the PLL is considered to be 'Out of Lock'. Hence the acquisition time is predictable and short and the output clock CKOUT is always kept within the 500 ppm (2000 ppm) limits, ensuring safe clocking of down stream circuitry.

The LOCK Signal

The status of the lock-detection circuit is given by the LOCK signal. In CDR mode LOCK is steady high. In acquisition mode LOCK is alternating indicating the continuous shifts between the Bang-Bang Detector (high) and the PFD (low).

The LOCK output may be used to generate *Loss Of Signal* (LOS). The time for LOCK to assert is predictable and short, equal to the time to go into lock, but the time for LOCK to de-assert must be considered. When the line is down (i.e. no information received) the optical receiver circuit may produce random noise. It is possible that this random noise will keep the GD16547 within the 500 ppm (2000 ppm) range of the line frequency, hence LOCK will remain asserted for a non-deterministic time. This may be prevented by injecting a small current at the loop filter node, which actively pulls the PLL out of the lock range when the output of the phase detector acts randomly.

The negligible penalty paid is a static phase error on the sampling time in the decision gate. However, due to the nature of the phase detector the error will be small (few degrees), forcing the loop to be at one edge of the error-function shaped transfer characteristic of the detector.

Inputs

The input amplifier (pins DI / DIN) is designed as a limiting amplifier with a sensitivity better than 8 mV (differential).

The inputs may be either AC or DC coupled. In both cases input termination is made through pins DIREF / DIREFN. If the inputs are AC coupled the amplifier features an internal offset cancelling DC feedback. Notice that the offset cancellation will only work when the input is differential and AC-coupled as shown in the Figures on page 3.

Following the CDR block the data is output together with a 2.5 GHz clock. The data and clock outputs are differential ECL outputs that should be terminated via 50 Ω to -2 V.

Package

The GD16547 is provided in a 48 lead power enhanced TQFP.

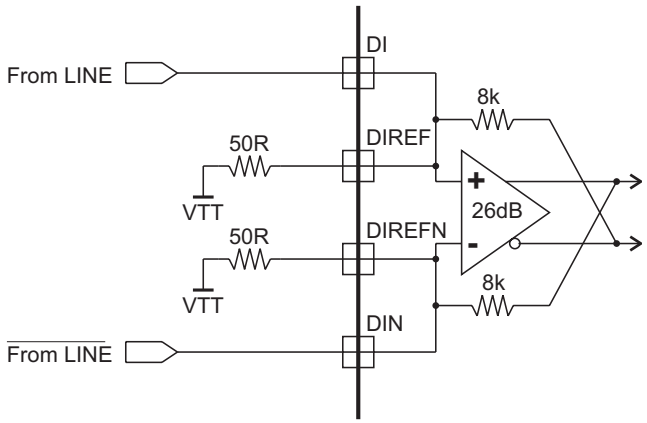


Figure 1. *DC Coupled Input (Ignoring internal offset compensation)*

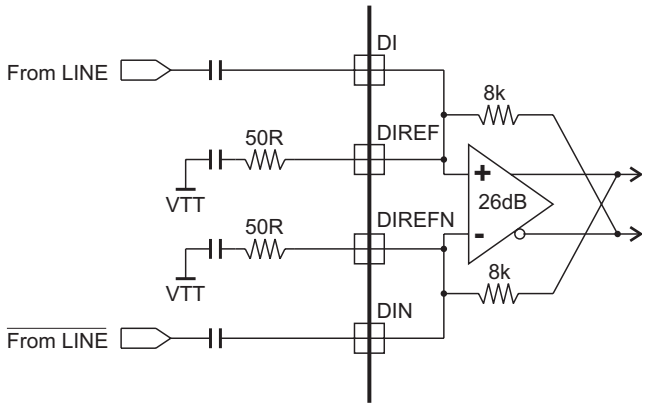


Figure 2. *AC Coupled Input (Using internal offset compensation)*

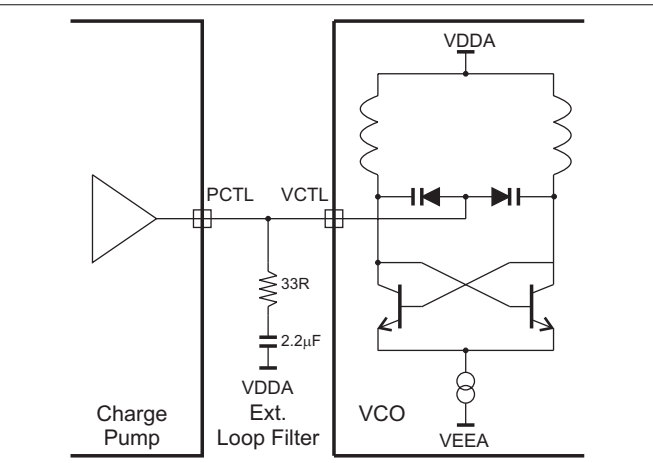


Figure 3. *Loop Filter*

Pin List

Mnemonic:	Pin no.:	Pin Type:	Description:
DO, DON	31, 32	ECL OUT	Data output, differential 2.5 Gbit/s.
REFCK, REFCKN	18 19	ECL IN	Differential 38 MHz reference clock input.
SEL1, SEL2	16, 15	ECL IN	Clock and Data recovery set-up. SEL1 SEL2 0 0 Auto lock, 500 ppm. 0 1 Auto Lock, 2000 ppm. 1 0 Manual Phase Freq. detector PFC. 1 1 Manual Bang-Bang phase detector.
DI, DIN	8, 6	Data IN	Differential AC or DC coupled 2.5 Gbit/s Data input.
DIREF, DIREFN	9 5	Termination	Termination for DI and DIN. Normally terminated to VDD through 47 nF. For DC connected inputs connect to reference voltage.
CKO, CKON	29, 28	ECL OUT	Clock output, differential 2.5 GHz.
LOCK	22	ECL OUT	Lock-detect output. When low, the divided VCO frequency deviates more than 500/2000 ppm from REFCK / REFCKN.
PCTL	42	Analog OUT	Charge pump control.
VCTL	46	Analog IN	VCO voltage control input.
RESET	21	ECL IN	Not needed on power up. Connect to VEE. Only used for test purposes.
TCK	38	ECL IN	Leave open for normal operation. Only used at DC test.
SELTCK	35	ECL IN	Test-clock select. Connect to VDD for normal operation. Only used for test purposes.
VDD	1, 7, 12, 13, 24, 25, 27, 30, 33, 36, 37, 48	PWR	Positive supply voltage.
VDDA	44, 47	PWR	Positive supply voltage for PLL section.
VDDL	4, 11	PWR	Positive supply voltage.
VEE	2, 10, 14, 17, 26, 34, 39, 43, 45	PWR	Negative supply voltage.
NC	3, 20, 23, 40, 41	NC	Not connected.
Heat sink			Connected to VDD.

Pin Outline

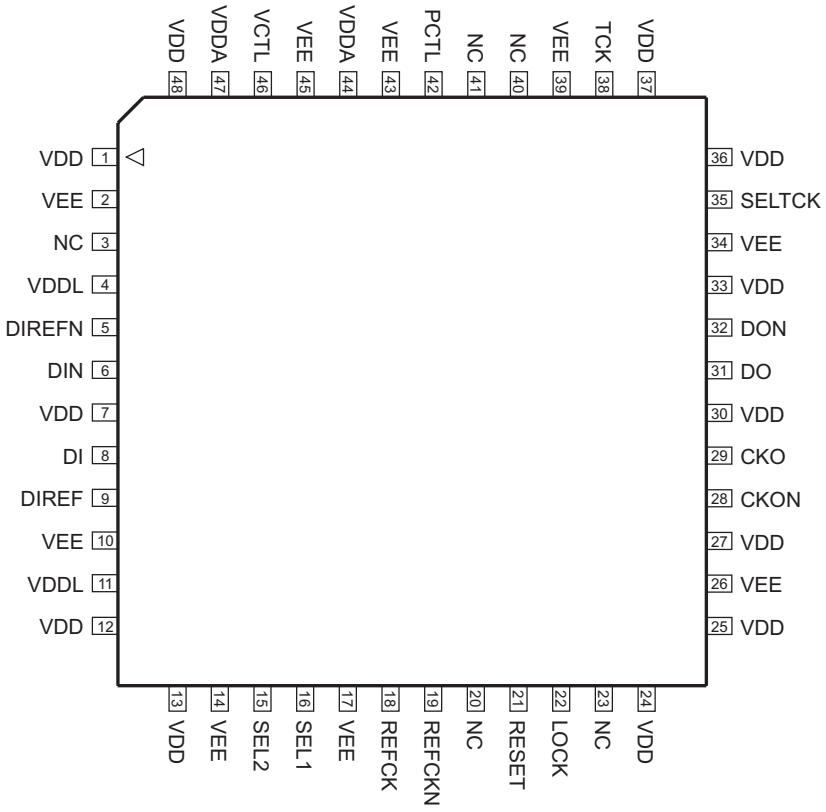


Figure 4. *48 Lead TQFP, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to VDD.
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
V_{EE}, V_{EEA}	Supply voltage		-6		0	V
V_0 *MAX*	Output voltage		V_{EE} - 0.5		0.5	V
I_0 *MAX, ECL*	Output current				30	mA
I_0 *MAX, PCTL*	Output current				0.5	mA
V_I *MAX*	Input voltage		V_{EE} - 0.5		0.5	V
I_I *MAX*	Input current		-1.0		1.0	mA
T_0	Operating temperature	Junction	-55		125	°C
T_S	Storage temperature		-65		150	°C

DC Characteristics

T_{CASE} = -5 °C to 95 °C, V_{EE} = -4.5 V to -5.5 V

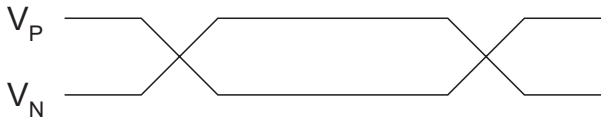
All voltages in the table are referred to VDD.
All inputs signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristlcs:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Supply voltage		-5.50	-5.0	-4.5	V
I_{EE}	Supply current			180	240	mA
$V_{diff\ DI/DIN}$	Data sensitivity, differential/single-ended	Note 1, 5		5	8	mV
$V_{diff\ DI/DIN}$	Necessary input amplitude to stay locked	Note 1, 5		2	3	mV
$V_{diff\ MAX,\ DI/DIN}$	Maximum input voltage, differential	Note 7			500	mV
$V_{CM\ DI/DIN}$	Data common mode	Note 6	-2	-1.3	-1	V
$V_{IH\ ECL}$	ECL input high voltage		-1.1		0	V
$V_{IL\ ECL}$	ECL input low voltage		V_{EE}		-1.5	V
$I_{IH\ ECL}$	ECL input high current	V_I = -1.1 V			30	µA
$I_{IL\ ECL}$	ECL input low current	V_I = -1.5 V			30	µA
$V_{1\ VCTL}$	VCO control voltage	I_{VCTL} < 30 µA	V_{EE}		-1	V
$V_{OH\ ECL}$	ECL output high voltage	Note 2, T_{CASE} =-40 °C	-1.1		-1	V
$V_{OH\ ECL}$	ECL output high voltage	Note 2, T_{CASE} =25 °C	-1.02		-0.91	V
$V_{OH\ ECL}$	ECL output high voltage	Note 2, T_{CASE} =85 °C	-0.94		-0.82	V
$V_{OL\ ECL}$	ECL output low voltage	Note 2, T_{CASE} =-40 °C	V_{TT}		-1.7	V
$V_{OL\ ECL}$	ECL output low voltage	Note 2, T_{CASE} =25 °C	-1.97		-1.62	V
$V_{OL\ ECL}$	ECL output low voltage	Note 2, T_{CASE} =85 °C	-1.92		-1.56	V
$V_{PP\ ECL}$	ECL output amplitude, peak to peak	Note 2, 8	650	800	1150	mV
$I_{OH\ PCTL}$	Source current	Note 3	85	100		µA
$I_{OL\ PCTL}$	Sink current	Note 3	-85	-100		µA

Note 1: AC-coupled, p-p voltage for differential coupling, BER 10^{-10}
Data eye diagram in accorcance with ITU G.957, 2^{23} -1 PRBS, terminated via loop through 50 Ω.
Note 2: V_{TT} = -2.0 V ±5 %.
Note 3: R_L = 50 Ω to V_{TT}.
Note 4: Output terminated to -2.5 V during test.

Note 5: $V_{diff} = \left| V_P - V_N \right|$.

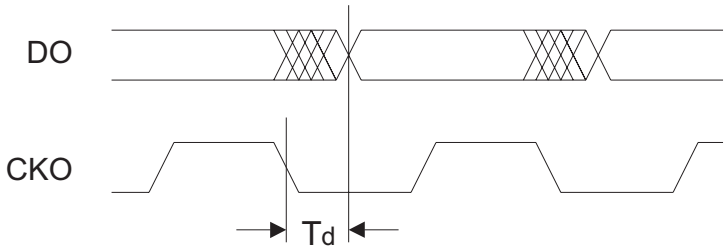
Note 6: $V_{CM} = \frac{V_P + V_N}{2}$.



Note 7: AC coupled input, p-p voltage.
Note 8: Guaranteed swing within V_{OH}/V_{OL} range.

AC Characteristics

T_{CASE} = -5 °C to 95 °C, V_{EE} = -4.5 to -5.5 V



Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
J_{TOL}	Jitter tolerance Note 1, 2. See Figure 5.	f < 100 kHz f > 1 MHz	1.5 0.15	>2 >0.35		UI_{p-p} UI_{p-p}
J_{TRF}	Jitter transfer/Jitter gain Note 1. See Figure 6.	f < 2 MHz		0.08	0.1	dB
J_{OUT}	Output clock intrinsic jitter Note 1, 2	5 kHz < f < 20 MHz 1 MHz < f < 20 MHz 5 kHz < f < 20 MHz			0.125 0.05 0.01	UI_{p-p} UI_{p-p} UI_{RMS}
T_A	Acquisition time	2^{23} – 1 PRBS		50	500	µs
L_{CID}	Consecutive identical bits	# of bits with no transistion	400	1000		bits
D_C	Input data / REFCK frequency deviation	Note 3	-200		200	ppm
$C_{DUTY, REFCK}$	REFCK clock duty cycle	Vthr = -1.3 V	40		60	%
F_{VCO}	VCO tuning range		2.3	2.488	2.7	GHz
$C_{DUTY, CKO}$	Output clock duty cycle	Vthr = -1.3 V, 50 Ω to -2.0 V	45		55	%
$T_{RISE/FALL, DO/DON}$	ECL output rise/fall time	20 - 80%, 50 Ω to -2.0 V		120	160	ps
$T_{RiISE/FALL, CKO/CKON}$	ECL output rise/fall time	80 - 20%, 50 Ω to -2.0 V		100	120	ps
$T_{D, DO}$	Data output from CKO	See figure above	20	50	100	ps

Note 1: Jitter parameters acquired at V_{EE} = 5.0 V ±5 %, R = 33 Ω, and C = 2.2 µF.
When shifting the V_{EE} range and tolerance, R and C values should be changed to accommodate for changed loop gain parameters.
Note 2: 1 UI_{p-p} = 402 ps.
Note 3: Maximum allowable deviation between reference clock and divided VCO clock when locked to data.

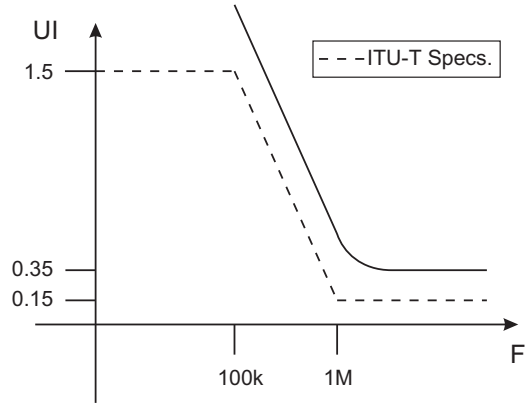


Figure 5. *Jitter Tolerance, Typical*

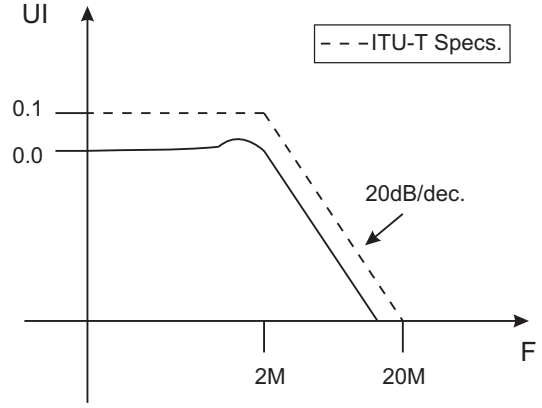
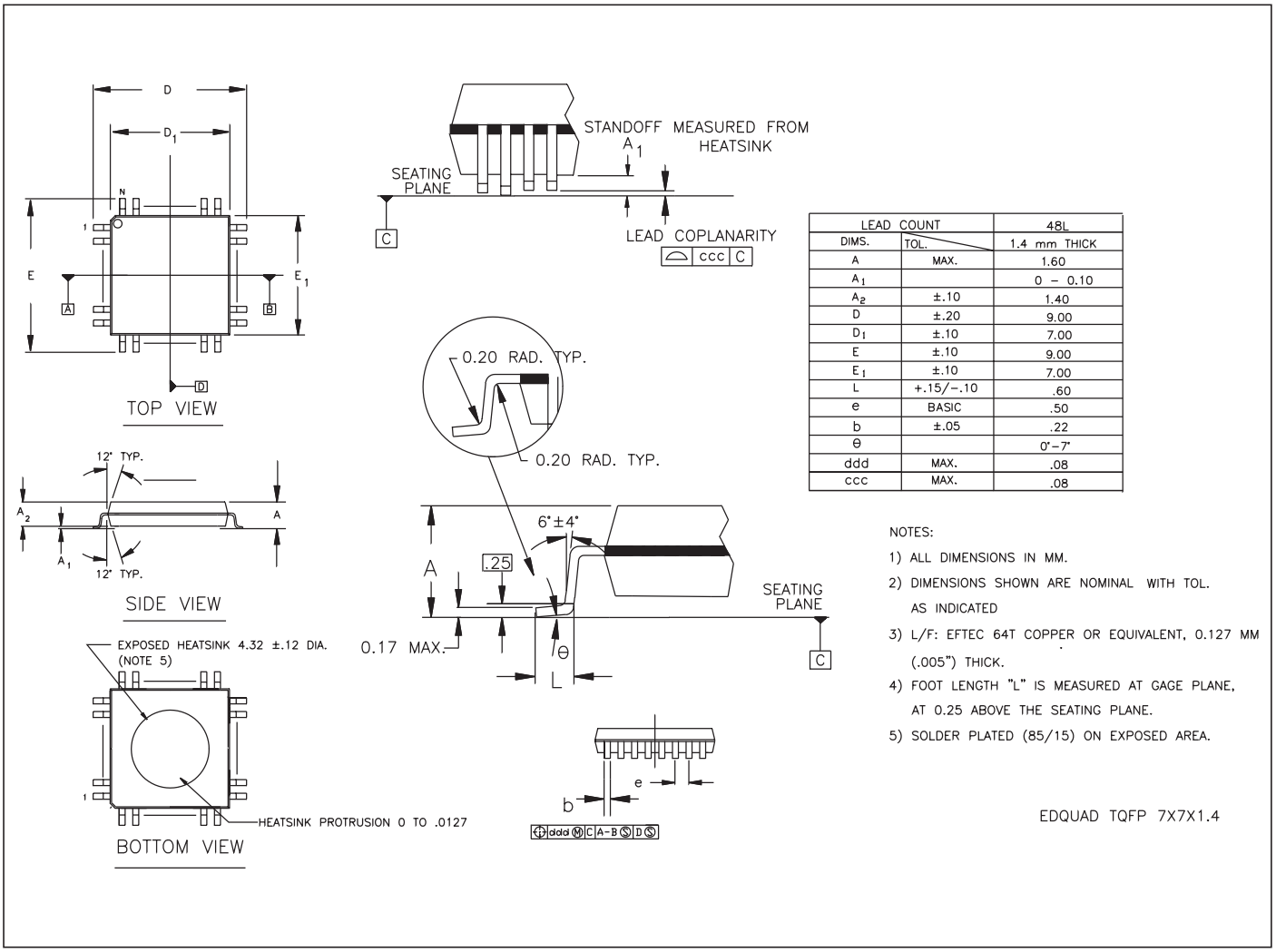


Figure 6. *Jitter Transfer, Typical*

Package Outline



LEAD COUNT		48L
DIMS.	TOL.	1.4 mm THICK
A	MAX.	1.60
A_1		0 – 0.10
A_2	±.10	1.40
D	±.20	9.00
D_1	±.10	7.00
E	±.10	9.00
E_1	±.10	7.00
L	+.15/–.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ddd	MAX.	.08
ccc	MAX.	.08

Figure 7. *48 Lead TQFP, Power Enhanced (All Dimensions are mm)*

External References

ITU-T G.825 (03/93) Control of Jitter and Wander within digital networks based on SDH
ITU-T G.957 (07/95) Optical interfaces for equip. and systems relating to SDH
ITU-T G.958 (11/94) Digital line systems based on SDH for use on optical fibre cables

Device Marking

Figure 8. *Device Marking, Top View*

Ordering Information

To order, please specify as shown below:

Product Name:	Intel Order Number:	Package Type:	Case Temperature Range:
GD16547-48BA	**FAGD1654748BA** MM#: 836072	48 lead TQFP, EDQUAD	-5..95 °C

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