

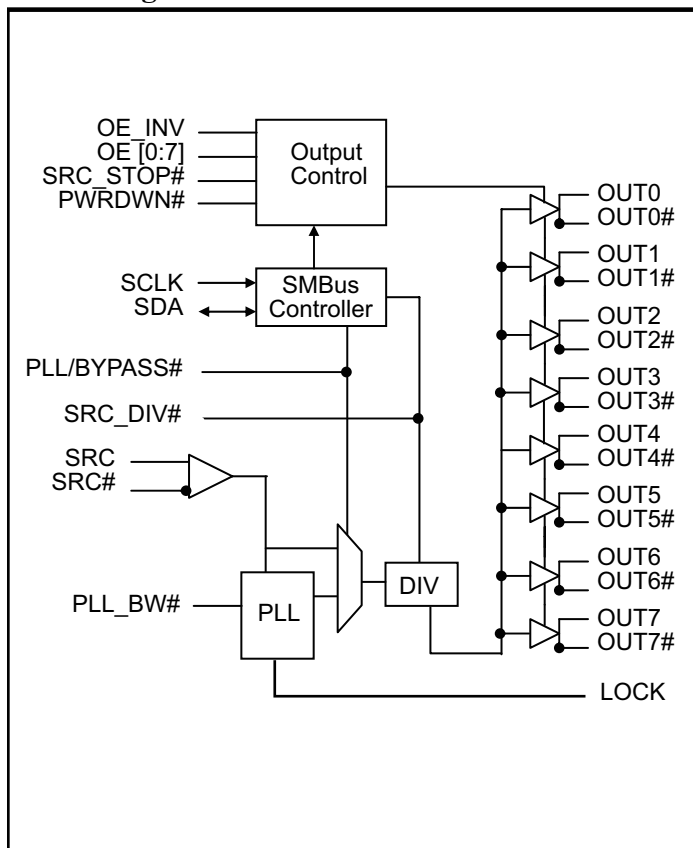
Features

- Phase jitter filter for PCIe® application
- Eight Pairs of Differential Clocks
- Low skew < 50ps (PI6C20800S), <60ps (PI6C20800SI)
- Low Cycle-to-cycle jitter < 70ps
- Output Enable for all outputs
- Outputs Tristate control via SMBus
- Power Management Control
- Programmable PLL Bandwidth
- PLL or Fanout operation
- 3.3V Operation
- Industrial Temperature Option - PI6C20800SI
- Packaging (Pb-Free & Green):
 - 48-Pin SSOP (V)
 - 48-Pin TSSOP (A)

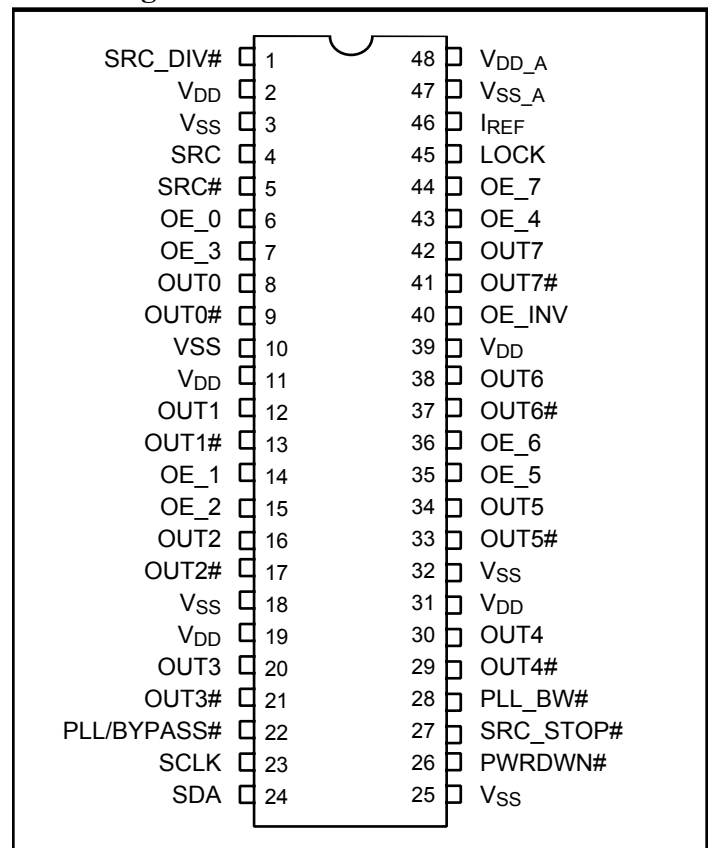
Description

PI6C20800S is a PCI Express®, high-speed, low-noise differential clock buffer designed to be a companion to PI6C410BS PCI Express clock generator for Intel server chipsets. The device distributes the differential SRC clock from PI6C410BS to eight differential pairs of clock outputs either with or without PLL. The input SRC clock can be divided by 2 when SRC_DIV# is LOW. The clock outputs are controlled by input selection of SRC_STOP#, PWRDWN# and SMBus, SCLK and SDA. When input of either SRC_STOP# or PWRDWN# is LOW, the output clocks are Tristated. When PWRDWN# is LOW, the SDA and SCLK inputs must be Tristated.

Block Diagram



Pin Configuration



Pin Descriptions

| Pin Name | Type | Pin # | Descriptions |
|----------------------|--------|---|--|
| SRC_DIV# | Input | 1 | 3.3V LVTTTL input for selecting input frequency divide by 2, active LOW. |
| SRC & SRC# | Input | 4, 5 | 0.7V Differential SRC input from PI6C410 clock synthesizer |
| OE [0:7] | Input | 6, 7, 14, 15, 35, 36, 43, 44 | 3.3V LVTTTL input for enabling outputs, active HIGH. |
| OE_INV | Input | 40 | 3.3V LVTTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins. When 0 = same stage When 1 = OE[0:7], SRC_STOP#, PWRDWN# inverted. |
| OUT[0:7] & OUT[0:7]# | Output | 8, 9, 12, 13, 16 17, 20, 21, 29, 30, 33, 34, 37, 38, 41, 42 | 0.7V Differential outputs |
| PLL/BYPASS# | Input | 22 | 3.3V LVTTTL input for selecting fan-out of PLL operation. |
| SCLK | Input | 23 | SMBus compatible SCLOCK input |
| SDA | I/O | 24 | SMBus compatible SDATA |
| I _{REF} | Input | 46 | External resistor connection to set the differential output current |
| SRC_STOP# | Input | 27 | 3.3V LVTTTL input for SRC stop, active LOW |
| PLL_BW# | Input | 28 | 3.3V LVTTTL input for selecting the PLL bandwidth |
| PWRDWN# | Input | 26 | 3.3V LVTTTL input for Power Down operation, active LOW |
| LOCK | Output | 45 | 3.3V LVTTTL output, transition high when PLL lock is achieved (Latched output) |
| V _{DD} | Power | 2, 11, 19, 31, 39 | 3.3V Power Supply for Outputs |
| V _{SS} | Ground | 3, 10, 18, 25, 32 | Ground for Outputs |
| V _{SS_A} | Ground | 47 | Ground for PLL |
| V _{DD_A} | Power | 48 | 3.3V Power Supply for PLL |

Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | W/R |
|----|----|----|----|----|----|----|-----|
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0/1 |

Data Write Protocol⁽¹⁾

| | | | | | | | | | | | | |
|-----------|------------|---|-----|-----------------|-----|----------------|-----|------------------|-----|-----------------|-----|----------|
| 1 bit | 7 bits | 1 | 1 | 8 bits | 1 | 8 bits | 1 | 8 bits | 1 | 8 bits | 1 | 1 bit |
| Start bit | Slave Addr | W | Ack | Register offset | Ack | Byte Count = N | Ack | Data Byte Offset | Ack | Data Byte N - 1 | Ack | Stop bit |

Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Read Protocol(2)

| | | | | | | | | | | | | | | | | |
|-----------|------------|---|-----|-----------------|-----|--------------|------------|---|-----|----------------|-----|------------------|-----|-----------------|---------|----------|
| 1 bit | 7 bits | 1 | 1 | 8 bits | 1 | 1 | 7 bits | 1 | 1 | 8 bits | 1 | 8 bits | 1 | 8 bits | 1 | 1 bit |
| Start bit | Slave Addr | W | Ack | Register offset | Ack | Repeat Start | Slave Addr | R | Ack | Byte Count = N | Ack | Data Byte Offset | Ack | Data Byte N - 1 | Not Ack | Stop bit |

Note:

- Register offset for indicating the starting register for indexed block write and indexed block read.

Data Byte 0: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Pin |
|-----|---|------|-------------------------|---------------------|-----|
| 0 | SRC_DIV# 0 = Divide by 2 1 = Normal | RW | 1 = x1 | OUT[0:7], OUT[0:7]# | NA |
| 1 | PLL/BYPASS# 0 = Fanout 1 = PLL | RW | 1 = PLL | OUT[0:7], OUT[0:7]# | NA |
| 2 | PLL Bandwidth 0 = HIGH Bandwidth, 1 = LOW Bandwidth | RW | 1 = Low | OUT[0:7], OUT[0:7]# | NA |
| 3 | RESERVED | | | | |
| 4 | RESERVED | | | | |
| 5 | RESERVED | | | | |
| 6 | SRC_STOP# 0 = Driven when stopped 1 = Tristate | RW | 0 = Driven when stopped | OUT[0:7], OUT[0:7]# | |
| 7 | PWRDWN# 0 = Driven when stopped 1 = Tristate | RW | 0 = Driven when stopped | OUT[0:7], OUT[0:7]# | NA |

Data Byte 1: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Pin |
|-----|---|------|--------------------|--------------------|-----|
| 0 | OUTPUTS enable 1 = Enabled 0 = Disabled | RW | 1 = Enabled | OUT0, OUT0# | NA |
| 1 | | RW | 1 = Enabled | OUT1, OUT1# | NA |
| 2 | | RW | 1 = Enabled | OUT2, OUT2# | NA |
| 3 | | RW | 1 = Enabled | OUT3, OUT3# | NA |
| 4 | | RW | 1 = Enabled | OUT4, OUT4# | NA |
| 5 | | RW | 1 = Enabled | OUT5, OUT5# | NA |
| 6 | | RW | 1 = Enabled | OUT6, OUT6# | NA |
| 7 | | RW | 1 = Enabled | OUT7, OUT7# | NA |

Data Byte 2: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Pin |
|-----|--|------|--------------------|--------------------|-----|
| 0 | Allow control of OUTPUTS with assertion of SRC_STOP# 0 = Free running 1 = Stopped with SRC_Stop# | RW | 0 = Free running | OUT0, OUT0# | NA |
| 1 | | RW | 0 = Free running | OUT1, OUT1# | NA |
| 2 | | RW | 0 = Free running | OUT2, OUT2# | NA |
| 3 | | RW | 0 = Free running | OUT3, OUT3# | NA |
| 4 | | RW | 0 = Free running | OUT4, OUT4# | NA |
| 5 | | RW | 0 = Free running | OUT5, OUT5# | NA |
| 6 | | RW | 0 = Free running | OUT6, OUT6# | NA |
| 7 | | RW | 0 = Free running | OUT7, OUT7# | NA |

Data Byte 3: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Pin |
|-----|--------------|------|--------------------|--------------------|-----|
| 0 | RESERVED | RW | | | |
| 1 | | RW | | | |
| 2 | | RW | | | |
| 3 | | RW | | | |
| 4 | | RW | | | |
| 5 | | RW | | | |
| 6 | | RW | | | |
| 7 | | RW | | | |

Data Byte 4: Pericom ID Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Pin |
|-----|--------------|------|--------------------|--------------------|-----|
| 0 | Pericom ID | R | 0 | NA | NA |
| 1 | | R | 0 | NA | NA |
| 2 | | R | 0 | NA | NA |
| 3 | | R | 0 | NA | NA |
| 4 | | R | 0 | NA | NA |
| 5 | | R | 1 | NA | NA |
| 6 | | R | 0 | NA | NA |
| 7 | | R | 0 | NA | NA |

Functionality

| PWRDWN# | OUT | OUT# | SRC_Stop# | OUT | OUT# |
|---------|-----------------------------|--------|-----------|-----------------------------|--------|
| 1 | Normal | Normal | 1 | Normal | Normal |
| 0 | $I_{REF} \times 2$ or Float | LOW | 0 | $I_{REF} \times 6$ or Float | LOW |

Power Down (PWRDWN# assertion)

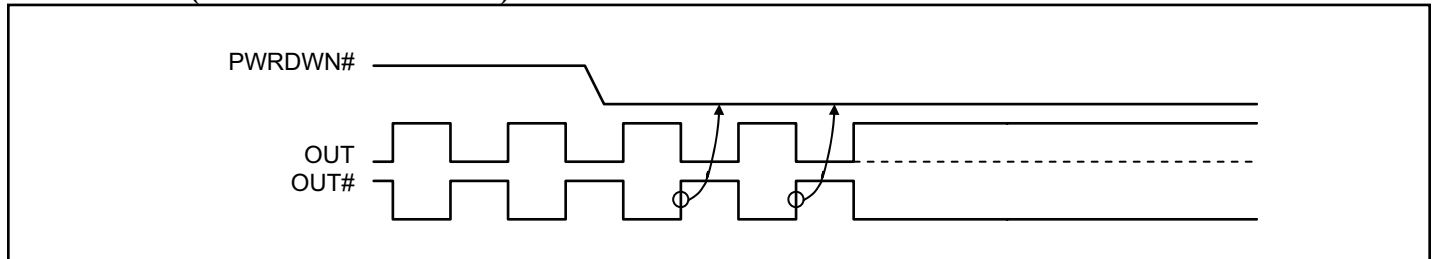


Figure 1. Power down sequence

Power Down (PWRDWN# De-assertion)

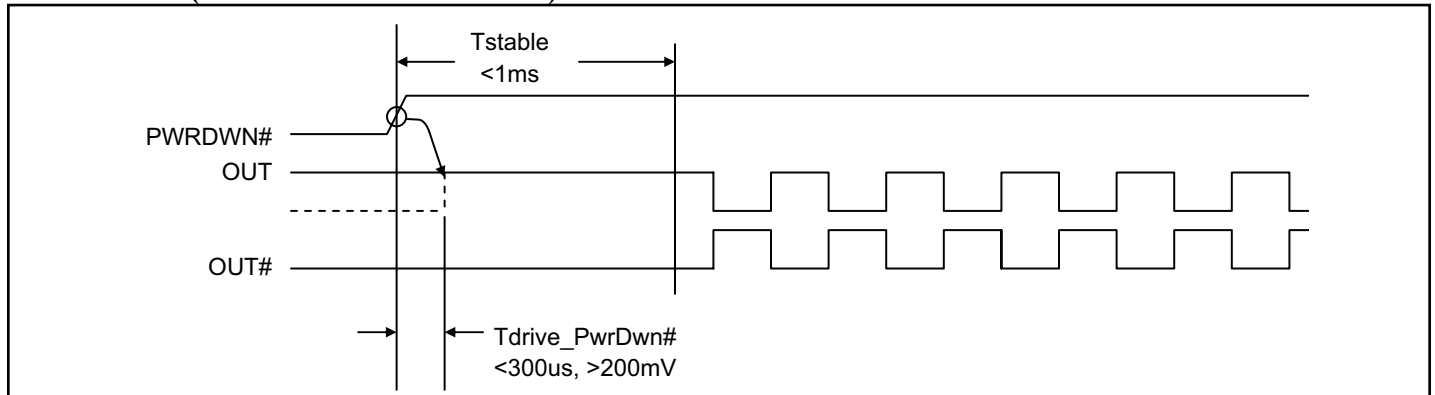


Figure 2. Power down de-assert sequence

Current-mode output buffer characteristics of OUT[0:7], OUT[0:7]#

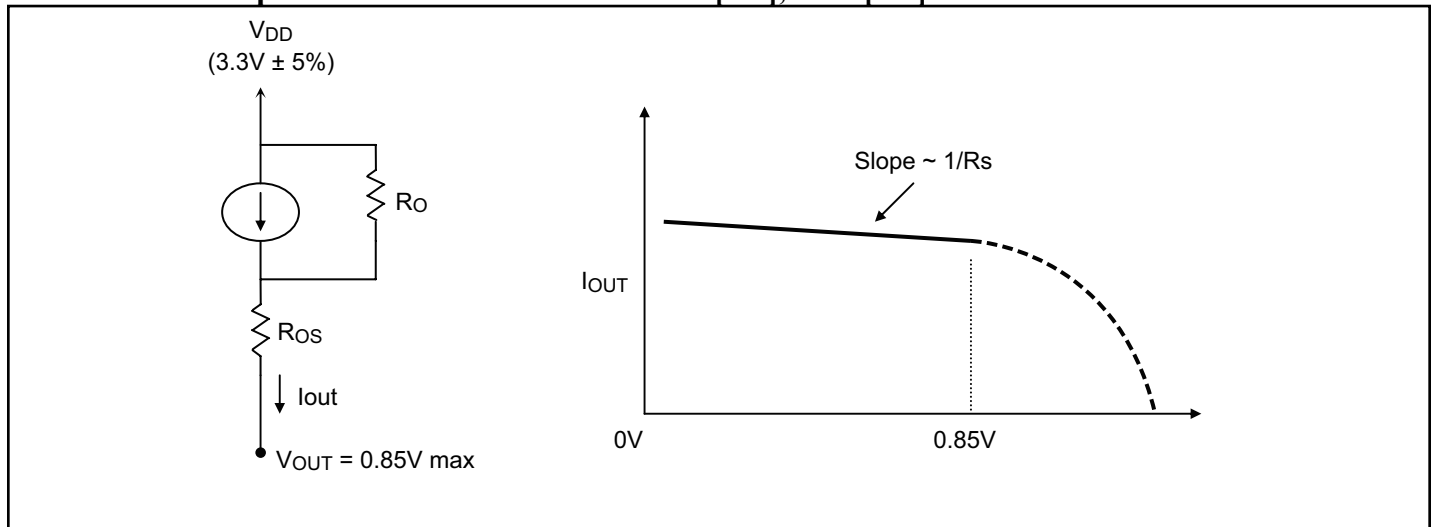


Figure 9. Simplified diagram of current-mode output buffer

Differential Clock Buffer characteristics

| Symbol | Minimum | Maximum |
|-----------|-------------|-------------|
| R_o | 3000Ω | N/A |
| R_{os} | unspecified | unspecified |
| V_{OUT} | N/A | 850mV |

Current Accuracy

| Symbol | Conditions | Configuration | Load | Min. | Max. |
|-----------|-------------------------|---|---|-----------------------|-----------------------|
| I_{OUT} | $V_{DD} = 3.30 \pm 5\%$ | $R_{REF} = 475\Omega \text{ 1\%}$ $I_{REF} = 2.32mA$ | Nominal test load for given configuration | -12% $I_{NOMINAL}$ | +12% $I_{NOMINAL}$ |

Note:

- $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Differential Clock Output Current

| Board Target Trace/Term Z | Reference R, $I_{ref} = V_{DD}/(3xRr)$ | Output Current | $V_{OH} @ Z$ |
|--|---|-----------------------------|--------------|
| 100Ω (100Ω differential \approx 15% coupling ratio) | $R_{REF} = 475\Omega \text{ 1\%}$, $I_{REF} = 2.32mA$ | $I_{OH} = 6 \times I_{REF}$ | 0.7V @ 50 |

Absolute Maximum Ratings⁽¹⁾ (Over operating free-air temperature range)

| Symbol | Parameters | Min. | Max. | Units |
|-------------------|--------------------------|------|------|-------|
| V _{DD_A} | 3.3V Core Supply Voltage | -0.5 | 4.6 | V |
| V _{DD} | 3.3V I/O Supply Voltage | -0.5 | 4.6 | |
| V _{IH} | Input HIGH Voltage | | 4.6 | |
| V _{IL} | Input LOW Voltage | -0.5 | | |
| T _s | Storage Temperature | -65 | 150 | °C |
| V _{ESD} | ESD Protection | 2000 | | V |

Note:

1. Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

DC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3±5%)

| Symbol | Parameters | Condition | Min. | Max. | Units |
|-------------------|-----------------------------|---|-----------------------|-----------------------|-------|
| V _{DD_A} | 3.3V Core Supply Voltage | | 3.135 | 3.465 | V |
| V _{DD} | 3.3V I/O Supply Voltage | | 3.135 | 3.465 | |
| V _{IH} | 3.3V Input HIGH Voltage | | 2.0 | V _{DD} + 0.3 | |
| V _{IL} | 3.3V Input LOW Voltage | | V _{SS} - 0.3 | 0.8 | |
| I _{IK} | Input Leakage Current | 0 < V _{IN} < V _{DD} | -5 | +5 | µA |
| V _{OH} | 3.3V Output HIGH Voltage | I _{OH} = -1mA | 2.4 | | V |
| V _{OL} | 3.3V Output LOW Voltage | I _{OL} = 1mA | | 0.4 | |
| I _{OH} | Output HIGH Current | I _{OH} = 6 x I _{REF} , I _{REF} = 2.32mA | 12.2 | 15.6 | mA |
| C _{IN} | Logic Input Pin Capacitance | | 1.5 | 5 | |
| C _{OUT} | Output Pin Capacitance | | | 6 | pF |
| L _{PIN} | Pin Inductance | | | 7 | nH |
| I _{DD} | Power Supply Current | V _{DD} = 3.465V, F _{CPU} = 100MHz | | 250 | mA |
| I _{SS} | Power Down Current | Driven outputs | | 80 | |
| I _{SS} | Power Down Current | Tristate outputs | | 12 | |
| T _A | Ambient Temperature | Commercial (PI6C20800S) | 0 | 70 | °C |
| | | Industrial (PI6C20800SI) | -40 | 85 | |

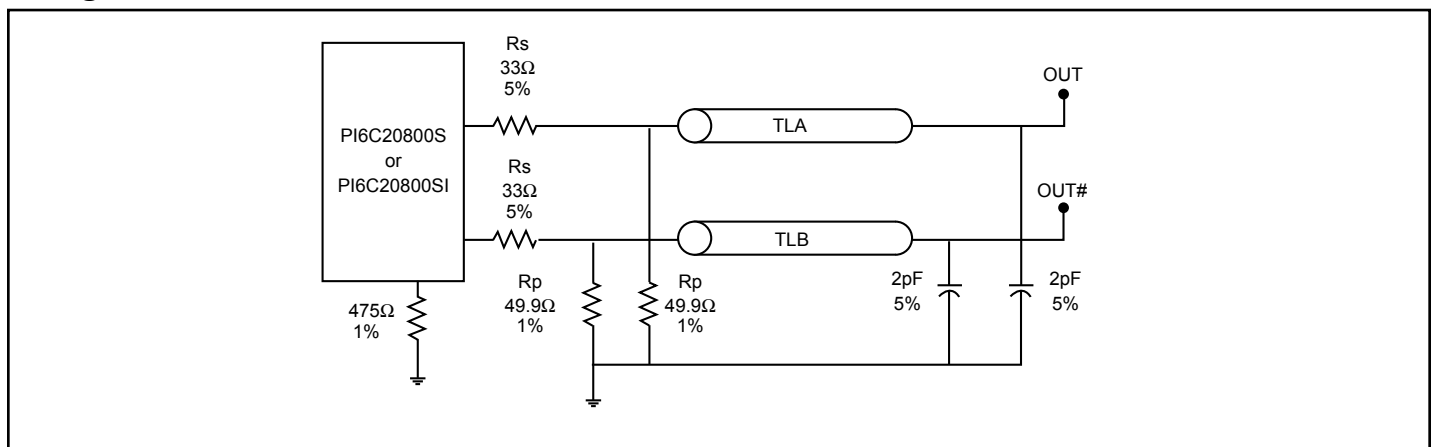
AC Switching Characteristics^(1,2,3) ($V_{DD} = 3.3 \pm 5\%$, $V_{DD_A} = 3.3 \pm 5\%$)

| Symbol | Parameters | Min | Max. | Units | Notes | |
|-------------------------------------|--|-------------|-------------|-------|-------|----|
| F_{in} | SRC/SRC# Input Frequency PLL Mode | 95 | 105 | MHz | 6 | |
| | SRC/SRC# Input Frequency Bypass Mode | 95 | 400 | MHz | 6 | |
| T_{rise} / T_{fall} | Rise and Fall Time (measured between 0.175V to 0.525V) | 175 | 700 | ps | 2 | |
| $\Delta T_{rise} / \Delta T_{fall}$ | Rise and Fall Time Variation | | 125 | | 2 | |
| T_{pd} | Input to Output Propagation Delay | PLL Mode | PI6C20800S | -250 | 250 | ps |
| | | | PI6C20800SI | -450 | 450 | |
| | | Bypass Mode | PI6C20800S | -6 | 6 | ns |
| | | | PI6C20800SI | -8 | 8 | |
| T_{skew} | Output-to-Output Skew (PI6C20800S) | | 50 | ps | 3 | |
| | Output-to-Output Skew (PI6C20800SI) | | 65 | | 3 | |
| V_{HIGH} | Voltage HIGH (Measured at 100MHz @ 3.3V) | 600 | 900 | mV | 2 | |
| V_{OVS} | Max. Voltage | | 1150 | | | |
| V_{UDS} | Min. Voltage | -300 | | | | |
| V_{LOW} | Voltage LOW | -150 | +150 | | 2 | |
| V_{cross} | Absolute crossing poing voltages | 250 | 550 | | 2 | |
| ΔV_{cross} | Total Variation of V_{cross} over all edges | | 140 | | 2 | |
| T_{DC} | Duty Cycle (Measured at 100 MHz) | 45 | 57 | % | 3 | |
| $T_{jycyc-cyc}$ | Jitter, Cycle-to-cycle (PLL Mode, Measurement for differential waveform) | | 70 | ps | 4 | |
| | Jitter, Cycle-to-cycle (BYPASS mode as additive jitter) | | | | | |
| J_{add} | Additive RMS phase jitter for PCIe 2.0 | <0 | 1 | ps | 5 | |

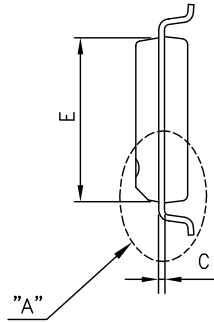
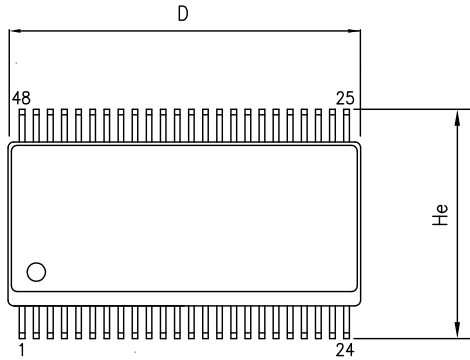
Notes:

1. Test configuration is $R_S = 33.2\Omega$, $R_p = 49.9\Omega$, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measured using M1 timing analyzer from Amherst.
5. Additive jitter is calculated from input and output RMS phase jitter by using PCIe 2.0 filter. ($J_{add} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$)
6. -0.5% downnspread input

Configuration Test Load Board Termination

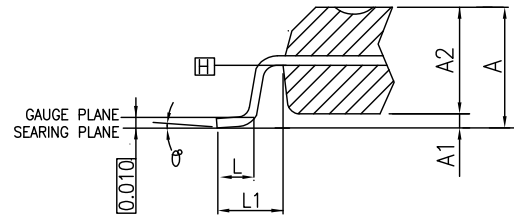
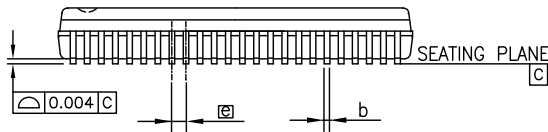


Packaging Mechanical: 48-Pin SSOP (V)



| SYMBOLS | MIN. | NOM. | MAX. |
|---------|-------|-------|--------|
| A | 0.095 | 0.102 | 0.110 |
| A1 | 0.008 | 0.012 | 0.016 |
| A2 | 0.089 | 0.094 | 0.099 |
| b | 0.008 | 0.010 | 0.0135 |
| c | — | 0.008 | — |
| D | 0.620 | 0.625 | 0.630 |
| E | 0.291 | 0.295 | 0.299 |
| e | — | 0.025 | — |
| He | 0.395 | 0.406 | 0.420 |
| L | 0.020 | 0.030 | 0.040 |
| L1 | — | 0.056 | — |
| θ | 0° | — | 8° |

UNIT : INCH



DETAIL : A

Notes:

1. All dimensions are in inches
2. JEDEC outline : MO-118 AA.
3. Dimensions E and D do not include mold protrusion.



DATE: 09/27/11

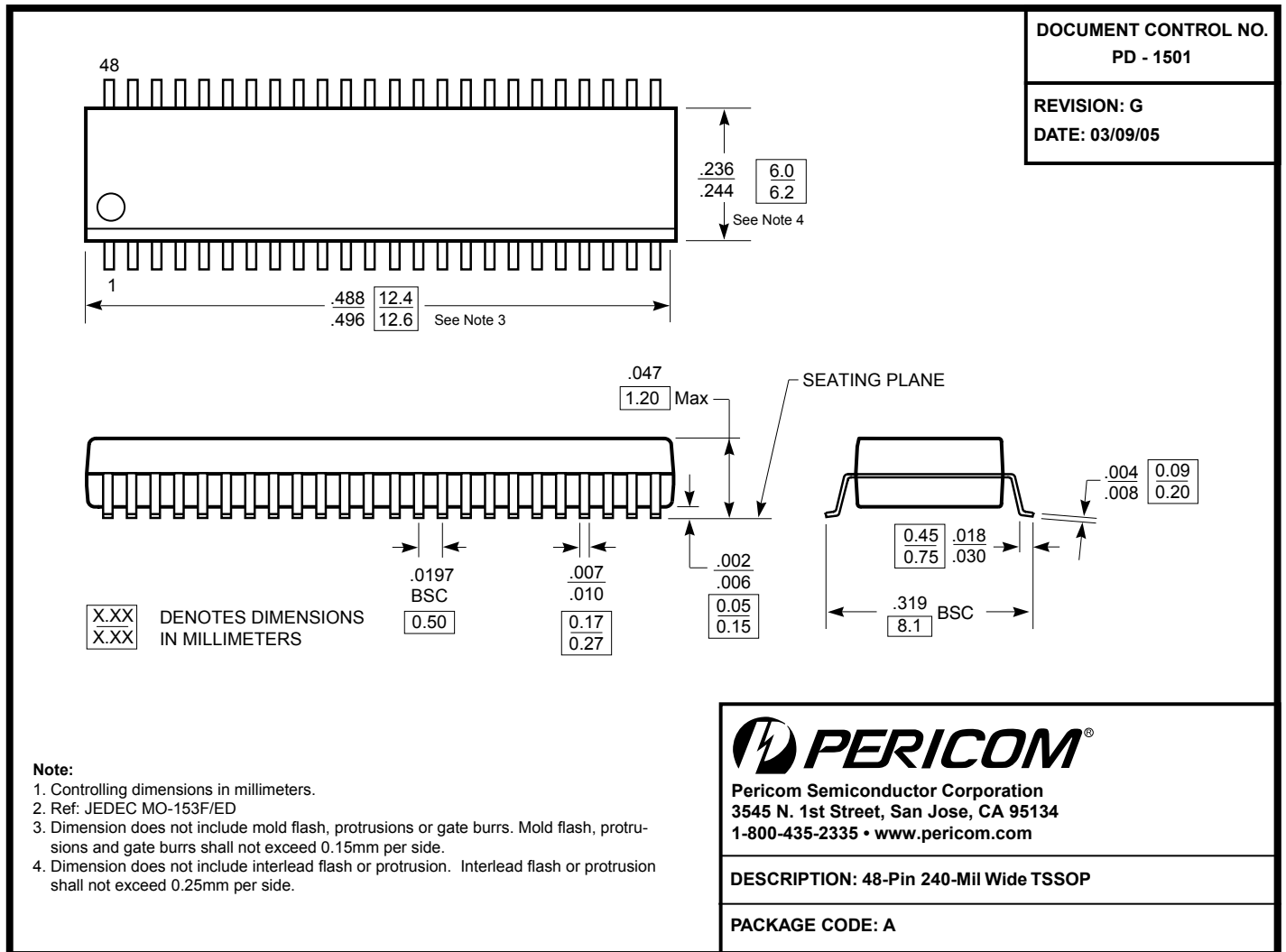
DESCRIPTION: 48-Pin, 300-Mil Wide, SSOP

PACKAGE CODE: V (V48)

DOCUMENT CONTROL #: PD-1401

REVISION:F

Packaging Mechanical: 48-Pin TSSOP (A)



Ordering Information(1,2)

| Ordering Code | Package Code | Package Description |
|---------------|--------------|---|
| PI6C20800SVE | VE | 48-pin, 300-mil wide, SSOP, Pb-Free and Green |
| PI6C20800SAE | AE | 48-pin, 240-mil wide, TSSOP, Pb-Free and Green |
| PI6C20800SIVE | VE | 48-pin, 300-mil wide, SSOP, Pb-Free and Green (Industrial) |
| PI6C20800SIAE | AE | 48-pin, 240-mil wide, TSSOP, Pb-Free and Green (Industrial) |

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel