

## PCIe® 3.0/2.0/1.0 Clock Generator with 2 HCSL Outputs

### Features

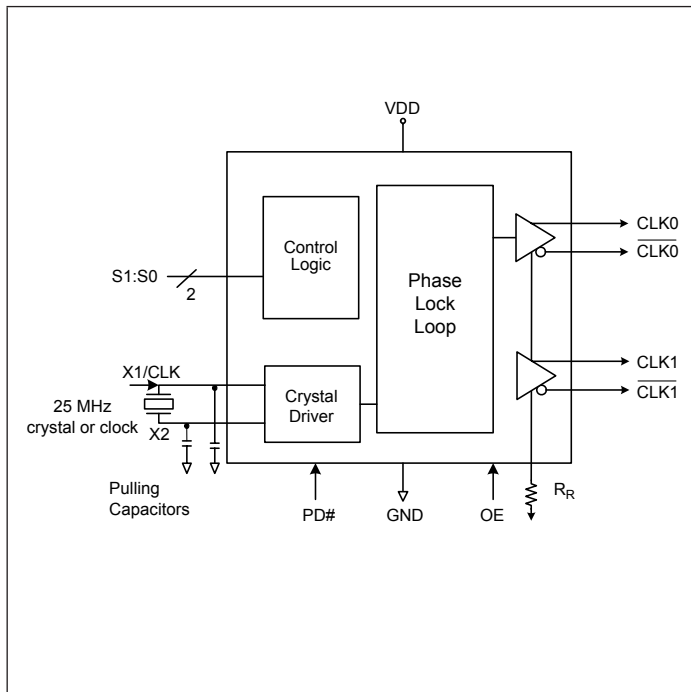
- PCIe® 3.0/2.0/1.0 compliant
  - PCIe 3.0 Phase jitter - 0.45ps RMS (High Freq. Typ.)
- LVDS compatible outputs
- Supply voltage of 3.3V ±10%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.8V Current mode differential pair
- Jitter 35ps cycle-to-cycle (typ)
- RMS phase jitter 12kHz ~ 20MHz @ 100MHz - 0.32ps (typ)
- RMS phase jitter 12kHz ~ 20MHz @ 125MHz - 0.3ps (typ)
- Power down mode
- Industrial temperature range
- Packaging: (Pb-free and Green): 16-pin TSSOP (L16)

### Description

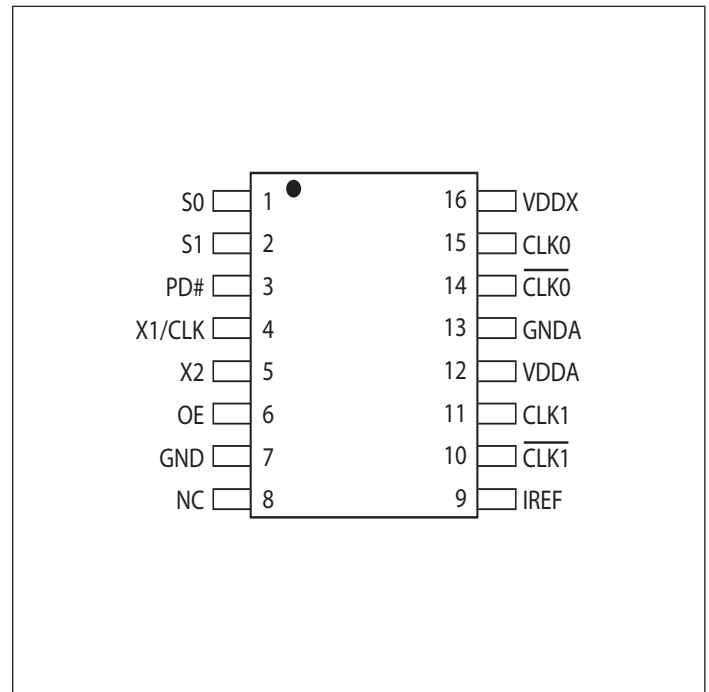
The PI6LC48H02-01 is a clock generator compliant to PCI Express® 3.0/2.0/1.0 and Ethernet requirements. The device is used for servers, networking or embedded systems.

The PI6LC48H02-01 provides two differential (HCSL) or LVDS outputs. Using Pericom's patented Phase Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces two pairs of differential outputs (HCSL) at 25MHz, 100MHz, 125MHz, 200MHz clock frequencies.

### Block Diagram



### Pin Configuration (16-Pin TSSOP)



### Pin Description

Pin #	Pin Name	I/O Type	Description
1	S0	Input	Select pin 0 (Internal pull-up resistor). See Table 1.
2	S1	Input	Select pin 1 (Internal pull-up resistor). See Table 1.
3	PD#	Input	Power down mode. Internla pull-up resistor. See Table 2.
4	X1/CLK	Input	Crystal or clock input. Connect to a 25MHz crystal or single ended clock.
5	X2	Output	Crystal connection. Leave unconnected for clock input.
6	OE	Input	Output enable. Internal pull-up resistor.
7	GND	Power	Ground
8	NC	-	Do not connect
9	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
10	$\overline{\text{CLKI}}$	Output	HCSL compliment clock output
11	CLK1	Output	HCSL clock output
12	VDDA	Power	Connect to a +3.3V source.
13	GND <sub>A</sub>	Power	Output and analog circuit ground.
14	$\overline{\text{CLK0}}$	Output	HCSL compliment clock output
15	CLK0	Output	HCSL clock output
16	VDDX	Power	Connect to a +3.3V source.

**Table 1: Output Select Table**

S1	S0	CLK(MHz)
0	0	25
0	1	100
1	0	125
1	1	200

**Table 2: Power down mode**

PD#	Device
0	Power down mode
1	Normal Operation mode, default

## Application Information

### Decoupling Capacitors

Decoupling capacitors of 0.01μF should be connected between each V<sub>DD</sub> pin and the ground plane and placed as close to the V<sub>DD</sub> pin as possible.

### Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

### Crystal Capacitors

$C_L$  = Crystals's load capacitance in pF

Crystal Capacitors (pF) =  $(C_L - 8) * 2$

For example, for a crystal with 16pF load caps, the external effective crystal cap would be 16 pF.  $(16-8)*2=16$ .

### Current Source (IREF) Reference Resistor - R<sub>R</sub>

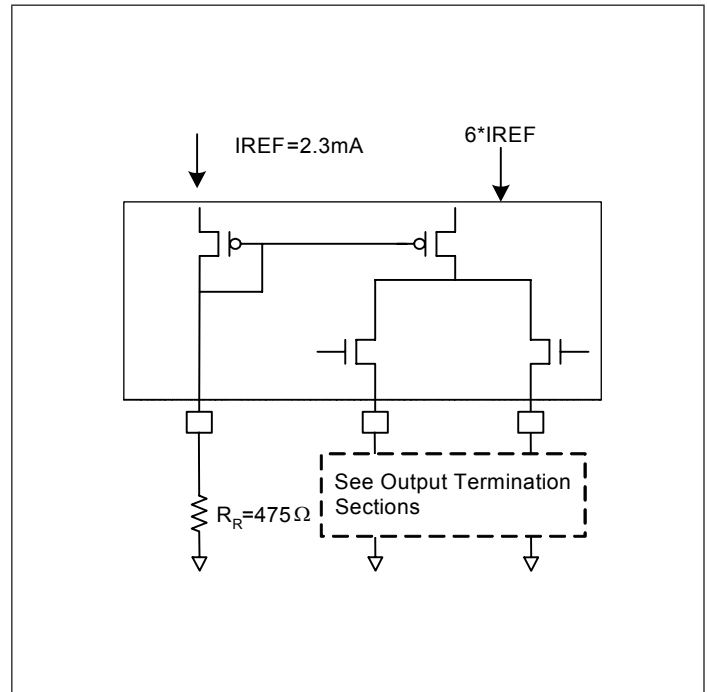
If board target trace impedance is 50Ω, then R<sub>R</sub> = 475Ω providing an IREF of 2.32 mA. The output current (I<sub>OH</sub>) is 6\*IREF.

### Output Termination

The PCI Express differential clock outputs of the PI6LC48H02-01 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

The PI6LC48H02-01 can be configured for LVDS compatible voltage levels. See the LVDS Compatible Layout Guidelines section.

## Output Structures



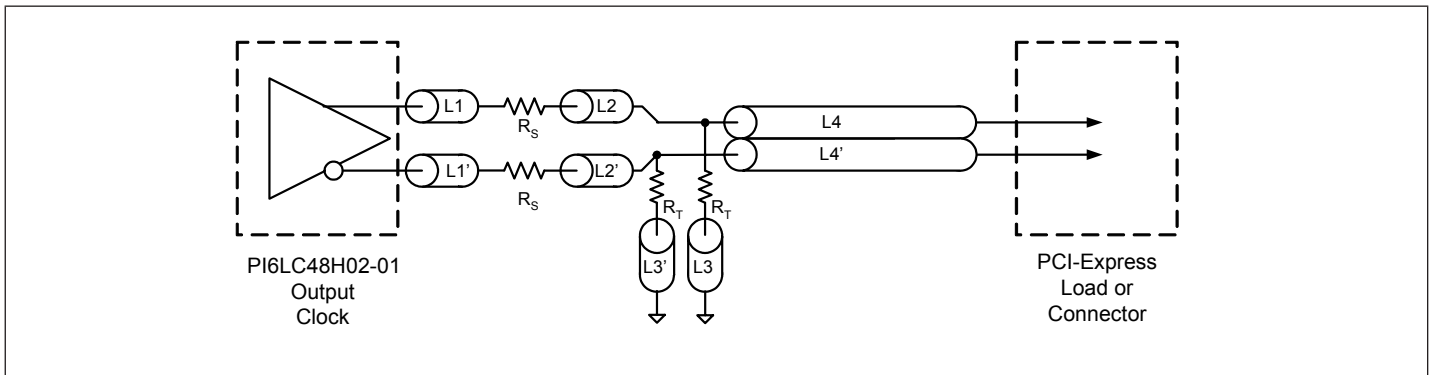
### PCI Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
$R_S$	33	Ω
$R_T$	49.9	Ω

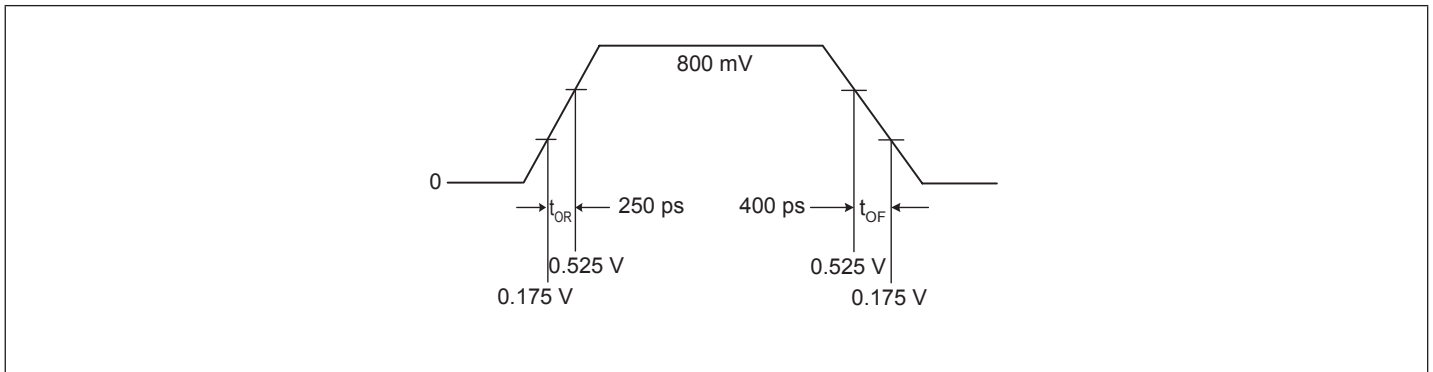
Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	1.8 min to 14.4 max	inch

Differential Routing to a PCI Express connector	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	0.225 min to 12.6 max	inch

### PCI Express Device Routing



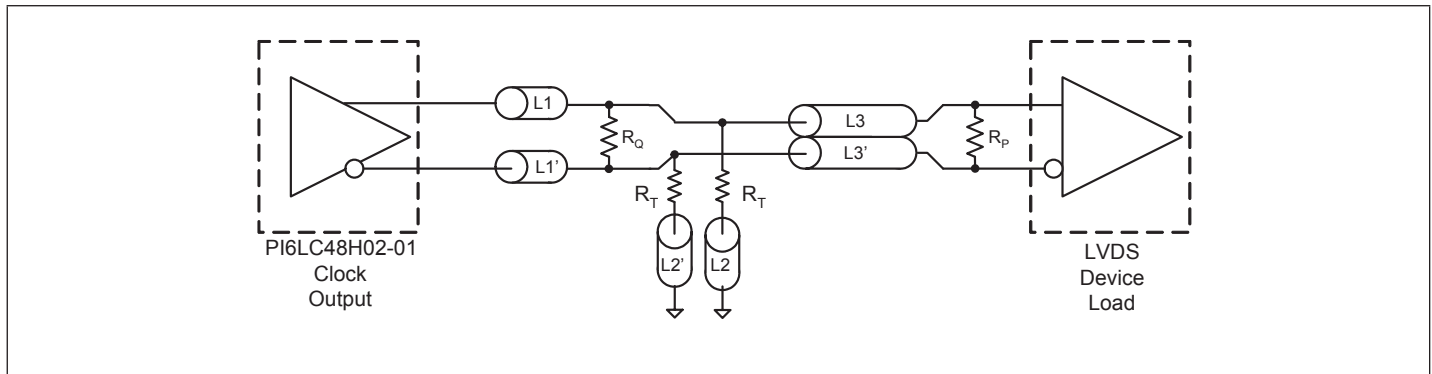
### Typical PCI Express (HCSL) Waveform



### Application Information

LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
RP	100	Ω
RQ	100	Ω
RT	150	Ω
L3 length, route as 100Ω differential trace.		
L3 length, route as 100Ω differential trace.		

### LVDS Device Routing



## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential . . . . .	4.6V
All Inputs and Outputs . . . . .	-0.5V to V <sub>DD</sub> +0.5V
Ambient Operating Temperature . . . . .	-40 to +85°C
Storage Temperature . . . . .	-65 to +150°C
ESD Protection (HBM) . . . . .	2000 V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Specifications

### Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

### DC Characteristics (V<sub>DD</sub> = 3.3V ±10%, T<sub>A</sub> = -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		3.0	3.3	3.6	V
V <sub>IH</sub>	Input High Voltage <sup>(1)</sup>	OE, S0, S1, PD#	2.0		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage <sup>(1)</sup>	OE, S0, S1, PD#	GND -0.3		0.8	V
I <sub>IH</sub>	Input High Current	V <sub>in</sub> = V <sub>DD</sub>	-5		5	μA
I <sub>IL</sub>	Input Low Current	V <sub>in</sub> = 0	-20		20	
I <sub>DD</sub>	Operating Supply Current	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 2pF		100	115	mA
I <sub>DDOE</sub>		OE = LOW		58	65	mA
I <sub>DDPD</sub>	Power down Supply Current	PD# = LOW		0.07	0.15	mA
C <sub>IN</sub>	Input Capacitance	@ 25MHz			7	pF
C <sub>OUT</sub>	Output Capacitance	@ 25MHz			6	pF
L <sub>PIN</sub>	Pin Inductance				5	nH
R <sub>OUT</sub>	Output Resistance	CLK Outputs	3.0			kΩ

Notes:

1. Single edge is monotonic when transitioning through region.

**HCSL Output AC Characteristics ( $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$F_{IN}$	Input Frequency			25		MHz
$F_{OUT}$	Output Frequency		25		200	MHz
$V_{OH}$	Output High Voltage <sup>(1,2)</sup>	100 MHz HCSL output @ $V_{DD} = 3.3V$	660	800	900	mV
$V_{OL}$	Output Low Voltage <sup>(1,2)</sup>		-150	0		mV
$V_{CPA}$	Crossing Point Voltage <sup>(1,2)</sup>	Absolute	250	350	550	mV
$V_{CN}$	Crossing Point Voltage <sup>(1,2,4)</sup>	Variation over all edges			140	mV
$J_{CC}$	Jitter, Cycle-to-Cycle <sup>(1,3)</sup>			35	60	ps
$J_{Phase}$	RMS Phase Jitter, (Random)	100MHz 25MHz Xtal input, 12kHz - 20MHz		0.33	0.5	ps
		125MHz 25MHz Xtal input, 12kHz - 20MHz		0.3	0.5	ps
$J_{RMS2.0}$	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output		2.03	3.1	ps
$J_{RMS3.0}$	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		0.51	3	ps
		PLL L-BW @ 2M & 4M 1st H3		0.58	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.44	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.38	1	ps
$t_{OR}$	Rise Time <sup>(1,2)</sup>	From 0.175V to 0.525V	175		700	ps
$t_{OF}$	Fall Time <sup>(1,2)</sup>	From 0.525V to 0.175V	175		700	ps
$T_{SKEW}$	Skew between outputs	At Crossing Point Voltage			50	ps
$T_{DUTY-CYCLE}$	Duty Cycle <sup>(1,3)</sup>		45		55	%
$T_{OE}$	Output Enable Time <sup>(5)</sup>	All outputs			10	$\mu s$
$T_{OT}$	Output Disable Time <sup>(5)</sup>	All outputs			10	$\mu s$
$t_{STABLE}$	Stabilization Time	From Power-up $V_{DD}=3.3V$		14		ms

**Notes:**

1.  $R_L = 50\text{-}\Omega$  with  $C_L = 2\text{ pF}$
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

### Thermal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\theta_{JA}$	Thermal Resistance Junction to Ambient	Still air			90	°C/W
$\theta_{JC}$	Thermal Resistance Junction to Case				24	°C/W

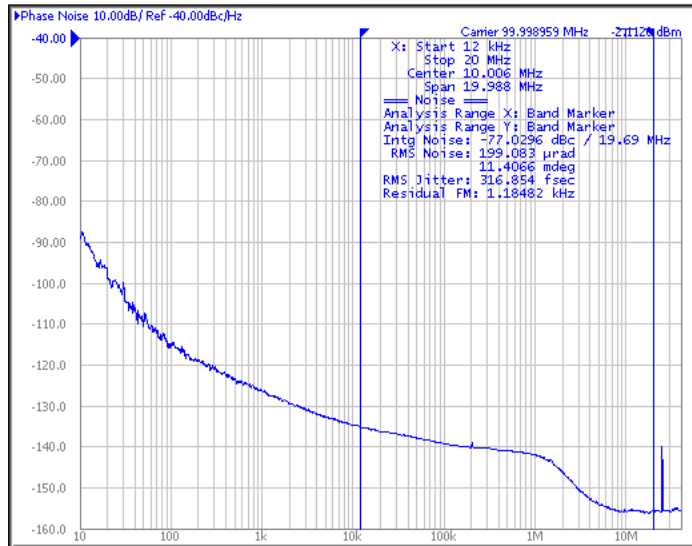
### Recommended Crystal Specification

Pericom recommends:

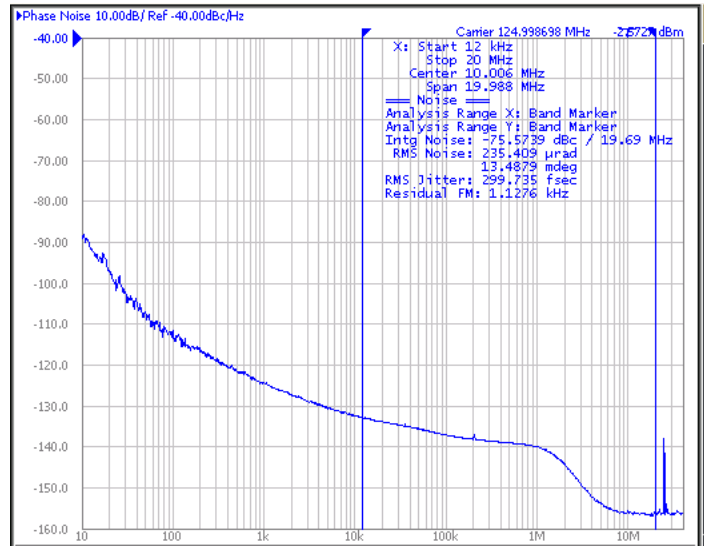
- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/GC\\_GF.pdf](http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf)
- b) FY2500091, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
- c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm  
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

### Phase Noise Plot

#### 100MHz

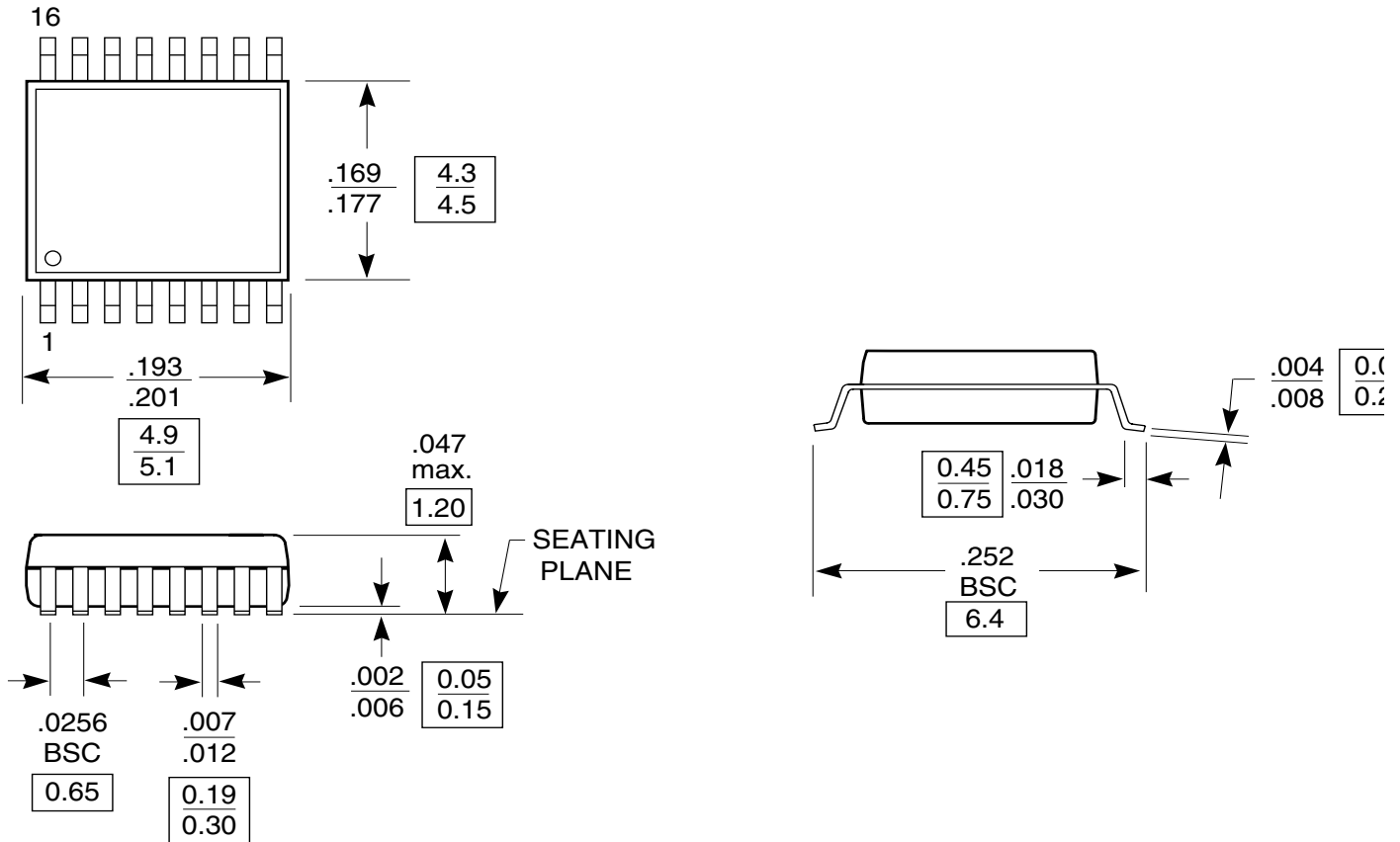


#### 125MHz





**Packaging Mechanical: 16-Pin TSSOP (L)**



Note: For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

**Ordering Information**

Ordering Code	Package Code	Package Type
PI6LC48H02-01LIE	L	Pb-free & Green, 16-pin TSSOP
PI6LC48H02-01LIEX	L	Pb-free & Green, 16-pin TSSOP, Tape & Reel

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging