Single Output LVCMOS Clock Generator

Features

- Single LVCMOS output
- Supports 125MHz or 130MHz output frequencies
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.15ps (typical)
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz – 20MHz): 0.33ps (typical)
- Full 3.3V or 2.5V supply modes
- Industrial ambient operating temperature
- Available in lead-free package: 8-TSSOP

Description

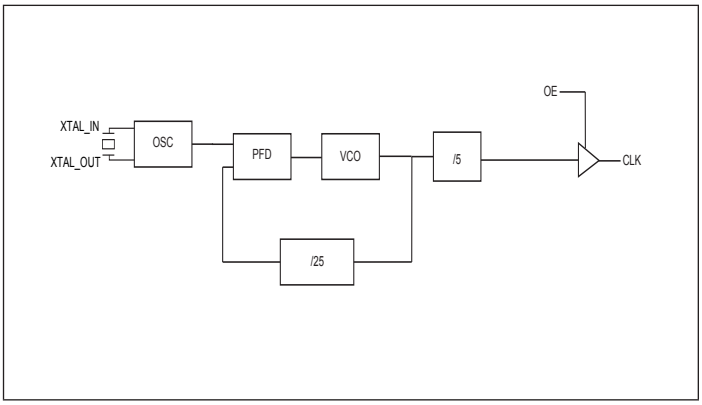
The PI6LC48C21 is a single LVCMOS output synthesizer optimized to generate Ethernet reference clock frequencies and is a member of Pericom's HiFlex family of high performance clock solutions. Using a 25MHz crystal, It can generate 125MHz with very low phase jitter.

It is ideal for Ethernet interface in all kind of systems.

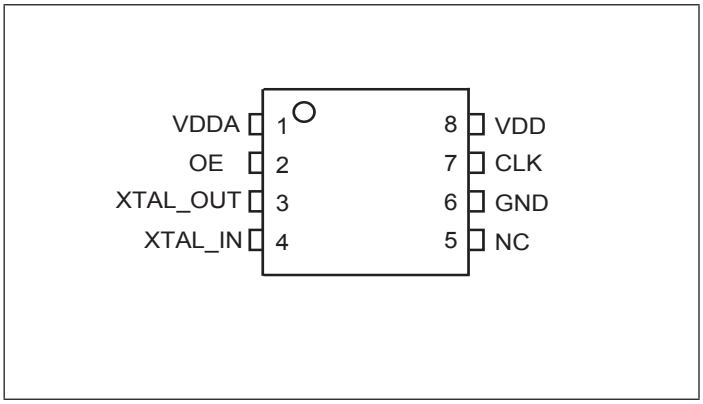
Applications

- Networking systems

Block Diagram



Pin Configuration



Pinout Table

Pin No.	Pin Name	I/O Type		Description
1	VDDA	Power		Analog Power Supply
2	OE	Input	Pull-up	High: Output enabled; Low: Output high impedence
3, 4	XTAL_OUT, XTAL_IN	Crystal		Crystal Input and Output
5	NC			No Connect
6	GND	Power		Ground
7	CLK	Output		Output Clock
8	VDD	Power		Power Supply

Typical Crystal Requirement

Parameter	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental		
Frequency	22.4	25	27.2	MHz
Equivalent Series Resistance (ESR)			50	Ω
Shunt Capacitance			7	pF
Drive Level			1	mW

Recomended Crystal Specification

Pericom recommends:
a) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm. http://www.pericom.com/pdf/datasheets/se/FL.pdf

b) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm. http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2600018, SMD 3.2x2.5(4P), 26MHz, CL=18pF, +/-20ppm. http://www.pericom.com/pdf/datasheets/se/FL.pdf

Output Frequency

Crystal Frequency (MHz)	Output Frequency (MHz)
25	125
26	130

Pin Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
C_{JN}	Input Capacitance		4		pF
R_{PULLUP}	Pull up resistor		51		kΩ
R_{OUT}	Output Impedence		15		Ω

Maximum Ratings (Over operating free-air temperature range)

Storage Temperature..... -65°C to+155°C
Ambient Temperature with Power Applied.....-40°C to+85°C
3.3V Analog Supply Voltage.....-0.5 to +3.6V
ESD Protection (HBM) 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

Power Supply DC Characterisitcs, ($V_{DD} = V_{DDA}$, T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}, V_{DDA}	Core, Analog Supply Voltage		3.135	3.3	3.465	V
V_{DD}, V_{DDA}	Core, Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				45	mA
I_{DDA}	Analog Supply Current				25	mA

DC Electrical Characteristics, ($V_{DD} = V_{DDA}$, T_A = -40 to 85°C)

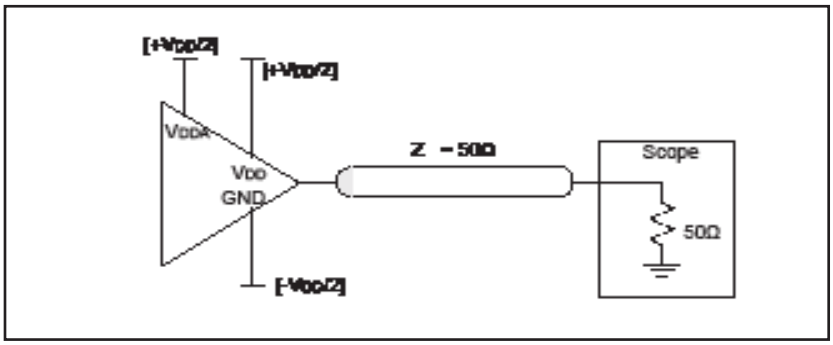
Symbol	Parameter		Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V **±5%**	2		V_{DD} +0.3	V
			V_{DD} = 2.5V ±5%	1.7		V_{DD} +0.3	
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ±5%	-0.3		0.8	V
			V_{DD} = 2.5V ±5%	-0.3		0.7	
V_{OH}	Output High Voltage		V_{DD} = 3.3V±5%, I_{OH} = -8mA	2.6			V
			V_{DD} = 2.5V±5%, I_{OH} = -4mA	90% VDD			
V_{OL}	Output Low Voltage		V_{DD} = 3.3V±5%, I_{OL} = 8mA			0.4	V
			V_{DD} = 2.5V±5%, I_{OL} = 4mA			10% VDD	
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN}$ = 3.465V			5	uA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			uA

AC Electrical Characteristics, ($V_{DD} = V_{DDA}$, T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
f_{OUT}	Output Frequency		112	125	136	MHz
$t_{jit(Ø)}$	RMS Phase Jitter, (Random)(1)	125MHz, (1.875MHz - 20MHz)		0.15		ps
		125MHz, (12kHz - 20MHz)		0.33		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		800	ps
o_{DC}	Output Duty Cycle		47		53	%

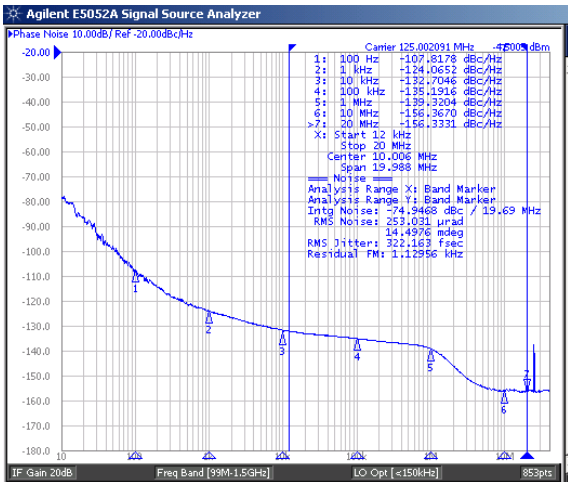
Note:
1. Please refer to the Phase Noise Plots.

LVCMOS Test Circuit



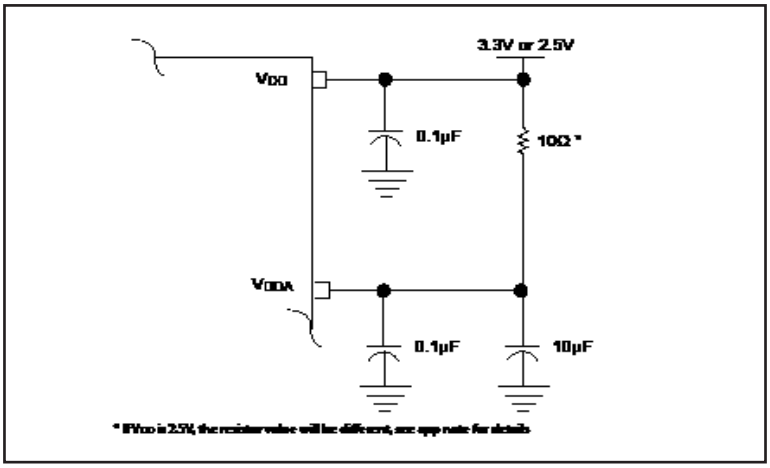
Phase Noise Plot

125MHz



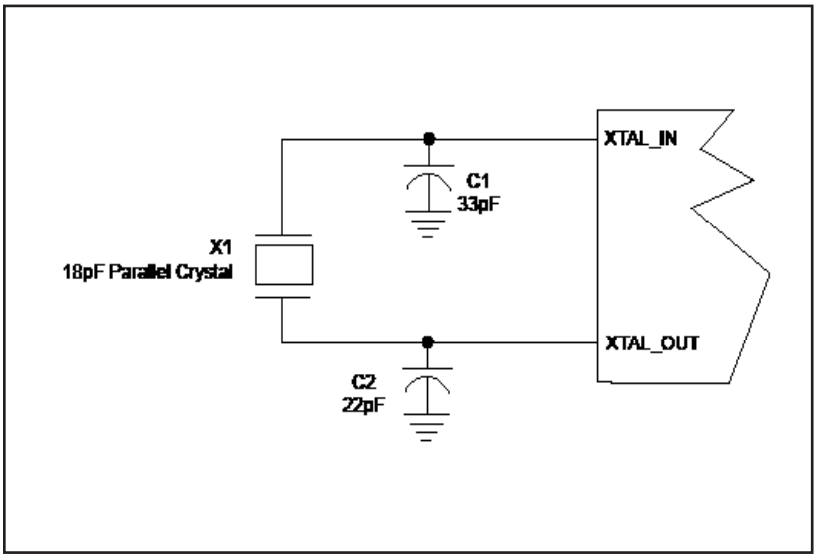
Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48C21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.1µF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.



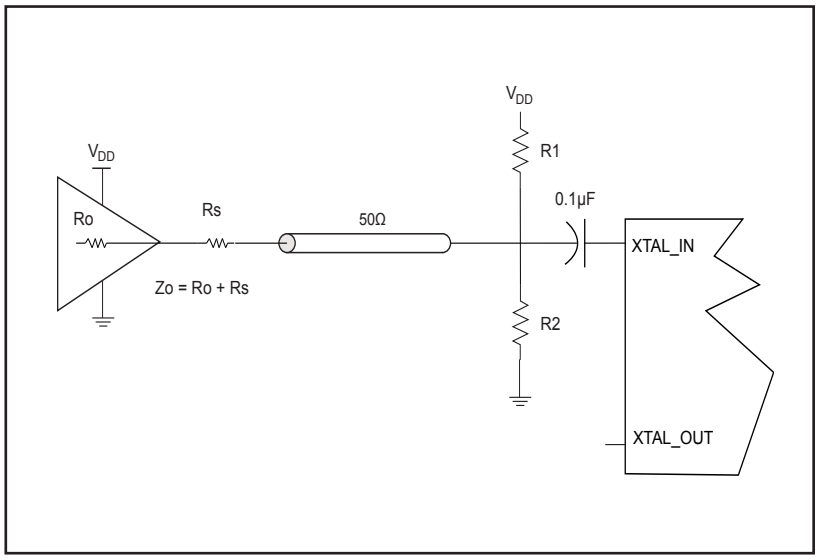
Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

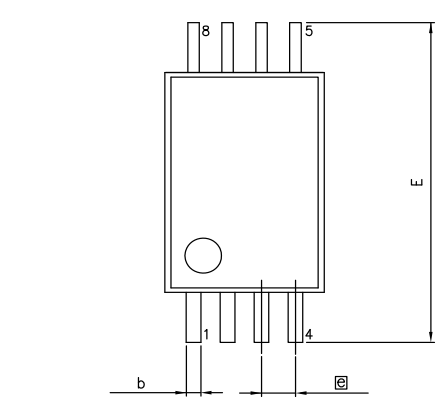


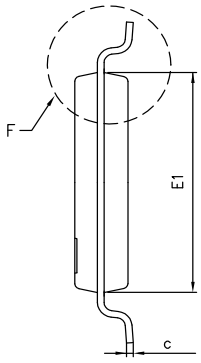
LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R1 and R2 in parallel should equal the transmission line empedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is quaranteed by using a quartz crystal.



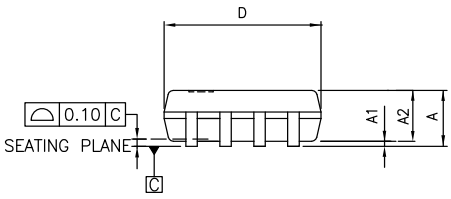
Packaging Mechanical: 8-Contact TSSOP (L)

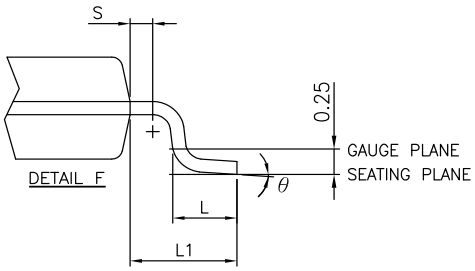




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E		6.40 BSC	
e		0.65 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	–	–
θ°	0	–	8

UNIT : MM





Notes:
1. Refer JEDEC MO-153F/AA
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity — **DATE: 05/03/12**

DESCRIPTION: 8 pin, 173mil wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1308 **REVISION: F**

12-0370

Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6LC48C21LIE	L	Pb-free & Green, 8-pin TSSOP	Industrial
PI6LC48C21LIEX	L	Pb-free & Green, 8-pin TSSOP, Tape & Reel	Industrial

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging