

### Features

- 2.5/3.3V supply voltage
- 4 HCSL 100/125/200/250MHz outputs with OE
- 2 LVCMOS 33/50/66/100MHz selectable outputs
- 5 LVCMOS 25MHz or 125MHz outputs
- 1 LVPECL 312.5MHz, 156.25MHz or 125MHz output
- 1 CMOS 156.25MHz or 125MHz output
- 1 LVPECL 125MHz or 25MHz output
- 25MHz crystal or differential input
- 0.5ps (typ) RMS integrated phase noise design at 3.3V operation
- 1.0ps (typ) RMS integrated phase noise design at 2.5V operation
- PLL Bypass mode for test
- Industrial Temperature -40°C to 85°C
- TQFN - 56 package

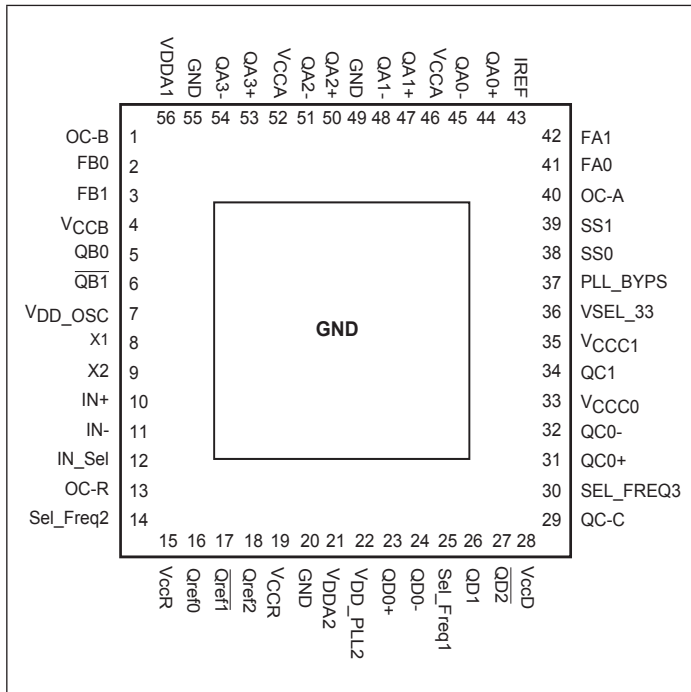
### Description

The PI6LC4833 implements Pericom's advanced LC VCO technology and is specifically designed for Power PC network processor (Freescale MPC8548, MPC8572, AMCC 460, AMI732). This high performance device is optimized to generate CPU core/PCI clock, high performance PCIe Gen1/2 Clock, SRIO, Gigabit Ethernet's MAC and PHY clock. All outputs are generated from 25MHz external clock input or crystal.

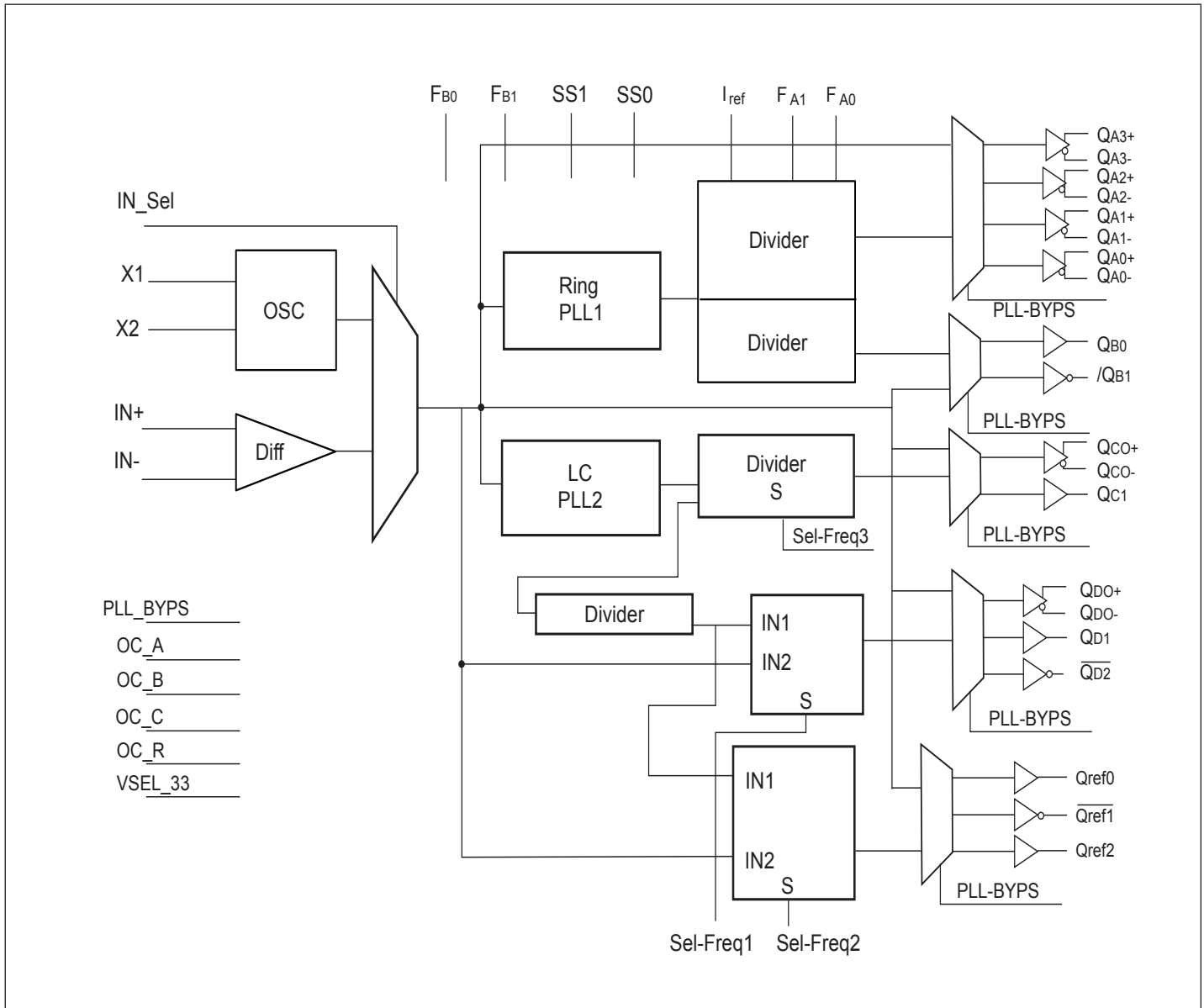
### Application

- Router/Switch
- OLT, BSC, WLAN, Wireless gateway
- Wireless

### Pin Configuration (56-Pin TQFN)



**Block Diagram**



**Pinout Table**

Pin Number	Pin Name	I/O Type	Description
44, 45, 47, 48, 50, 51, 53, 54	Q <sub>A0+</sub> , Q <sub>A0-</sub> , Q <sub>A1+</sub> , Q <sub>A1-</sub> , Q <sub>A2+</sub> , Q <sub>A2-</sub> , Q <sub>A3+</sub> , Q <sub>A3-</sub>	Output	100/125/200/250MHz HCSL Outputs
5, 6	Q <sub>B0</sub> , $\overline{Q}_{B1}$	Output	33/50/66/100MHz LVCMOS Outputs
8	X1	Input	Crystal Input Pin
9	X2	Output	Oscillator Output Pin
10, 11	IN+, IN-	Input	HCSL/LVPECL/LVDS Inputs
12	IN_Sel	Input	Low: X1 and X2 are selected. High: IN+ and IN- are selected. The pin has an internal pull-up resistor of 100k $\Omega$ .
37	PLL_BYPS	Input	Low: Output buffers are switched to the PLL. High: Output buffers are switched to the input mux. The pin has an internal pull-down resistor of 100k $\Omega$ .
40, 1, 29, 13	OC_A, OC_B, OC_C, OC_R	Input	Low: Outputs are enabled. High: High impedance mode is selected. The pin has an internal pull-down resistor of 100k $\Omega$ .
7	V <sub>DD_OSC</sub>	Power	Power for crystal OSC core
21	V <sub>DDA2</sub>	Power	Power for LC PLL2
46, 52, 4, 33, 35, 28, 15, 19	V <sub>ccA</sub> , V <sub>ccB</sub> , V <sub>ccC0</sub> , V <sub>ccC1</sub> V <sub>ccD</sub> , V <sub>ccR</sub>	Power	Power for output buffers (Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub> , Q <sub>ref</sub> )
56	V <sub>DDA1</sub>	Power	Power for Ring PLL1
20, 49, 55	GND	Power	Ground includes external paddle (EPAD).
34, 31, 32	Q <sub>C1</sub> , Q <sub>C0+</sub> / Q <sub>C0-</sub>	Output	125MHz/156.25MHz/312.5MHz LVCMOS and LVPECL
16, 17, 18, 23, 24, 26, 27	Q <sub>ref0</sub> , $\overline{Q}_{ref1}$ , Q <sub>ref2</sub> , Q <sub>D0+</sub> /Q <sub>D0-</sub> , Q <sub>D1</sub> , $\overline{Q}_{D2}$	Output	25MHz or 125MHz LVCMOS, or LVPECL (Q <sub>D0+</sub> /Q <sub>D0-</sub> )
42, 41	F <sub>A1</sub> , FA0	Input	Q <sub>A</sub> Bank Output Frequency Selection (see function table). This pin has a built-in pull-down resistor of 100k $\Omega$ .
3, 2	F <sub>B1</sub> , FB0	Input	Q <sub>B</sub> Bank Output Frequency Selection (see function table). This pin has a built-in pull-up resistor of 100k $\Omega$ .
25	Sel_Freq1	Input	Low: Q <sub>D</sub> 25MHz Output High: Q <sub>D</sub> 125MHz Output This pin has a built-in pull-up resistor of 100k $\Omega$ .
22	V <sub>DD_PLL2</sub>	Power	Power for PLL2 Core
14	Sel_Freq2	Input	Low: Q <sub>ref</sub> 25MHz Output High: 125MHz Output This pin has a built-in pull-down resistor of 100k $\Omega$ .

Pin Number	Pin Name	I/O Type	Description
30	Sel_Freq3	Input	Low: Q <sub>C</sub> 156.25MHz Output High: 125MHz Output Floating: Output 312.5MHz (Q <sub>C1</sub> is HiZ if floating) This pin has a built-in pull-up resistor of 150kΩ and pull-down resistor of 100kΩ.
39, 38	SS1, SS0	Input	Spread Selection Pin for Q <sub>A</sub> and Q <sub>B</sub> This pin has a built-in pull-up resistor of 100kΩ (see function table).
43	I <sub>REF</sub>	Input	External resistor connection for internal current reference
36	VSEL_33	Input	Low: 2.5V mode, High: 3.3V mode This pin has a built-in pull_up resistor of 100kΩ

### Function Table

Output	Buffer	Frequency (MHz)	Selection Pin
Q <sub>A0+/-</sub> , Q <sub>A1+/-</sub> , Q <sub>A2+/-</sub> , Q <sub>A3+/-</sub>	HCSL x4	100, 125, 200, 250	F <sub>A1</sub> , F <sub>A0</sub>
$\overline{Q}_{B1}$ , Q <sub>B0</sub>	CMOS x2	33.3333, 50, 66.6667, 100	F <sub>B1</sub> , F <sub>B0</sub>
Q <sub>C0+/-</sub>	LVPECL x1	125, 156.25, 312.5	Sel_Freq3
Q <sub>C1</sub>	CMOS x1	125, 156.25, HiZ	
Q <sub>D0+/-</sub>	LVPECL x1	25, 125	Sel_Freq1
$\overline{Q}_{D2}$ , Q <sub>D1</sub>	CMOS x2	25, 125	
Q <sub>ref2</sub> , $\overline{Q}_{ref1}$ , Q <sub>ref0</sub>	CMOS x3	25, 125	Sel_Freq2

F <sub>B1</sub>	F <sub>B0</sub>	Q <sub>B0</sub>	$\overline{Q}_{B1}$	Output
0	0	33.33MHz	33.33MHz	LVC MOS
0	1	66.66MHz	66.66MHz	LVC MOS
1	0	100MHz	100MHz	LVC MOS
1	1	50MHz	50MHz	LVC MOS

F <sub>A1</sub>	F <sub>A0</sub>	Q <sub>A0+</sub> / Q <sub>A0-</sub>	Q <sub>A1+</sub> / Q <sub>A1-</sub>	Q <sub>A2+</sub> / Q <sub>A2-</sub>	Q <sub>A3+</sub> / Q <sub>A3-</sub>
0	0	100MHz	100MHz	100MHz	100MHz
0	1	125MHz	125MHz	125MHz	125MHz
1	0	200MHz	200MHz	200MHz	200MHz
1	1	250MHz	250MHz	250MHz	250MHz

Sel_Freq3	Q <sub>Cx</sub>	Output_Freq
0	Q <sub>Cx</sub>	156.25MHz
1	Q <sub>Cx</sub>	125MHz
NC	Q <sub>C0</sub>	312.5MHz
	Q <sub>C1</sub>	HiZ

Sel_Freq1	Q <sub>D0+</sub> , Q <sub>D0-</sub>	$\bar{Q}_{D2}$ , Q <sub>D1</sub>	Output_Freq
0	LVPECL	LVC MOS	25MHz
1	LVPECL	LVC MOS	125MHz

Sel_Freq2	Q <sub>ref2</sub> , $\bar{Q}_{ref1}$ , Q <sub>ref0</sub>	Output_Freq
0	LVC MOS	25MHz
1	LVC MOS	125MHz

SS1	SS0	Spread %
0	0	+/- 0.25
0	1	-0.5
1	0	-0.75
1	1	No spread

Note: The SS1 and SS0 pins control the spread ratio of both Q<sub>A</sub> and Q<sub>B</sub>.

### Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +155°C
Operating Temperature .....	-40°C to +85°C
Supply Voltage .....	-0.5V to 4.6V
ESD Protection (HBM) .....	2000V

**Note:** Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>DD_XX</sub>	OSC, A1, A2, PLL2	2.5V	2.375	-	2.625	V
V <sub>CC_X</sub>	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub> , Q <sub>ref</sub>	2.5V	2.375	-	2.625	V
V <sub>DD_XX</sub>	OSC, A1, A2, PLL2	3.3V	3.135	-	3.465	V
V <sub>CC_X</sub>	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub> , Q <sub>ref</sub>	3.3V	3.135	-	3.465	V
I <sub>DD</sub>	Total Power Supply Current	-	-	-	360	mA
I <sub>DDA1, 2</sub>	Individual Analog PLL Current, V <sub>DDA1,2</sub>	-	-	-	50	mA
P <sub>Diss</sub>	Power Dissipation	-	-	-	1250	mW
T <sub>A</sub>	Operating Temperature	-	-40	-	+85	°C

### LVC MOS DC Electrical Characteristics (Over Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input High Voltage		2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage		-0.3	-	0.8	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -8mA	V <sub>DD</sub> -0.4	-	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA	-	-	0.4	V
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = V <sub>DD</sub>	-	-	45	μA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = 0V	-45	-	-	μA
R <sub>PU</sub>	Internal Pull Up Resistance	IN-, IN_SEL, F <sub>B1</sub> , F <sub>B0</sub> , Sel_Freq1, SS1, SS0, VSEL_33		100	-	kΩ
		Sel_Freq3		150		kΩ
R <sub>DN</sub>	Internal Pull Down Resistance	IN+, PLL_BYPS, OC_A, OC_B, OC_C, OC_R, F <sub>A1</sub> , F <sub>A0</sub> , Sel_ Freq2, Sel_Freq3		100	-	kΩ
Z <sub>O</sub>	Output Impedance	V <sub>DD</sub> = 2.5V	-	22	-	Ω
		V <sub>DD</sub> = 3.3V	-	17	-	Ω

**LVC MOS AC Characteristics** (Over Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units	
$f_{error}$	Frequency Synthesis Error	-	-	-	0	ppm	
$T_r/T_f$	Output Rise/Fall time	20% to 80%, CL =10pF	-	-	3	ns	
$T_{DC}$	Output Duty Cycle	$t_{DC} = t_H/t_{CY}$ , $t_H$ =High Pulse Width, $t_{CY}$ =Output Cycle Time, at $V_{DD}/2$	47	-	53	%	
$t_{jit(CC)}$	Jitter, Cycle-to-Cycle	$V_{DD} = 3.3V$ , $Q_B$ , $SS1 = SS0 = 1$	33.33MHz	-	70	110	ps
			66.67MHz	-	80	110	ps
			50MHz	-	70	100	ps
			100MHz	-	80	110	ps
		$V_{DD} = 3.3V$ , $Q_D, Q_{C1}, Q_{ref}$	25MHz	-	80	100	ps
			125MHz/ 156MHz	-	70	100	ps
		$V_{DD} = 2.5V$ , $Q_B$ , $SS1 = SS0 = 1$	33.33MHz	-	90	140	ps
			66.67MHz	-	110	130	ps
			50MHz	-	100	120	ps
			100MHz	-	100	120	ps
		$V_{DD} = 2.5V$ , $Q_D, Q_{C1}, Q_{ref}$	25MHz	-	90	120	ps
			125MHz/ 156MHz	-	90	130	ps
Jitter	RMS Phase Jitter	3.3V Operation $Q_D, Q_C, Q_{ref}$ (125MHz), 12k~20MHz $SS1 = SS0 = 1$	-	0.5	-	ps	
		2.5V Operation $Q_D, Q_C, Q_{ref}$ (125MHz), 12k~20MHz $SS1 = SS0 = 1$	-	1	-	ps	

**Differential DC Input Characteristics** (Over Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I <sub>IH</sub>	Input High Current, IN-	V <sub>IN</sub> = V <sub>DD</sub> =3.465V	-	-	5	μA
	Input High Current, IN+		-	-	45	μA
I <sub>IL</sub>	Input Low Current, IN-	V <sub>IN</sub> = 0V	-45	-	-	μA
	Input Low Current, IN+		-5	-	-	μA
V <sub>COMMON</sub>	Common Mode Voltage Range	-	0.2	-	V <sub>DD</sub> -0.925V	V
V <sub>PK</sub>	Peak-to-Peak Input Voltage Swing	-	0.15	-	1.3	V

1. V<sub>IL</sub> should not be less than -0.3V
2. Common mode voltage is defined as the cross point of the differential signal

**HCSL DC Electrical Characteristics** (Over Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>OH</sub>	Output High Voltage	All frequencies except at 250MHz	660	-	850	mV
		Only at 250MHz	600	-	850	mV
V <sub>OL</sub>	Output Low Voltage	-	-	-	150	mV
V <sub>CROSS</sub>	Absolute Crossing Point Voltages	-	250	-	550	mV
ΔV <sub>CROSS</sub>	Total Variation of V <sub>CROSS</sub> Overall Edges	-	-	-	140	mV
I <sub>OH</sub>	Output High Current with 475-Ohm resistor. Connected between I <sub>REF</sub> pin and GND	-	-	15	-	mA



**HCSL AC Switching Characteristics** <sup>(1, 2, 3)</sup> (Over Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$f_{error}$	Frequency Synthesis Error	-	-	-	0	ppm
$T_r / T_f$	Output Rise/Fall time (measured between 0.175V to 0.525V) <sup>2</sup>	-	175	-	700	ps
$\Delta T_r / \Delta T_f$	Rise and Fall Time Variation <sup>2</sup>	-	-	-	125	ps
$T_{skew}$	Output-to-Output Skew <sup>3</sup>	-	-	-	50	ps
$T_{DC}$	Output Duty Cycle <sup>3</sup>	-	47	-	53	%
$J_{HF-RMS}$	>1.5MHz-50MHz RMS jitter applying PCIe G2 jitter mask <sup>3</sup>	SS1= SS0 = 1	-	-	3.1	ps
	Using PCIe G3 jitter mask <sup>3</sup>	SS1= SS0 = 1, Low Frequency	-	-	3.0	ps
		SS1= SS0 = 1, High Frequency	-	0.5	1.0	ps
PSRR	Power Supply Noise Rejection Ratio with 20mVp-p Input Sine Wave 100kHz to 600kHz <sup>2</sup>	-	-	-50	-	dBc
PLL <sub>LBW</sub>	PLL Loop Bandwidth	-	-	350	-	kHz

1. Test configuration is  $R_s=33\Omega$ ,  $R_p=49.9\Omega$ , and 2pF

2. Measurement taken from Single-Ended Waveform

3. Measurement taken from Differential Waveform

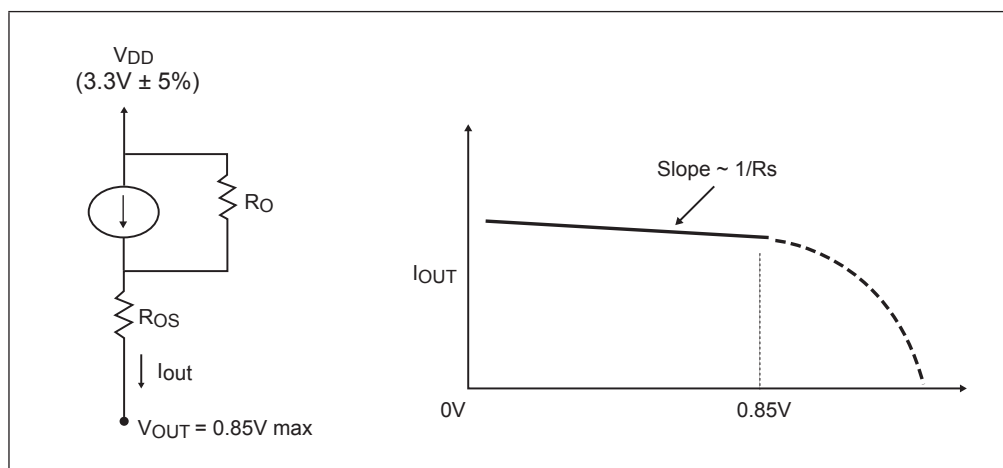
**LVPECL DC Electrical Characteristics** (Over Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{PP}$	Output peak-peak Voltage	-	0.4	-	1	V
$V_{OH}$	Output High Voltage	-	$V_{DD}-1.2$	-	$V_{DD}-0.7$	V
$V_{OL}$	Output Low Voltage	-	$V_{DD}-1.85$	-	$V_{DD}-1.55$	V

**LVPECL AC Switching Characteristics** (Over Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$T_r / T_f$	Rise/Fall time	20% to 80%, Differential	-	-	475	ps
$T_{DC}$	Duty Cycle	Differential	47	-	53	%
$J_{Phase}$	RMS Phase Jitter from 12kHz - 20MHz	At 3.3V with SS1= SS0 = 1	-	0.5	-	ps
		At 2.5V with SS1= SS0 = 1	-	1	-	ps

**HCSL Output Buffer Characteristics**

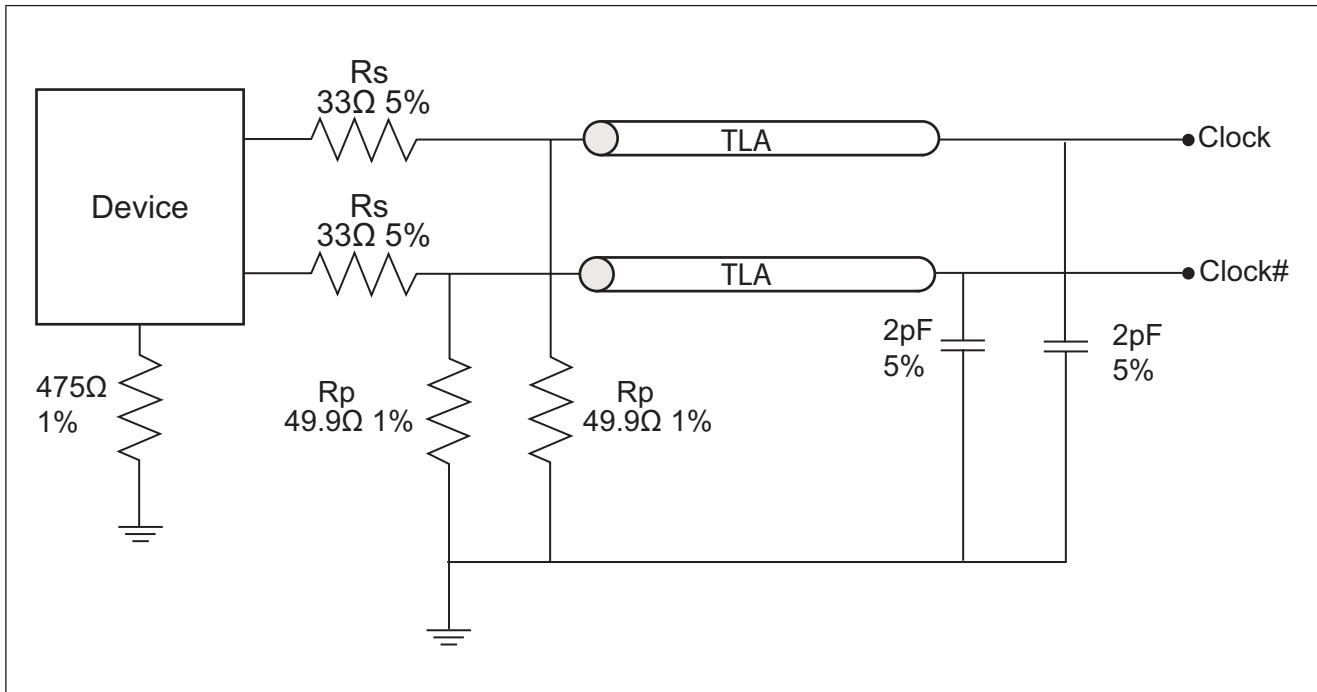


**Simplified Diagram of Current-Mode Output Buffer**

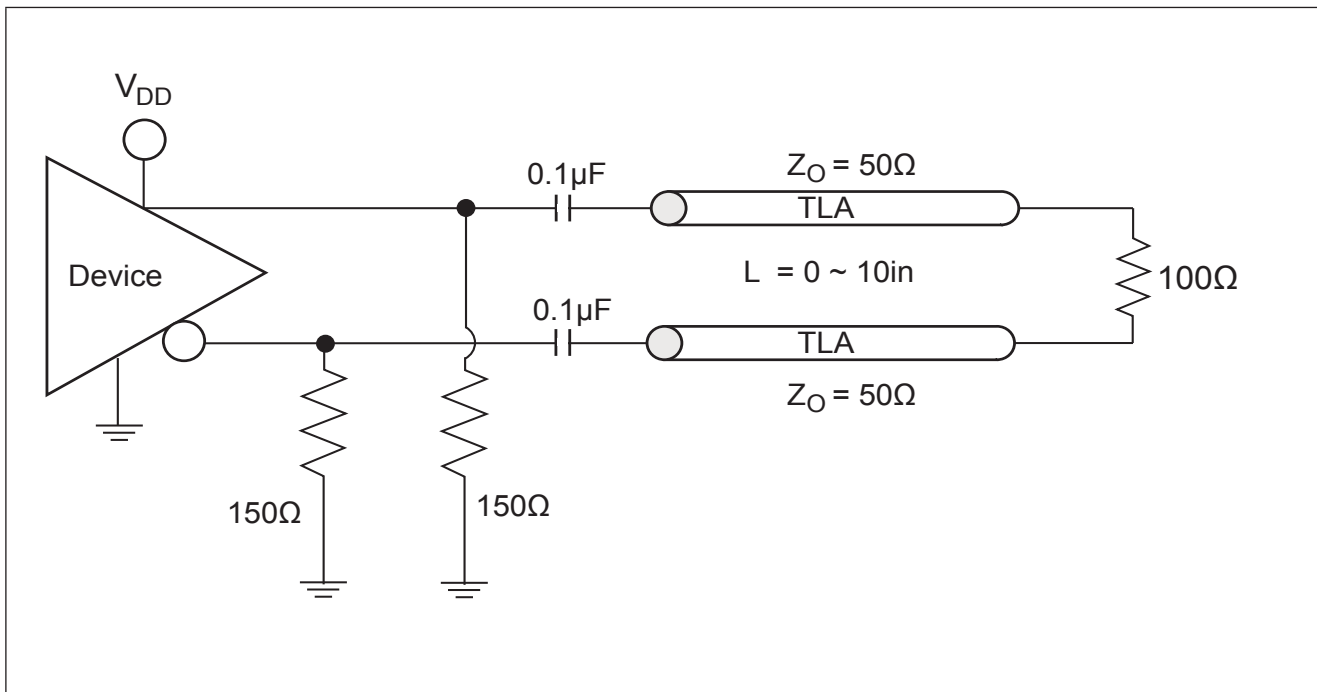
**HCSL Output Buffer Characteristics**

Symbol	Minimum	Maximum
$R_O$	$3000\Omega$	N/A
$R_{OS}$	unspecified	unspecified
$V_{OUT}$	N/A	$850mV$

**Configuration Test Load Board Termination for HCSL Output**



**Configuration Test Load Board Termination for LVPECL Output**

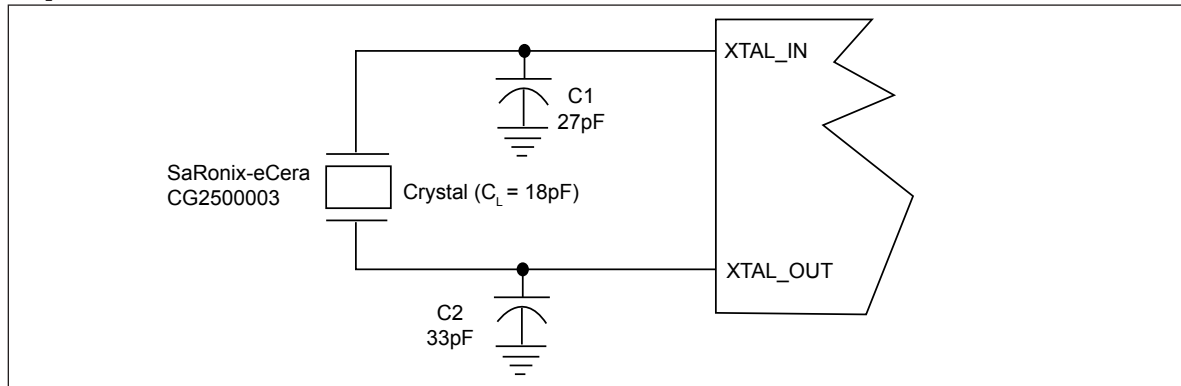


## Application Notes

### Crystal circuit connection

The following diagram shows PI6LC4833 crystal circuit connection with a parallel crystal. For the  $CL=18\text{pF}$  crystal, it is suggested to use  $C1=27\text{pF}$ ,  $C2=33\text{pF}$ .  $C1$  and  $C2$  can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

### Crystal Oscillator Circuit

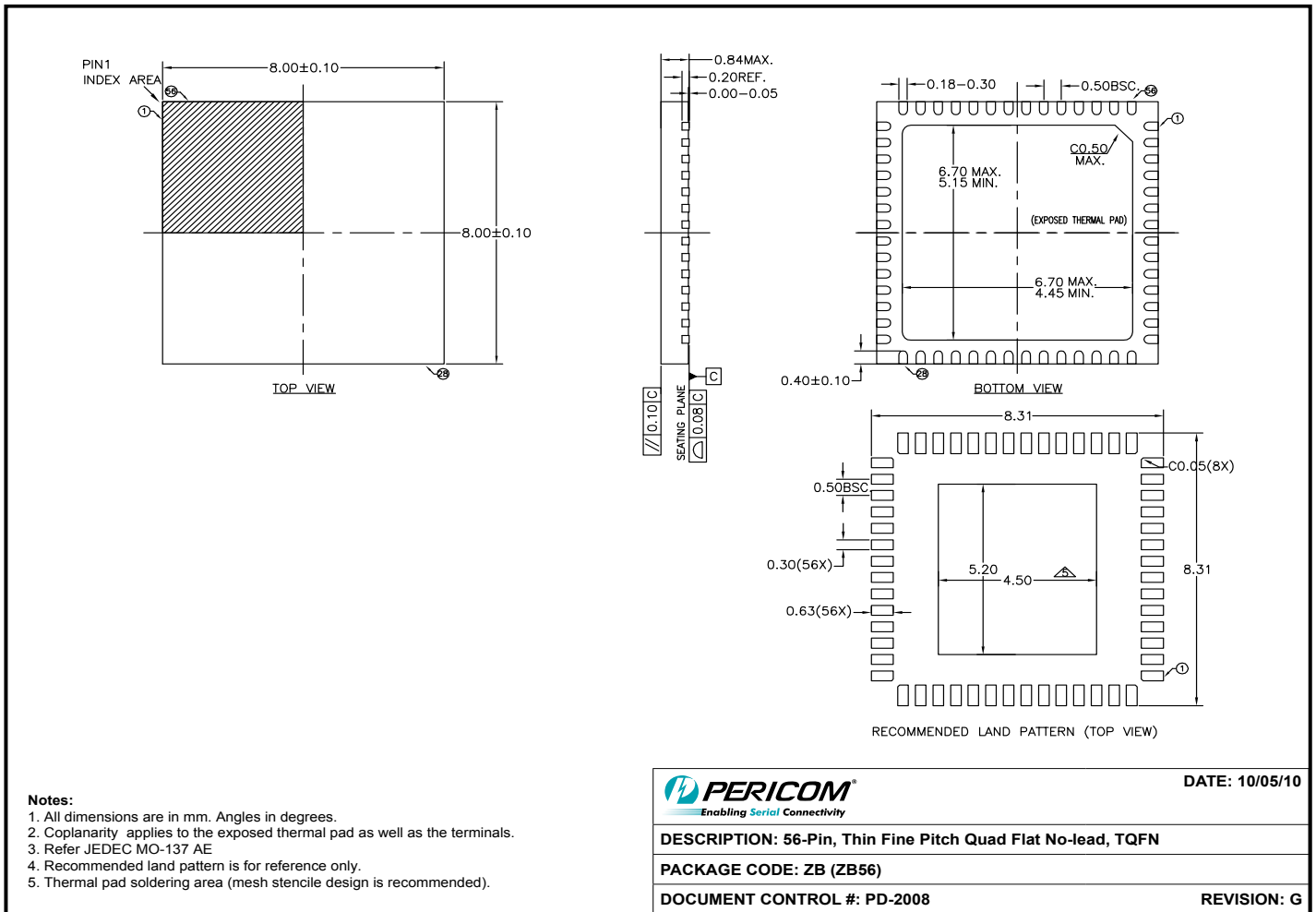


### Recommended Crystal Specification

**Pericom recommends:**

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M,  $CL=18\text{pF}$ ,  $\pm 30\text{ppm}$ , [http://www.pericom.com/pdf/datasheets/se/GC\\_GF.pdf](http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf)
- b) FY2500081, SMD 5x3.2(4P), 25M,  $CL=18\text{pF}$ ,  $\pm 30\text{ppm}$ , [http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
- c) FL2500047, SMD 3.2x2.5(4P), 25M,  $CL=18\text{pF}$ ,  $\pm 20\text{ppm}$ , <http://www.pericom.com/pdf/datasheets/se/FL.pdf>

**Packaging Mechanical: 56-Pin TQFN (ZB)**



**Ordering Information**

Ordering Code	Package Code	Package Type	Operating Temperature
PI6LC4833ZBIE	ZB	Pb-free & Green, 56-pin 315-mil wide TQFN	-40°C + 85°C

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)