CY2212

Direct Rambus Clock Generator (Lite)

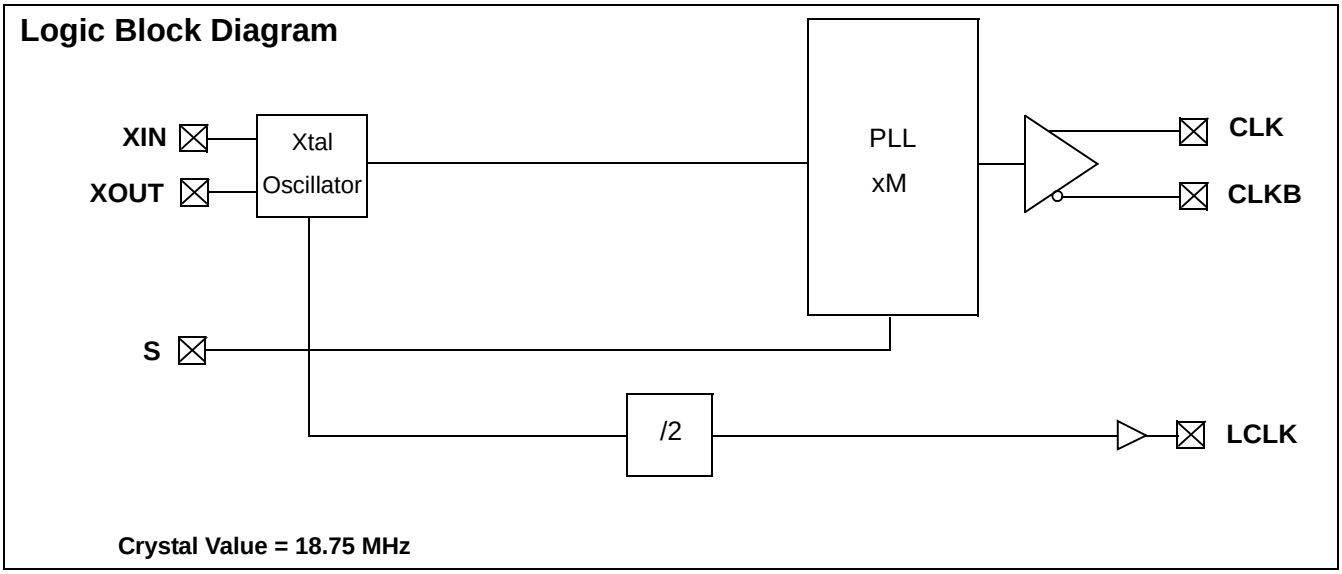
Features

- Direct Rambus Clock Support
- High Speed Clock Support
- Input Select Option
- Crystal Oscillator Divider Output
- Output Edge Rate Control
- 16-Pin TSSOP

Benefits

- One pair of differential output drivers
- 400 MHz and 300 MHz differential output frequencies
- Phase Locked Loop (PLL) multiplier select
- LCLK = XTAL/2, not driven by PLL
- Minimize EMI
- Space saving, low cost package

Logic Block Diagram



Pinouts

Figure 1. Pin Configuration – 16-Pin TSSOP Package

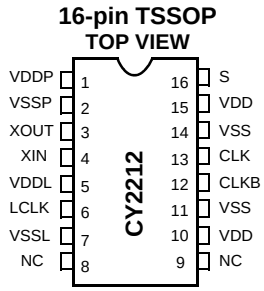


Table 1. Frequency Select Table

S	M (PLL Multiplier)	CLK, CLKB	LCLK
0	16	300 MHz	9.375 MHz
1	64/3	400 MHz	9.375 MHz

Table 2. Pin Description

Pin Name	Pin Number	Description
VDDP	1	3.3V Power Supply for PLL
VSSP	2	Ground for PLL
XOUT	3	Reference Crystal Feedback
XIN	4	Reference Crystal Input
VDDL	5	1.8V Power Supply for LCLK
LCLK	6	LVCMOS Output, x1/2 Crystal Frequency
VSSL	7	Ground for LCLK
NC	8	No Connect (Reserved for Test Mode)
NC	9	No Connect (Reserved for Test Mode)
VDD	10	3.3V Power Supply
VSS	11	Ground
CLKB	12	Output Clock (complement), Connect to Rambus Channel
CLK	13	Output Clock, Connect to Rambus Channel
VSS	14	Ground
VDD	15	3.3V Power Supply
S	16	PLL Multiplier Select Input, Pull-up Resistor Internal

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
$V_{DD,ABS}$	Max voltage on V_{DD}, V_{DDP}, or V_{DDL} with respect to ground	–0.5	4.0	V
$V_{I, ABS}$	Max voltage on any pin with respect to ground	–0.5	V_{DD} + 0.5	V
$V_{IL, ABS}$	Max voltage on LCLK with respect to ground	–0.5	V_{DDL} + 0.5	V

Crystal Requirements

These are the requirements for the recommended crystal to be used with the CY2212 DRCG Lite clock source. The crystal load capacitance is internally set to 11 pF.

Crystal Requirements

Parameter	Description	Min	Max	Unit
X_F	Frequency	14.0625	18.75	MHz
X_{FTOL}	Frequency Tolerance[1]	–15	15	ppm
X_{EQRES}	Equivalent Resistance[2]		100	Ω
X_{TEMP}	Temperature Drift[3]		10	ppm
X_{DRIVE}	Drive Level	0.01	1500	µW
X_{MI}	Motional Inductance	20.7	25.3	mH
X_{IR}	Insulation Resistance	500		MΩ
X_{SAR}	Spurious Attenuation Ratio[4]	3		dB
X_{OS}	Overtone Spurious	8		dB

Notes
1. At 25°C ± 3°C.
2. CL = 10 pF.
3. –10°C to 75°C.
4. At X_F ± 500 kHz.

DC Electrical Specification

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.04	3.56	V
V_{DDL}	LCLK Supply Voltage	1.7	2.1	V
T_A	Ambient Operating Temperature	0	70	°C
V_{IL}	Input Signal Low Voltage At Pin S	–	0.35	V_{DD}
V_{IH}	Input Signal High Voltage At Pin S	0.65	–	V_{DD}
R_{PUP}	Internal Pull Up Resistance	10	100	kΩ

AC Electrical Specifications

Parameter	Description	Min	Typ	Max	Unit
$f_{XTAL,IN}$	Input Frequency at Crystal Input[5]	14.0625	–	18.75	MHz
$C_{IN,CMOS}$	Input Capacitance at S Pin[6]	–	–	10	pF
C_{XTAL}	Crystal Load Capacitance	–	11	–	pF

Notes
5. Nominal condition with 18.75 MHz crystal.
6. Capacitance measured at Freq = 1 MHz, DC Bias = 0.9V, and VAC < 100 mV.

DC Device Specifications

Parameter	Description	Min	Max	Unit
V_{CM}	Differential Output Common Mode Voltage	1.35	1.75	V
V_X	Differential Output Crossing Point Voltage	1.25	1.85	V
V_{COS}	Output Voltage Swing (P-P Single-Ended)[7]	0.4	0.7	V
V_{COH}	Output High Voltage	–	2.1	V
V_{COL}	Output Low Voltage	1.0	–	V
r_{OUT}	Output Dynamic Resistance (at Pins)[8]	12	50	Ω
V_{LOH}	LCLK Output High Voltage at I_{OH} = –10 mA	V_{DDL} – 0.45V	V_{DDL}	V
V_{LOL}	LCLK Output Low Voltage at I_{OL} = 10 mA	0	0.45	V

State Transition Characteristics

Specifies the maximum settling time of the CLK, CLKB, and LCLK outputs from device power up. For V_{DD}, V_{DDP}, and V_{DDL} any sequences are allowed to power up and power down the CY2212 DRCG Lite.

State Transition Characteristics

From	To	Transition Latency	Description
$V_{DD}/V_{DDL}/V_{DDP}$ On	CLK/CLKB/LCLK Normal	3 ms	Time from $V_{DD}/V_{DDL}/V_{DDP}$ is applied and settled to CLK/CLKB/LCLK outputs settled.

Notes
7. $V_{COS} = V_{OH} – V_{OL}$.
8. $r_{OUT} = \Delta V_O / \Delta I_O$. This is defined at the output pins, not at the measurement point of Figure 4.

AC Device Specifications

Parameter	Description	Min	Max	Unit
t_{CYCLE}	Clock Cycle Time	2.5	3.33	ns
t_J	Jitter Over 1–6 Clock Cycles at 400 MHz[9]	–	100	ps
	Jitter Over 1–6 Clock Cycles at 300 MHz[9]	–	140	ps
t_{JL}	Long-Term Jitter at 400 MHz	–	300	ps
	Long-Term Jitter at 300 MHz	–	400	ps
DC	Long-Term Average Output Duty Cycle	45%	55%	t_{CYCLE}
$t_{DC,ERR}$	Cycle-Cycle Duty Cycle Error at 400 MHz	–	50	ps
	Cycle-Cycle Duty Cycle Error at 300 MHz	–	70	ps
t_{CR}, t_{CF}	Output Rise and Fall Times (Measured at 20%–80% of oUtput Voltage)	250	500	ps
$t_{CR, CF}$	Difference Between Output Rise and Fall Times on the Same Pin of a Single Device (20%–80%)	–	100	ps
BW_{LOOP}	PLL Loop Bandwidth	50 kHz (–3 dB)	8 MHz (–20 dB)	
$t_{CYCLE,L}$	LCLK Clock Cycle Time	106.6	142.2	ns
t_{LR}, t_{LF}	LCLK Output Rise and Fall Time	–	1	ns
$t_{JC,L}$	LCLK Cycle Jitter[10]	–0.8	0.8	ns
$t_{J10,L}$	LCLK 10-Cycle Jitter[10, 11]	$–1.1 * t_{JC,L}$	$1.1 * t_{JC,L}$	ns
DC_L	LCLK Output Duty Cycle	40%	60%	$t_{CYCLE,L}$

Notes
9. Output short-term jitter specification is peak-peak and defined in Figure 11.
10. LCLK cycle jitter and 10-cycle jitter are defined as the difference between the measured period and the nominal period as defined on page 11.
11. LCLK 10-cycle jitter specification is based on the measured value of LCLK cycle jitter as defined on page 11.

Functional Specifications

This section gives the detailed functional specifications of the device physical layer. These specifications refer to the logical and physical interfaces.

Crystal Input

The CY2212 receives its reference from an external crystal. Pin XIN is the reference crystal input, and pin XOUT is the reference crystal feedback. The parameters for the crystal are given on page 4 of this datasheet.

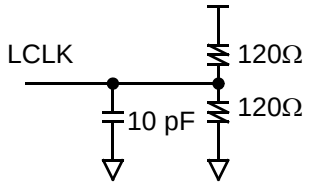
Select Input

There is only one select input, pin S. This pin selects the frequency multiplier in the PLL, and is a standard LVCMOS input. The S pin has an internal pull up resistor. The multiplier selection is given on Frequency Select Table on page 1 of this datasheet.

LCLK Output Driver

In addition to the Rambus clock driver outputs, there is another clock output driver. The LCLK driver is a standard LVCMOS output driver. Figure 2 below shows the LCLK output driver load circuit.

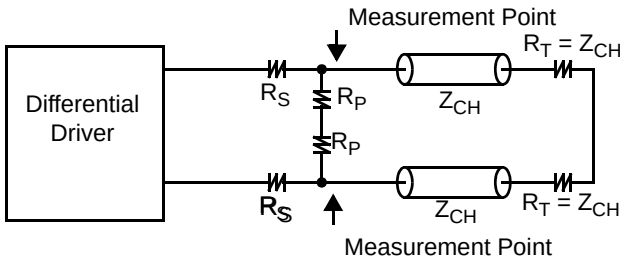
Figure 2. LCLK Test Load Circuit



RSL Clock Output Driver

Figure 3 shows the clock driver equivalent circuit.

Figure 3. Equivalent Circuit



The differential driver has a low output impedance in the range of about 20 Ω. The driver also produces a specified voltage swing on the channel. The nominal value of the channel impedance, Z_{CH}, is 28 Ω. Series resistor RS and parallel resistor RP are used to set the voltage swing on the channel. The driver output characteristics are defined together with the external components, and the output clock is specified at the measurement point indicated in Figure 3. The complete set of external components for the output driver, including edge-rate filter capacitors required for system operation, are shown in Figure 4. The values for the external components are given in Table 1.

The output clocks drive transmission lines, potentially long lines. Since circuit board traces act as lossy, imperfectly terminated transmission lines with some discontinuities, there are reflections generated that travel back to the DRCG Lite output driver. If the output impedance does not match ZCH, secondary reflections are generated that add to position dependent timing uncertainty. Therefore, the CY2212 not only provides proper output voltage swings, but also provides a well-matched output impedance. The driver impedance, R_{OUT}, is in series with R_S, and the combination is in parallel with R_P.

The clock driver is specified as a black-box at the packaged pins. The output characteristics are measured after the series resistance, R_S. The outputs are terminated differentially, with no applied termination voltage.

Figure 4 shows the clock driver implemented as a push-pull driver. When stimulating the output driver, the transmission lines shown in Figure 4 can be replaced by a direct connection to the termination resistors, R_T. The values for the external components are given in Table 1.

As mentioned previously, the clock driver's output impedance matches the channel impedance. To accomplish this, each of the output driver devices are sized to have an R_{OUT} of about 20 Ω when fully turned on. R_{OUT} is the dynamic output resistance, and is defined in the DC Device Specifications table on page 4 of this datasheet. Since R_{OUT} is in series with R_S, and that combination is in parallel with R_P, the effective output impedance is given by:

$$R_P(R_S + R_{OUT})/(R_P + R_S + R_{OUT}).$$

This calculation results in an effective output impedance of about 27 Ω for the values listed in Table 1. Since the total impedance is dominated by the external resistors, a large possible range of R_{OUT} is allowed. When the output is transitioning, the impedance of the CMOS devices increases dramatically. The purpose of R_P is to limit the maximum output impedance during output transitions.

In order to control signal attenuation and EMI, clock signal rise/fall times must be tightly controlled. Therefore, external filter capacitors C_F are used to control the output slew rate. In addition, the capacitor C_{MID} is used to provide AC ground at the mid-point of the R_P resistors.

Table 1 gives the nominal values of the external components and their maximum acceptable tolerance, assuming ZCH = 28 Ω.

Figure 4. Output Driver

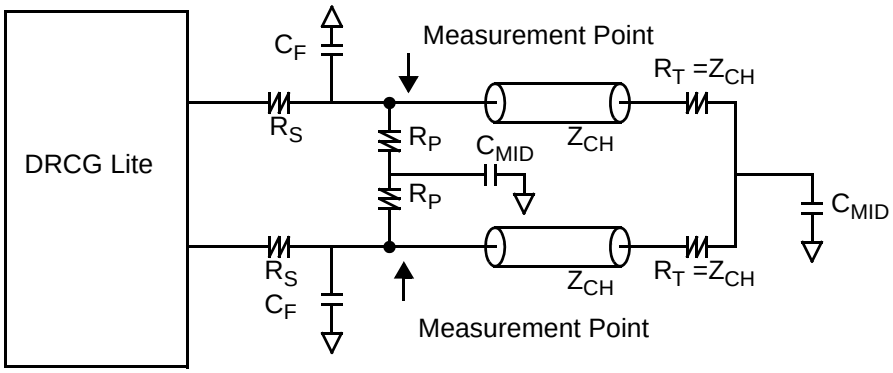
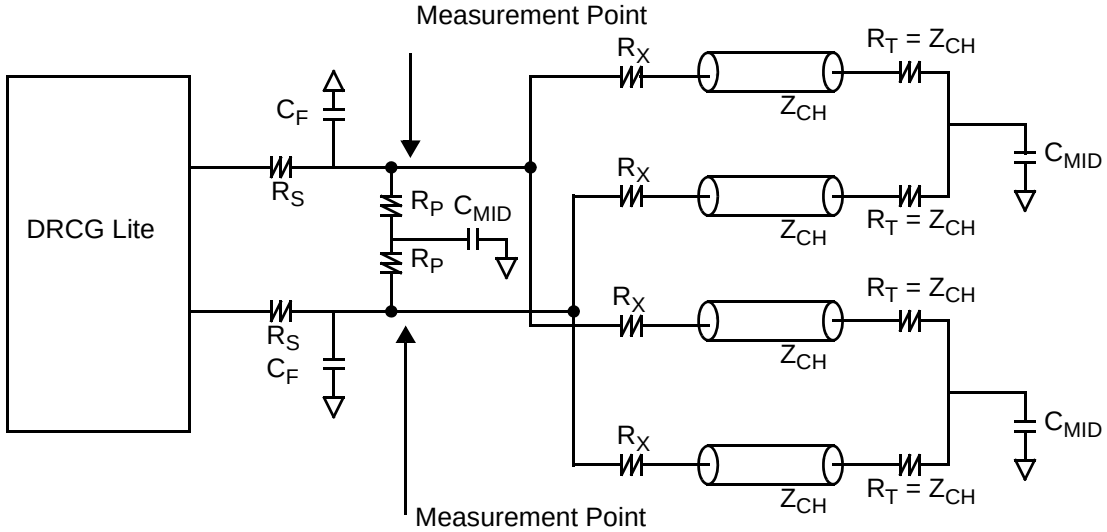


Table 3. Output External Component Values

Parameter	Description	Value	Tolerance	Unit
R_S	Series Resistor	68	±5%	Ω
R_P	Parallel Resistor	39	±5%	Ω
C_F	Edge-rate Filter Capacitor	15	±10%	pF
C_{MID}	AC Ground Capacitor	0.01	±20%	µF

Figure 5. Output Driving Two Channels



Dual Channel Output Driver

Figure 5 shows the clock driver driving two high-impedance channels. The purpose of the series resistors R_X is to decouple the two channels, and prevent noise from one channel from coupling onto the second channel. With Z_{CH} = 40 Ω and the series resistor set to R_X = 16 Ω, the channel becomes an effective 56-Ω channel. The two channels in parallel can be treated as a single 28-Ω channel, and all of the external component values listed in Table 3 can be used.

Signal Waveforms

A physical signal that appears at the pins of the device is deemed valid or invalid depending on its voltage and timing relations with other signals. This section defines the voltage and timing waveforms for the input and output pins of the CY2212. The Device Specifications tables list the specifications for the device parameters that are defined here.

Input and Output voltage waveforms are defined as shown in Figure 6. Both rise and fall times are defined between the 20% and 80% points of the voltage swing, with the swing defined as V_H – V_L. For example, the output voltage swing $V_{COS} = V_{OH} – V_{OL}$.

The device parameters defined according to Figure 6 are as follows.

Table 4. Definition of Device Parameters

Parameter	Definition
V_{OH}, V_{OL}	Clock output high and low voltages
V_{COS}	Clock output swing $V_{COS} = V_{OH} – V_{OL}$
V_{CM}	Common-mode voltage $V_{CM} = (V_{OH} – V_{OL})/2$
V_{IH}, V_{IL}	Vdd LVCMOS input high and low voltages
t_{CR}, t_{CF}	Clock output rise and fall times
t_{CR}, C_F	Clock output rise/fall time delta $t_{CR,CF} = t_{CR} – t_{CF}$

Figure 6. Voltage Waveforms

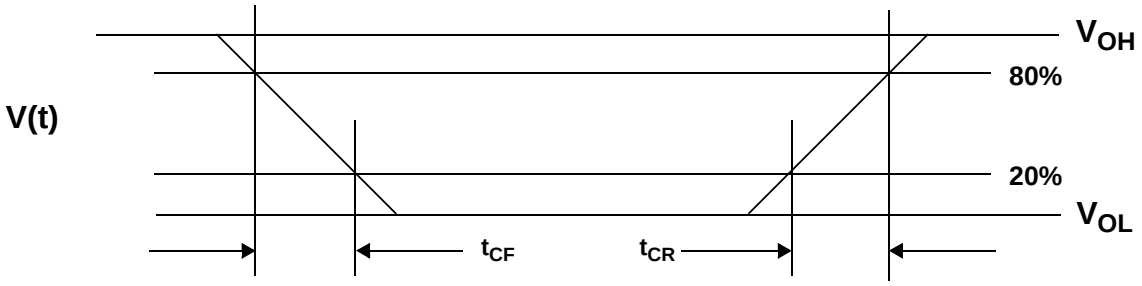


Figure 7. Crossing Point Voltage

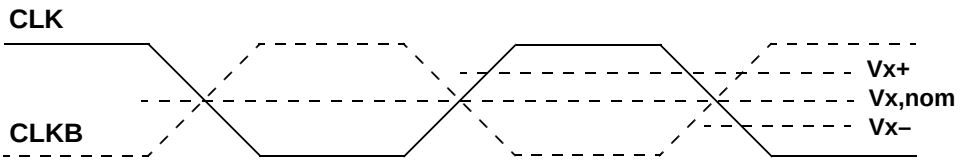


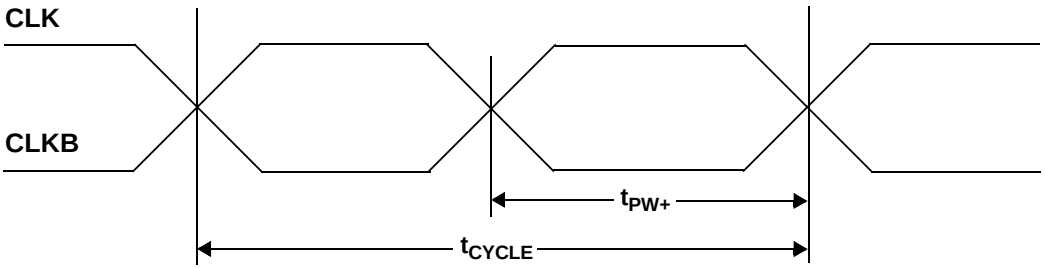
Figure 7 shows the definition of output crossing point. The nominal crossing point between the complementary outputs is defined to be at the 50% point of the DC voltage levels. There are two crossing points defined, Vx+ at the rising edge of CLK and Vx– at the falling edge of CLK. For some clock waveforms, both Vx+ and Vx– might be below Vx, nominal (for example, if t_{CR} is larger than t_{CF}). Vx is defined as the differential output crossing point voltage.

Figure 8 shows the definition of long-term duty cycle, which is simply the waveform high-time divided by the cycle time (defined at the crossing point). Long-term duty cycle is the average over many (>10,000) cycles. Short-term duty cycle is defined in the next section. DC is defined as the output clock long-term duty cycle.

Jitter

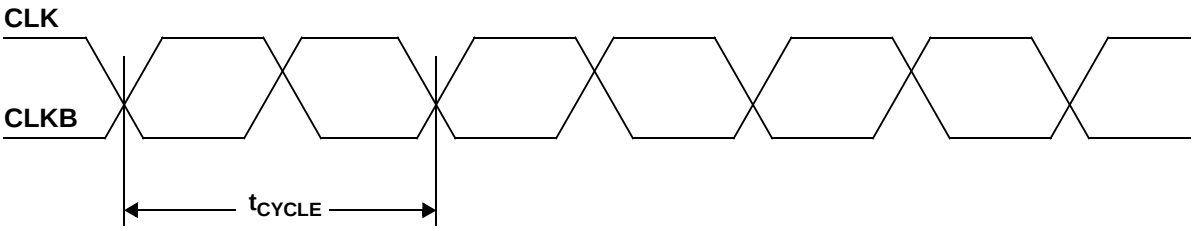
This section defines the specifications that relate to timing uncertainty (or jitter) of the input and output waveforms. Figure 9 shows the definition of long-term jitter with respect to the falling edge of the CLK signal. Long-term jitter is the difference between the minimum and maximum cycle times. Equal requirements apply for rising edges of the CLK signal. t_{JL} is defined as the output long-term jitter.

Figure 8. Duty Cycle



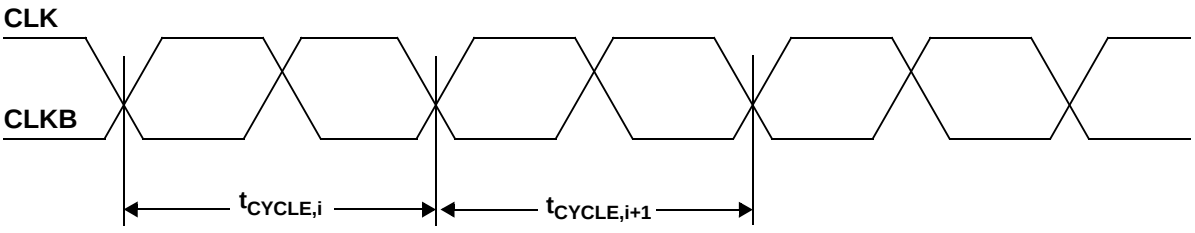
$DC = t_{PW+} / t_{CYCLE}$

Figure 9. Long-Term Jitter



$t_{JL} = t_{CYCLE,max} - t_{CYCLE,min\ over\ 10000\ cycles}$

Figure 10. Cycle-to-Cycle Jitter



$t_J = t_{CYLCE,i} - t_{CYCLE,i+1\ over\ 10000\ consecutive\ cycles}$

Figure 10 shows the definition of cycle-to-cycle jitter with respect to the falling edge of the CLK signal. Cycle-to-cycle jitter is the difference between cycle times of adjacent cycles. Equal requirements apply for rising edges of the CLK signal. t_J is defined as the clock output cycle-to-cycle jitter.

Figure 11 shows the definition of four-cycle short-term jitter. Short-term jitter is defined with respect to the falling edge of the CLK. Four-cycle short-term jitter is the difference between the cumulative cycle times of adjacent four cycles. Equal requirements apply for rising edges of the CLK signal. Equal requirements also apply for two-cycle short-term jitter and three-cycle short-term jitter, and for five-cycle short-term jitter and six-cycle short-term jitter. t_J is defined as the clock output short-term jitter over 2, 3, 4, 5, or 6 cycles.

The purpose of this definition of short-term jitter is to define errors in the measured time (for example, $t_{4CYCLE,i}$) vs. the expected time. The purpose for measuring the adjacent time $t_{4CYCLE, i+1}$ is only to help determine the expected time for $t_{4CYCLE, i}$. Alternate methods of determining t_J are possible, including comparing the measured time to an expected time based on a local cycle time, $t_{CYCLE,LOCAL}$. This local cycle time could be determined by taking the rolling average of a group of cycles (5–10 cycles) preceding the measured cycles. However, it is important to differentiate this rolling average from the average cycle time, $t_{CYCLE,AVG}$, which is the average cycle time over the 10,000 cycles. Using a long-term average instead of a rolling average would define t_J as a long-term jitter instead of a short-term jitter, and would normally giver overly pessimistic results.

Figure 12 shows the definition of cycle-to-cycle duty cycle error. Cycle-to-cycle duty cycle error is defined as the difference between high-times of adjacent cycles. Equal requirements apply to the low-times. $t_{DC,ERR}$ is defined as the clock output cycle-to-cycle duty cycle error.

Figure 11. Short-Term Jitter

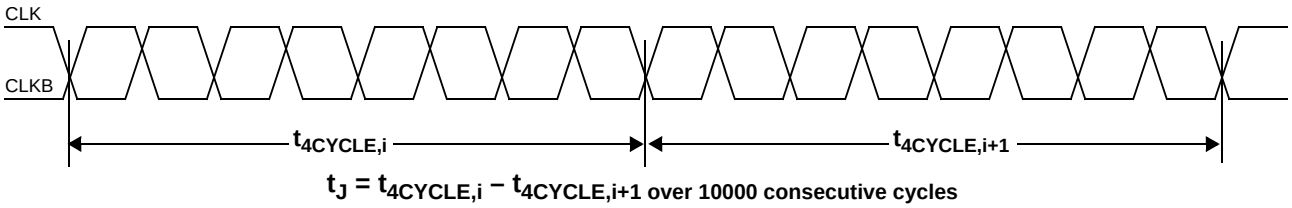


Figure 12. Cycle-to-Cycle Duty Cycle Error

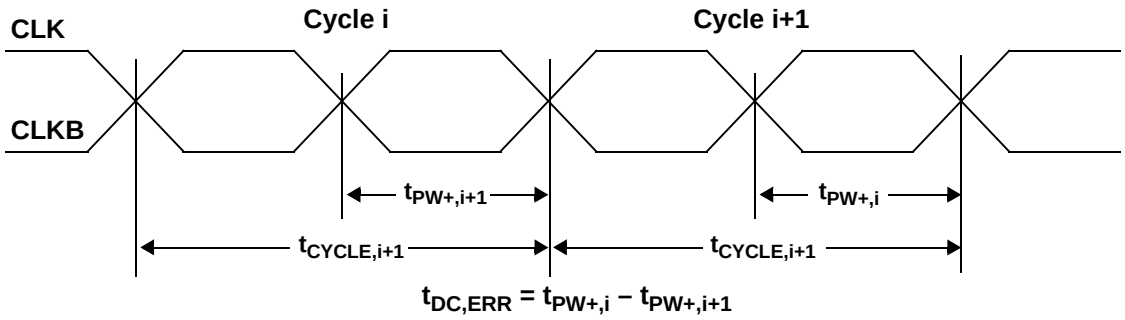


Figure 13. LCLK Jitter

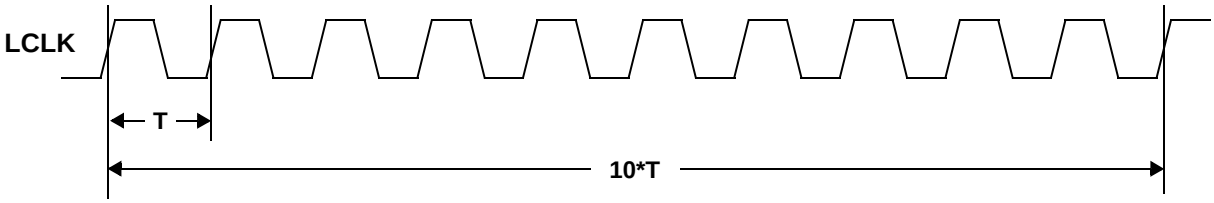


Figure 13 shows the definition of LCLK cycle jitter and LCLK 10-cycle jitter. These parameters apply to the LCLK output, and not to the Rambus channel clock outputs.

LCLK cycle jitter is the variation in the clock period, T, over a continuous set of clock cycles. The difference bet ween the maximum period and the nominal period in the set of clock cycles measured would be compared to the max spec listed in the AC Device Specifications on page 5. LCLK cycle jitter is measured between rising edges at 50% of the output voltage, and is measured continuously over 30,000 cycles.

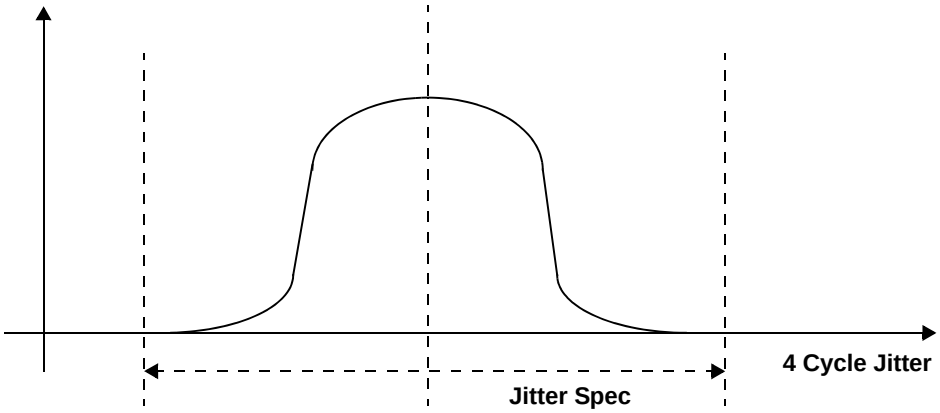
LCLK 10-cycle jitter is the variation in the time of 10 clock cycles, 10*T, where T is the clock period. The difference between the maximum 10-cycle period and the nominal 10-cycle period in the set of clock cycles measured would be compared to the max spec listed in the AC Device Characteristics Table on page 5. Note that the specification for LCLK 10-cycle jitter is defined based on the measured value of LCLK cycle jitter. LCLK 10-cycle jitter is measured between the first rising edge and the tenth rising edge at 50% of the output voltage, and is measured over 30,000 continuous cycles. $t_{JC,L}$ is defined as the LCLK output cycle jitter, and $t_{J10,L}$ is defined as the LCLK output jitter over 10 cycles.

Measurement

The short-term jitter specification (over one to six cycles) for the clock source is given as t_J, as previously shown. Jitter should be measured using a jitter measurement system that has the flexibility of measuring cycle-to-cycle jitter as a function of cycle count. It is important that the short-term jitter be measured over consecutive cycles in order to prevent long-term drift from causing overly pessimistic results. When measured over 10,000 consecutive cycles, the short-term jitter measurements generate large amounts of data which can be viewed in a histogram. Figure 14 shows an example histogram of data from a 4-cycle short-term jitter measurement, with results that are within spec lines for t_J. Note that the jitter is specified as peak-to-peak, so the center of the histogram need not be exactly zero.

Further details of jitter measurement methodologies are given in the Rambus *DRCG-Lite Specification* Appendix A published by Rambus, Inc.

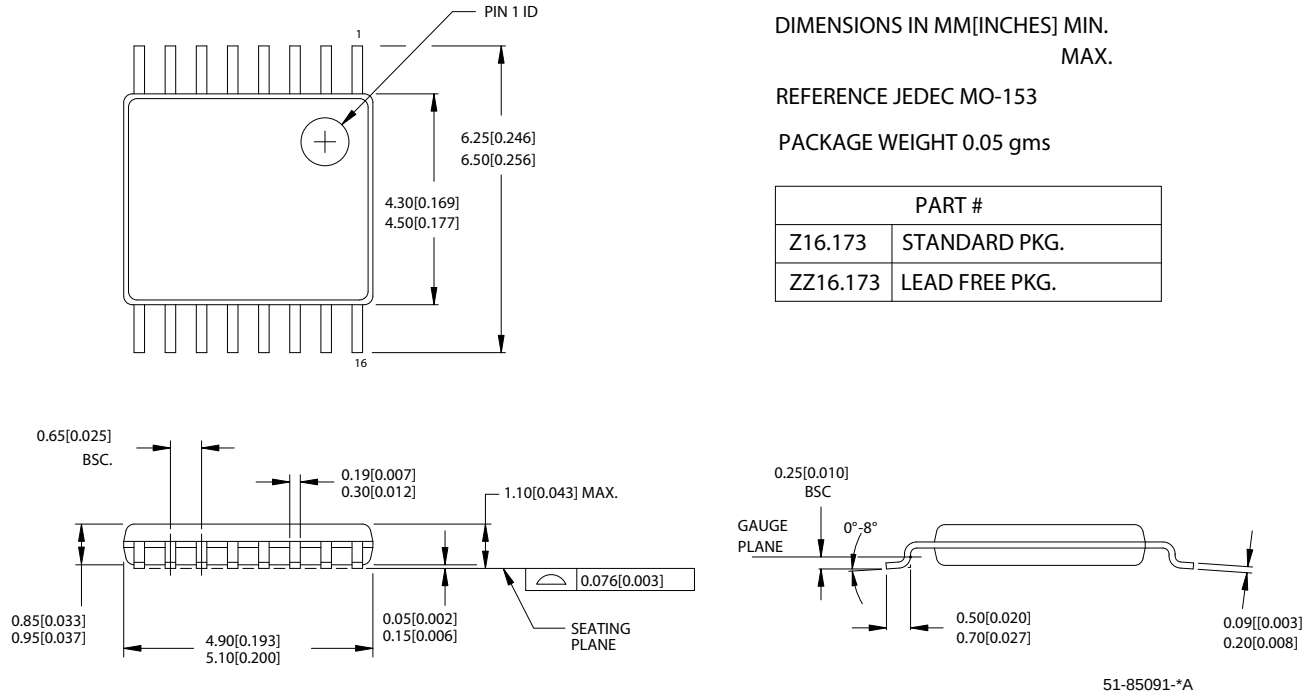
Figure 14. Example Jitter Measurement Histogram



Ordering Code	Package Type	Operating Range
CY2212ZXC-2	16-Pin TSSOP, Pb-free	Commercial
CY2212ZXC-2T	16-Pin TSSOP, Pb-free –Tape and Reel	Commercial

Package Drawing and Dimensions

Figure 15. 16-Pin TSSOP 4.40 mm Body Z16.173



Document History Page

Document Title: CY2212 Direct Rambus Clock Generator (Lite) Document Number: 38-07466				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	117801	CKN	12/10/02	New datasheet
*A	308300	RGL	See ECN	Corrected Ordering Info from -1 to -2 Added Lead Free Devices (-2) Added CXTAL specs in the AC Electrical specifications table
*B	2762435	KVM	09/11/09	Remove CY2212ZC-2 and CY2212ZC-2T from Ordering Information table

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