ZL30641 - ZL30645

Line Card Timing ICs with up to 5 Channels, 10 Inputs, 20 Outputs Product Brief

Features

Highlights

- Up to five independent clock channels
- Any-to-any frequency conversion per channel
- Inputs: up to 10, differential or single-ended
- Outputs: up to 10 differential, up to 20 CMOS
- Output jitter 100 fs_{RMS} typical for 156.25 MHz 12 kHz to 20 MHz
- Core power consumption <0.9W
- MiToDSync™ 1-wire time-of-day interface in/out
- MiToDBasic™ 3-wire time-of-day interface out

Input Clocks

- Accepts up to 10 differential or CMOS inputs
- Any input frequency from 1 kHz to 1250 MHz
- Per-input activity and frequency monitoring
- Automatic or manual reference switching
- Revertive or nonrevertive switching
- Any input can be a 0.5 Hz to 8 kHz Sync input for Ref-Sync frequency/phase/time locking
- Any input can be a clock with embedded Sync
- Input phase measurement, 1 ps resolution
- Per-input phase adjustment, 1 ps resolution

Up to 8 DPLLs

- Hitless reference switching
- High-resolution holdover averaging
- Per-DPLL phase adjustment, 1 ps resolution
- Programmable bandwidth, tracking range, phase-slope limiting, frequency-change limiting and other advanced features
- Locking to gapped-clock input signals

Output Clocks

- Any frequency 0.5 Hz to 750 MHz
- Each OUTP/N pair can be LVDS, LVPECL, 2xCMOS, Low-V_{CM}, or programmable differential
- In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125 MHz and 25 MHz)
- VDD per output pair, CMOS voltages 1.8V to 3.3V
- Per-synth phase adjustment, 1 ps resolution
- Per-output duty cycle adjustment
- Precise output alignment circuitry and per-output phase adjustment
- Per-output enable/disable and glitchless start/stop (stop high or low)

Local Oscillator

- Operates from a single oscillator 9.72 MHz to 400 MHz
- Very-low-jitter applications can connect a TCXO or OCXO as the stability reference and a low-jitter XO as the jitter reference

General Features

- Automatic self-configuration at power-up from internal Flash memory, 7 configurations
- Input-to-output alignment <100 ps
- Fast Ref-Sync locking for frequency and 1PPS phase alignment with lower-cost oscillator
- Numerically controlled oscillator behavior in each DPLL and each synthesizer
- Easy-to-configure design requires no external VCXO or loop filter components
- 5 GPIO pins with many possible behaviors, each REF can be GPI, each OUT can be GPO
- SPI or I^2C processor Interface
- 1.8V and 3.3V core VDD voltages
- Easy-to-use evaluation/programming software

Applications

- Line card timing ICs for SyncE, SyncE+1588, routers, switches, OTN, and other carrier-grade systems
- Wireless base stations (3G, W-CDMA, 4G/LTE, LTE-A, 5G)
- Remote Radio Unit (RRU), Remote Access Networks (RAN), small cells, wireless backhaul, wireless repeaters

1.0 BLOCK DIAGRAM

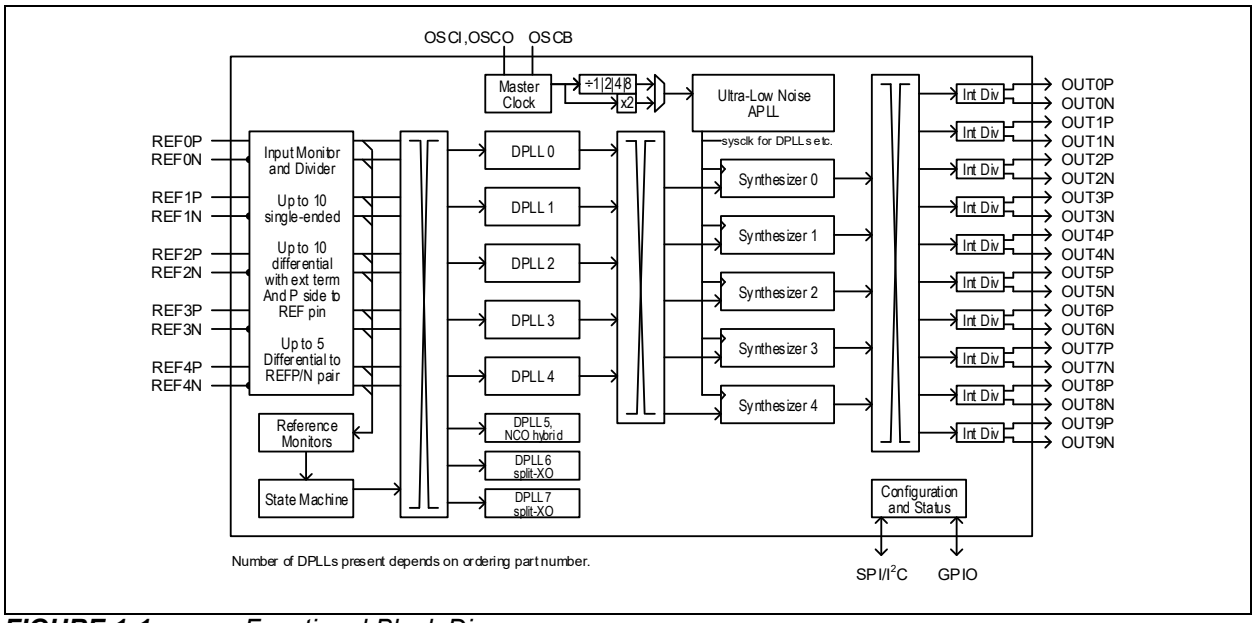

FIGURE 1-1: *Functional Block Diagram.*

2.0 APPLICATION EXAMPLE

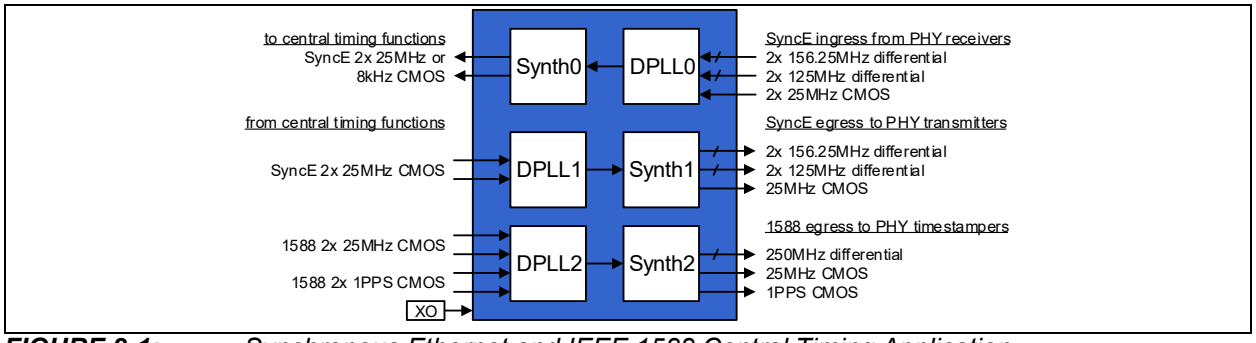

FIGURE 2-1: *Synchronous Ethernet and IEEE 1588 Central Timing Application.*

3.0 DETAILED FEATURES

3.1 General

- Up to five independent clock channels
- Operates from a single crystal resonator or clock oscillator
  - ≥48 MHz for lowest jitter
  - 9.72 MHz to 400 MHz total frequency range
- Configurable via SPI or I^2C interface
- Internal nonvolatile memory
  - Factory-configurable power-on configuration
  - Multiple time writeable/re-writeable
- Default settings can be overridden using SPI/I^2C

3.2 Input Block Features

- Ten input reference pins; each can accept a CMOS signal or the POS side of a differential pair; or two can be paired to accept both sides of a differential pair (see Figure 6-3)
- Any input can be a SYNC signal (0.5 Hz to 8 kHz) for Ref-Sync frequency/phase/time locking
- Any input can be a clock with embedded Sync signal (0.5 Hz to 1 kHz, duty cycle distortion for Sync)
- Any input can be a MiToDSync signal carrying one to three channels of frequency/phase/ToD information
- Input clocks can be any frequency from 1 kHz up to 1250 MHz (300 MHz max for CMOS inputs)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable frequency and single-cycle monitors
- Single-cycle monitor can quickly disqualify a reference when measured period is incorrect
- Frequency measurement and monitoring (coarse, fine, and frequency-step monitors)
- Optional input clock invalidation on GPIO or GPI assertion to react to LOS signals from PHYs
- Input phase measurement, 1 ps resolution
- Per-input phase adjustment, 1 ps resolution
- Each REF pin can be a GPI (general-purpose input)

3.3 DPLL Features

- Up to eight DPLLs: up to five for clock I/O channels, one for NCO-hybrid mode (SyncE assist), and two for locking to OCXOs for split-XO configuration
- Very high-resolution DPLL architecture
- State machine automatically transitions among freerun, tracking, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 5 Hz to 470 Hz
- Fast frequency/phase/time lock capability for clock+1PPS input references
- Programmable phase-slope limiting (PSL)
- Programmable frequency rate-of-change limiting (FCL)
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching
- Per-DPLL phase adjustment, 1 ps resolution
- High-resolution frequency and phase measurement (4e-15 and 1 ps)
- Fast detection of input clock failure and transition to holdover mode
- Supports holdover compensation for oscillator aging and temperature changes by learning oscillator characteristics during locked operation
- Time-of-Day registers: 48-bit seconds, 32-bit nanoseconds, writeable on input PPS edge

3.4 Synthesizer Features

- Five next-generation low-jitter, low-power, any-frequency synthesizers
- A total of five output frequency families
- Any-to-any frequency conversion with 0 ppm error
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Jitter suitable for OC-192, STM-64, and 1G, 10G, 40G, 100G, and 400G Ethernet jitter requirements

3.5 Output Clock Features

- Up to 20 single-ended outputs, up to 10 differential outputs, from any synthesizer
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 0.5 Hz to 750 MHz (250 MHz max for CMOS)
- Output jitter 100 fs_{RMS} typical for 156.25 MHz and many other frequencies (12 kHz to 20 MHz)
- In CMOS mode, the OUTxN frequency can be an integer divisor of the OUTxP frequency (Example 1: OUT3P 125 MHz, OUT3N 25 MHz. Example 2: OUT2P 25 MHz, OUT2N 1 Hz)
- Outputs directly interface (DC-coupled) with LVDS, LVPECL, HCSL, and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs, and other components
- Can produce PCIe Gen 1 to 5 clocks
- Each output pair can have clock plus embedded Sync signal (0.5 Hz to clock div 4)
- Each output pair can be MiToDSync signals carrying one to three channels of frequency/phase/ToD information
- Sophisticated output-to-output phase alignment
- Per-synthesizer phase adjustment, 1 ps resolution
- Per-output phase adjustment to accommodate trace delays or compensate for system routing paths
- Per-output duty cycle/pulse width configuration
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)
- Each OUT pin can be a GPO (general-purpose output)
- Each OUT pin can be a MiToDBasic data signal which can be combined with a MHz clock output and a 4 kHz sync output to form a 3-wire MiToDBasic interface carrying one channel of frequency/phase/ToD information

3.6 Local Oscillator

- Operates from a single oscillator (jitter reference for the device). Acceptable frequencies: 9.72 MHz to 400 MHz. Best jitter: ≥48 MHz.
- Very-low-jitter applications can connect a TCXO or OCXO (any frequency, any output jitter) as the stability reference and a low-cost low-jitter XO as the jitter reference
- This ability to have separate jitter and stability references greatly reduces the cost of the TCXO or OCXO (no jitter requirement, no high-frequency-requirement) and allows reuse of already-qualified TCXO and OCXO components
- Supports redundant TCXOs or OCXOs connected to two REF pins

3.7 General Features

- Automatic self-configuration at power-up from internal Flash memory
- Input-to-output alignment <200 ps with external feedback
- Fast Ref-Sync locking for frequency and 1PPS phase alignment with lower-cost oscillator
- Generates output SYNC signals: 1PPS (IEEE 1588), 2 kHz or 8 kHz (SONET/SDH), or other frequency
- JESD204B clocking: clock and SYSREF signal generation with skew adjustment
- Numerically controlled oscillator (NCO) behavior allows system software to steer DPLL frequency or synthesizer frequency with resolution better than 0.005 ppt
- Spread-spectrum modulation available in each synthesizer (PCIe compliant)
- Five general-purpose I/O pins each with many possible status and control options
- SPI or I^2C serial microprocessor interface

3.8 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the device quick and easy
- Generates configuration scripts
- Works with or without an evaluation board

4.0 PIN DIAGRAM

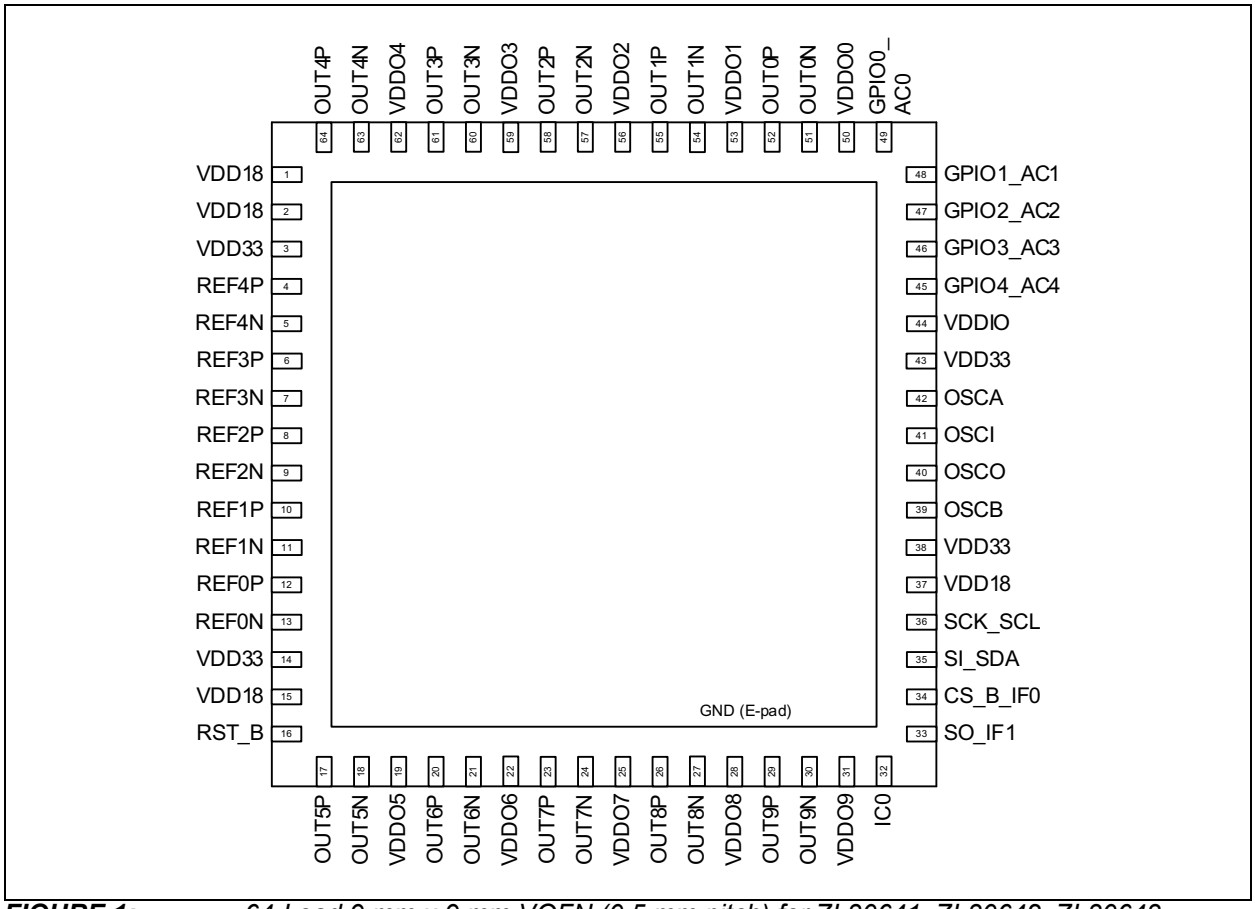

FIGURE 1: *64-Lead 9 mm x 9 mm VQFN (0.5 mm pitch) for ZL30641, ZL30642, ZL30643, ZL30644, ZL30645.*

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