



CYPRESS

PRELIMINARY

CY28412

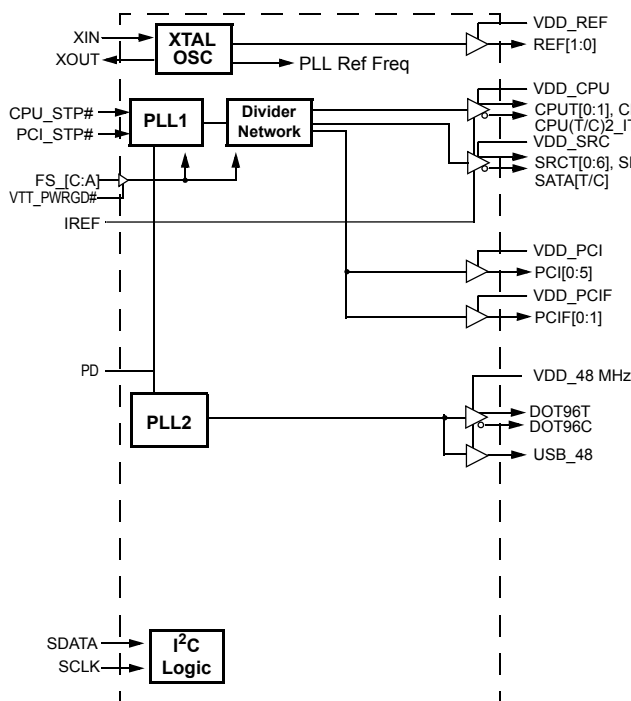
# Clock Generator for Intel® Grantsdale Chipset

## Features

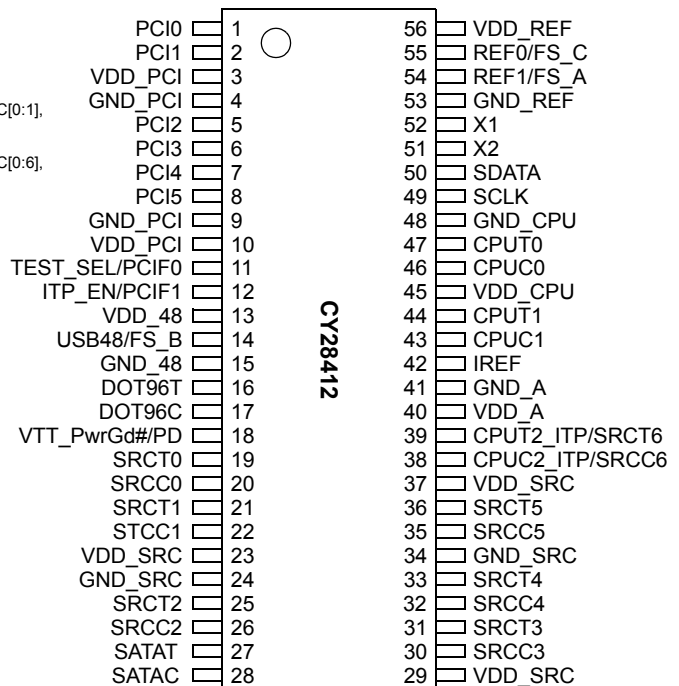
- Supports Intel® P4 and Prescott CPU
- Selectable CPU frequencies
- Differential CPU clock pairs
- 100-MHz differential SRC clocks
- 96-MHz differential dot clock
- 48-MHz USB clocks
- 33-MHz PCI clock
- Low-voltage frequency select input
- I<sup>2</sup>C Support with read back capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 56-pin SSOP package

CPU	SRC	PCI	REF	DOT96	USB_48
x2 / x3	x7 / x8	x 8	x 2	x 1	x 1

## Block Diagram



## Pin Configuration



56 SSOP

**Pin Definitions**

Pin No.	Name	Type	Description
47,46,44,43	CPUT/C	O, DIF	<b>Differential CPU clock outputs.</b>
39,38	CPUT2_ITP/SRCT6, CPUC2_ITP/SRCC6	O, DIF	<b>Selectable Differential CPU or SRC clock output.</b> ITP_EN = 0 @ VTT_PWRGD# assertion = SRC6 ITP_EN = 1 @ VTT_PWRGD# assertion = CPU2
16,17	DOT96T, DOT96C	O, DIF	<b>Fixed 96-MHz clock output.</b>
55, 54	REF0/FS_C, REF1/FS_A	I/O	14.318-MHz reference clock/3.3V-tolerant input for CPU frequency selection. Input is latched upon assertion (LOW) of VTT_PWRGD#/PD Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.
14	USB48/FS_B	I/O	<b>Fixed 48-MHz USB clock output/3.3V-tolerant input for CPU frequency selection.</b> Input is latched upon assertion (LOW) of VTT_PWRGD#/PD Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.
42	IREF	I	<b>A precision resistor is attached to this pin, which is connected to the internal current reference.</b>
1,2,5,6,7,8	PCI[0:5]	O, SE	<b>33-MHz clocks.</b>
11	TEST_SEL/PCIF0	I/O	<b>Free-running 33-MHz clocks/ 3.3V-tolerant input for selecting test mode.</b> Input is latched upon assertion (LOW) of VTT_PWRGD#/PD 1 = All outputs are three-stated for test 0 = All outputs normal operation **This input has an internal pull-down resistor.
12	ITP_EN/PCIF1	I/O, SE	<b>Free-running 33-MHz clock/CPU2 select (sampled on the VTT_PWRGD# assertion).</b> 1 = CPU2_ITP, 0 = SRC6
49	SCLK	I	<b>SMBus-compatible SCLOCK.</b>
50	SDATA	I/O	<b>SMBus-compatible SDATA.</b>
27,28	SATAT, SATAC	O, DIF	<b>Differential serial reference clock.</b> Recommended output for SATA.
19,20,21,22, 25,26,30,31, 32,33,35,36	SRCT/C[0:5]	O, DIF	<b>Differential serial reference clocks.</b>
13	VDD_48	PWR	3.3V power supply for outputs.
45	VDD_CPU	PWR	3.3V power supply for outputs.
3,10	VDD_PCI	PWR	3.3V power supply for outputs.
56	VDD_REF	PWR	3.3V power supply for outputs.
23,29,37	VDD_SRC	PWR	3.3V power supply for outputs.
40	VDD_A	PWR	3.3V power supply for PLL.
15	GND_48	GND	Ground for outputs.
48	GND_CPU	GND	Ground for outputs.
4,9	GND_PCI	GND	Ground for outputs.
53	GND_REF	GND	Ground for outputs.
24,34	GND_SRC	GND	Ground for outputs.
41	GND_A	GND	Ground for PLL.
18	VTT_PWRGD#/PD	I, PU	<b>3.3V LVTTTL input is a level sensitive strobe used to latch the REF0/FSC, REF1/FSA, USB48/FSB, TEST_SEL/PCIF0 and ITP_EN/PCIF1 inputs.</b> After VTT_PWRGD# (active LOW) assertion, this pin becomes a realtime input for asserting power-down (active HIGH).
52	X1	I	<b>14.318-MHz crystal input.</b>
51	X2	O, SE	<b>14.318-MHz crystal output.</b>

## Frequency Select Pins (FS\_A, FS\_B and FS\_C)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS\_A, FS\_B, FS\_C inputs prior to VTT\_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT\_PWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS\_A, FS\_B and FS\_C input values. For all logic levels of FS\_A, FS\_B and FS\_C VTT\_PWRGD# employs a one-shot functionality in that once a valid low on VTT\_PWRGD# has been sampled, all further VTT\_PWRGD#, FS\_A, FS\_B and FS\_C transitions will be ignored, except in test mode.

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initial-

izes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 1. Frequency Select Table (FS\_A, FS\_B, FS\_C)**

FS_C	FS_B	FS_A	CPU	SRC	PCIF/PCI	REF0	DOT96	USB
1	0	1	100 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	0	1	133 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	1	1	166 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	1	0	200 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
0	0	0	266 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
1	0	0	333 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
1	1	0	400 MHz	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz
1	1	1	Reserved	100 MHz	33 MHz	14.318 MHz	96 MHz	48 MHz

**Table 2. Command Code Definition**

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

**Table 3. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge from master

**Table 3. Block Read and Block Write Protocol (continued)**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
....	.....	39:46	Data byte from slave – 8 bits
....	Data Byte (N – 1) – 8 bits	47	Acknowledge from master
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Data Byte N – 8 bits	56	Acknowledge from master
....	Acknowledge from slave	....	Data byte N from slave – 8 bits
....	Stop	....	Acknowledge from master
		....	Stop

**Table 4. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Acknowledge from master
		39	Stop

## Control Registers

### Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	1	CPUT2_ITP/SRCT6 CPUC2_ITP/SRCC6	CPU[T/C]2_ITP/SRC[T/C]6 Output Enable 0 = Disable (Hi-Z), 1 = Enable
6	1	SRC[T/C]5	SRC[T/C]5 Output Enable 0 = Disable (Hi-Z), 1 = Enable
5	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	SATA[T/C]	SATA[T/C] Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	SRC[T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable

**Byte 1: Control Register 1**

Bit	@Pup	Name	Description
7	1	CPUT/C SRCT/C PCIF PCI	Center Spread Enable 0 = $\pm 0.25\%$ Center Spread, 1 = $-0.5\%$ Down Spread
6	1	DOT_96T/C	DOT_96 MHz Output Enable 0 = Disable (Hi-Z), 1 = Enabled
5	1	USB_48	USB_48 MHz Output Enable 0 = Disabled, 1 = Enabled
4	1	REF0	REF0 Output Enable 0 = Disabled, 1 = Enabled
3	1	REF1	REF1 Output Enable 0 = Disabled, 1 = Enabled
2	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enabled
1	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enabled
0	0	CPUT/C SRCT/C PCIF PCI	Spread Spectrum Enable 0 = Spread off, 1 = Spread on

**Byte 2: Control Register 2**

Bit	@Pup	Name	Description
7	1	PCI5	PCI5 Output Enable 0 = Disabled, 1 = Enabled
6	1	PCI4	PCI4 Output Enable 0 = Disabled, 1 = Enabled
5	1	PCI3	PCI3 Output Enable 0 = Disabled, 1 = Enabled
4	1	PCI2	PCI2 Output Enable 0 = Disabled, 1 = Enabled
3	1	PCI1	PCI1 Output Enable 0 = Disabled, 1 = Enabled
2	1	PCI0	PCI0 Output Enable 0 = Disabled, 1 = Enabled
1	1	PCIF1	PCIF1 Output Enable 0 = Disabled, 1 = Enabled
0	1	PCIF0	PCIF0 Output Enable 0 = Disabled, 1 = Enabled

**Byte 3: Control Register 3**

Bit	@Pup	Name	Description
7	0	CPUT2_ITP/SRCT6 CPUC2_ITP/SRCC6	Allow control of SRC[T/C]6 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#
6	0	SRC[T/C]5	Allow control of SRC[T/C]5 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#
5	0	SRC[T/C]4	Allow control of SRC[T/C]4 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#
4	0	SRC[T/C]3	Allow control of SRC[T/C]3 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#
3	0	SATA[T/C]	Allow control of SATA[T/C] with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#

**Byte 3: Control Register 3 (continued)**

Bit	@Pup	Name	Description
2	0	SRC2	Allow control of SRC[T/C]2 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#
1	0	SRC1	Allow control of SRC[T/C]1 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#
0	0	SRC0	Allow control of SRC[T/C]0 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#

**Byte 4: Control Register 4**

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED, Set = 0
6	0	DOT96[T/C]	DOT_PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Hi-Z
5	0	PCIF1	Allow control of PCIF2 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#
4	0	PCIF0	Allow control of PCIF1 with assertion of SW PCI_STP# 0 = Free-running, 1 = Stopped with SW PCI_STP#
3	0	RESERVED	RESERVED, Set = 0
2	1	RESERVED	RESERVED, Set = 1
1	1	RESERVED	RESERVED, Set = 1
0	1	RESERVED	RESERVED, Set = 1

**Byte 5: Control Register 5**

Bit	@Pup	Name	Description
7	0	SRC[T/C][6:0],SATA[T/C]	SRC[T/C], SATA[T/C]Stop Drive Mode 0 = Driven when SW PCI_STP# asserted,1 = Hi-Z when PCI_STP# asserted
6	0	RESERVED	RESERVED, Set = 0
5	0	RESERVED	RESERVED, Set = 0
4	0	RESERVED	RESERVED, Set = 0
3	0	SRC[T/C][6:0],SATA[T/C]	SRC[T/C], SATA[T/C] PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Hi-Z when PD asserted
2	0	CPU[T/C]2	CPU[T/C]2 PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Hi-Z when PD asserted
1	0	CPU[T/C]1	CPU[T/C]1 PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Hi-Z when PD asserted
0	0	CPU[T/C]0	CPU[T/C]0 PWRDWN Drive Mode 0 = Driven when PD asserted,1 = Hi-Z when PD asserted

**Byte 6: Control Register 6**

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED, Set = 0
6	0		Test Clock Mode Entry Control 1 = Hi-Z mode, 0 = Normal operation
5	1	REF1	REF1 Output Drive Strength 0 = Low, 1 = High
4	1	REF0	REF0 Output Drive Strength 0 = Low, 1 = High
3	1	PCIF, SRC, PCI	SW PCI_STP# Function 0=SW PCI_STP assert, 1= SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses.
2	Externally selected	CPUT/C	FS_C. Reflects the value of the FS_C pin sampled on power up 0 = FS_C was low during VTT_PWRGD# assertion
1	Externally selected	CPUT/C	FS_B. Reflects the value of the FS_B pin sampled on power up 0 = FS_B was low during VTT_PWRGD# assertion
0	Externally selected	CPUT/C	FS_A. Reflects the value of the FS_A pin sampled on power up 0 = FS_A was low during VTT_PWRGD# assertion

**Byte 7: Vendor ID**

Bit	@Pup	Name	Description
7	0	Revision Code Bit 3	Revision Code Bit 3
6	0	Revision Code Bit 2	Revision Code Bit 2
5	1	Revision Code Bit 1	Revision Code Bit 1
4	0	Revision Code Bit 0	Revision Code Bit 0
3	1	Vendor ID Bit 3	Vendor ID Bit 3
2	0	Vendor ID Bit 2	Vendor ID Bit 2
1	0	Vendor ID Bit 1	Vendor ID Bit 1
0	0	Vendor ID Bit 0	Vendor ID Bit 0

**Crystal Recommendations**

The CY28412 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the CY28412 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

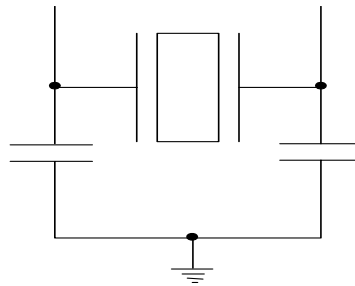
**Crystal Loading**

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

The following diagram shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

**Table 5. Crystal Recommendations**

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	50 ppm	50 ppm	5 ppm


**Figure 1. Crystal Capacitive Clarification**

### Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This mean the total capacitance on each side of the crystal must be 2 times the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

#### Load Capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

#### Total Capacitance (as seen by the crystal)

$$C_{Le} = \frac{1}{\left( \frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

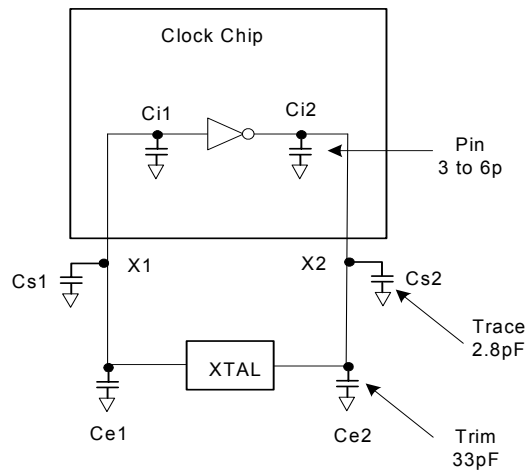
- CL.....Crystal load capacitance
- CLe.....Actual loading seen by crystal using standard value trim capacitors
- Ce.....External trim capacitors
- Cs.....Stray capacitance (terraced)
- Ci.....Internal capacitance (lead frame, bond wires etc.)

### PD (Power-down) Clarification

The VTT\_PWRGD# /PD pin is a dual function pin. During initial power-up, the pin functions as VTT\_PWRGD#. Once VTT\_PWRGD# has been sampled low by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active high input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted high, all clocks are driven to a low value and held prior to turning off the VCOs and the crystal oscillator.

### PD (Power-down) – Assertion

When PD is sampled high by two consecutive rising edges of CPUC, all single-ended outputs will be held low on their next high to low transition and differential clocks must be held high or Hi-Z (depending on the state of the control register drive mode bit) on the next diff clock# high to low transition. When the SMBus PD drive mode bit corresponding to the differential

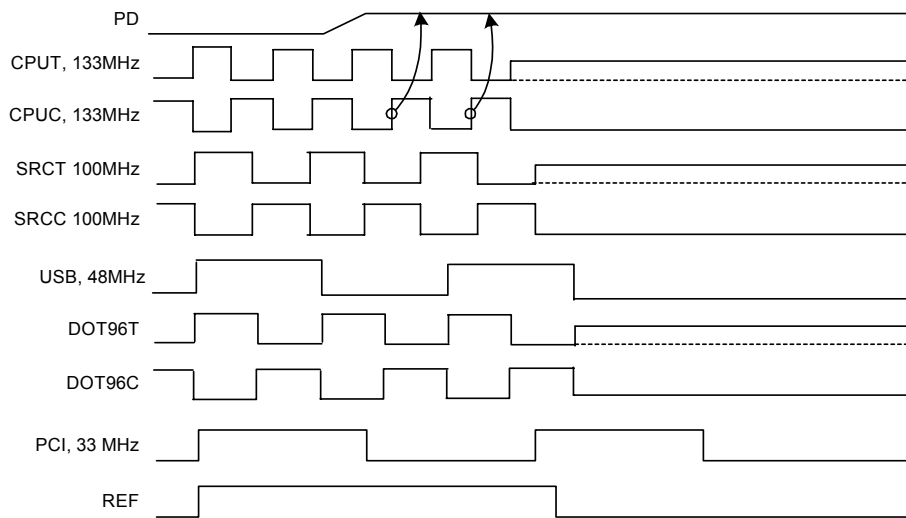

**Figure 2. Crystal Loading Example**



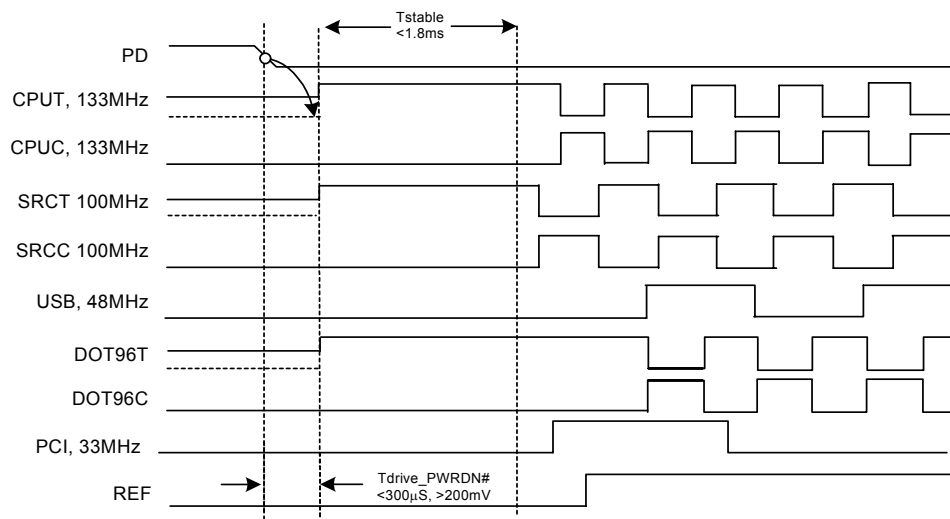
(CPU, SRC, and DOT) clock output of interest is programmed to '0', the clock output must be held with "Diff clock" pin driven high at  $2 \times I_{ref}$ , and "Diff clock#" tristate. If the control register PD drive mode bit corresponding to the output of interest is programmed to "1", then both the "Diff clock" and the "Diff clock#" are Hi-Z. Note the example below shows  $CPU_{T} = 133$  MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100,133,166,200,266,333, and 400 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted high in less than  $10 \mu s$  after asserting  $VTT\_PWRGD\#$ .

### PD Deassertion

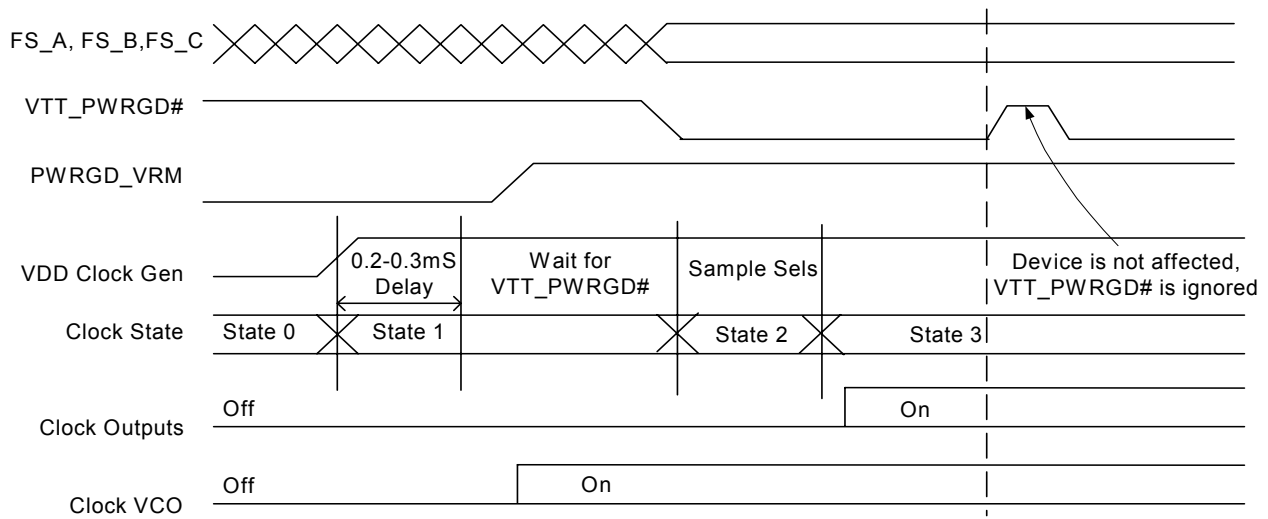
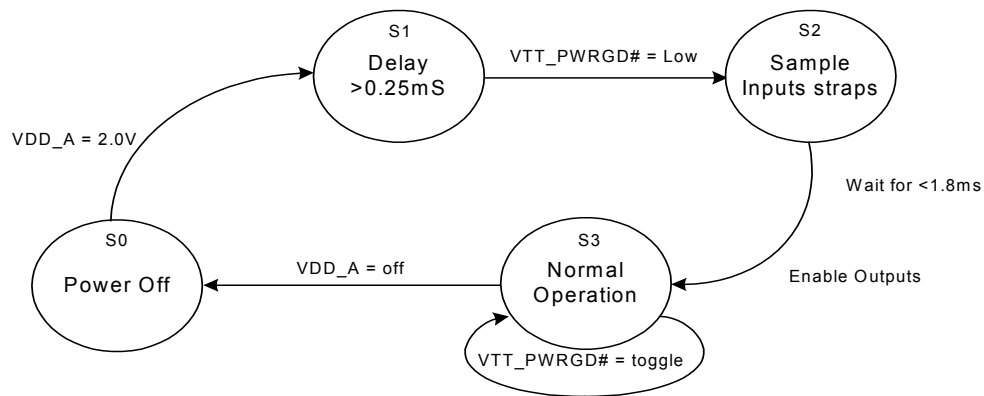
The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a tristate condition resulting from power down must be driven high in less than  $300 \mu s$  of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each other. Below is an example showing the relationship of clocks coming up.



**Figure 3. Power-down Assertion Timing Waveform**



**Figure 4. Power-down Deassertion Timing Waveform**


**Figure 5. VTT\_PWRGD# Timing Diagram**

**Figure 6. Clock Generator Power-up/Run State Diagram**

**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage		-0.5	4.6	V
V <sub>DD_A</sub>	Analog Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	Input Voltage	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.5	VDC
T <sub>S</sub>	Temperature, Storage	Non-functional	-65	150	°C
T <sub>A</sub>	Temperature, Operating Ambient	Functional	0	70	°C
T <sub>J</sub>	Temperature, Junction	Functional	-	150	°C
∅ <sub>JC</sub>	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	-	31.89	°C/W
∅ <sub>JA</sub>	Dissipation, Junction to Ambient	JEDEC (JESD 51)	-	48.29	°C/W
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	-	V
UL-94	Flammability Rating	At 1/8 in.	V-0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD_A</sub> , V <sub>DD_REF</sub> , V <sub>DD_PCI</sub> , V <sub>DD_3V66</sub> , V <sub>DD_48</sub> , V <sub>DD_CPU</sub>	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V <sub>IL2C</sub>	Input Low Voltage	SDATA, SCLK	-	1.0	V
V <sub>IH2C</sub>	Input High Voltage	SDATA, SCLK	2.2	-	V
V <sub>IL_FS</sub>	FS_(A,B,C) Input Low Voltage		V <sub>SS</sub> - 0.3	0.35	V
V <sub>IH_FS</sub>	FS_(A,B,C) Input High Voltage		0.7	V <sub>DD</sub> + 0.5	V
V <sub>IL</sub>	Input Low Voltage		V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>DD</sub> + 0.5	V
I <sub>IL</sub>	Input Low Leakage Current	except internal pull-up resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>	-5		μA
I <sub>IH</sub>	Input High Leakage Current	except internal pull-down resistors, 0 < V <sub>IN</sub> < V <sub>DD</sub>		5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 1 mA	-	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1 mA	2.4	-	V
I <sub>OZ</sub>	High-impedance Output Current		-10	10	μA
C <sub>IN</sub>	Input Pin Capacitance		2	5	pF
C <sub>OUT</sub>	Output Pin Capacitance		3	6	pF
L <sub>IN</sub>	Pin Inductance		-	7	nH
V <sub>XIH</sub>	Xin High Voltage		0.7V <sub>DD</sub>	V <sub>DD</sub>	V
V <sub>XIL</sub>	Xin Low Voltage		0	0.3V <sub>DD</sub>	V
I <sub>DD3.3V</sub>	Dynamic Supply Current	At max load and freq per Figure 8	-	500	mA
I <sub>PD3.3V</sub>	Power-down Supply Current	PD asserted, Outputs driven	-	75	mA
I <sub>PD3.3V</sub>	Power-down Supply Current	PD asserted, Outputs Hi-Z	-	2	mA

**AC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
<b>Crystal</b>					
T <sub>DC</sub>	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T <sub>PERIOD</sub>	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T <sub>R</sub> / T <sub>F</sub>	XIN Rise and Fall Times	Measured between 0.3V <sub>DD</sub> and 0.7V <sub>DD</sub>	–	10.0	ns
T <sub>CCJ</sub>	XIN Cycle to Cycle Jitter	As an average over 1- $\mu$ s duration	–	500	ps
L <sub>ACC</sub>	Long-term Accuracy	Over 150 ms	–	300	ppm
<b>CPU at 0.7V</b>					
T <sub>DC</sub>	CPUT and CPUC Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	100 MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	9.9970	10.003	ns
T <sub>PERIOD</sub>	133 MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	7.4978	7.5023	ns
T <sub>PERIOD</sub>	166 MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	5.9982	6.0018	ns
T <sub>PERIOD</sub>	200 MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	4.9985	5.0015	ns
T <sub>PERIOD</sub>	266 MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	3.7489	3.7511	ns
T <sub>PERIOD</sub>	333 MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	2.9991	3.0009	ns
T <sub>PERIOD</sub>	400 MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	2.4993	2.5008	ns
T <sub>PERIODSS</sub>	100 MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub>	9.9970	10.0533	ns
T <sub>PERIODSS</sub>	133 MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub>	7.4978	7.5400	ns
T <sub>PERIODSS</sub>	166 MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub>	5.9982	6.0320	ns
T <sub>PERIODSS</sub>	200 MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub>	4.9985	5.0266	ns
T <sub>PERIODSS</sub>	266 MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub>	3.7489	3.7700	ns
T <sub>PERIODSS</sub>	333 MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub>	2.9991	3.0160	ns
T <sub>PERIODSS</sub>	400 MHz CPUT and CPUC Period, SSC	Measured at crossing point V <sub>OX</sub>	2.4993	2.5133	ns
T <sub>SKEW</sub>	Any CPUT/C to CPUT/C Clock Skew, SSC	Measured at crossing point V <sub>OX</sub>	–	100	ps
T <sub>CCJ</sub>	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	85	ps
T <sub>CCJ2</sub>	CPU2_ITP Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	125	ps
T <sub>SKEW2</sub>	CPU2_ITP to CPU0 Clock Skew	Measured at crossing point V <sub>OX</sub>	–	150	ps
T <sub>R</sub> / T <sub>F</sub>	CPUT and CPUC Rise and Fall Times	Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V	175	700	ps
T <sub>RFM</sub>	Rise/Fall Matching	Determined as a fraction of 2*(T <sub>R</sub> – T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> )	–	20	%
$\Delta$ T <sub>R</sub>	Rise Time Variation		–	125	ps
$\Delta$ T <sub>F</sub>	Fall Time Variation		–	125	ps
V <sub>HIGH</sub>	Voltage High	Math averages <i>Figure 8</i>	660	850	mv
V <sub>LOW</sub>	Voltage Low	Math averages <i>Figure 8</i>	–150	–	mv
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		250	550	mv
V <sub>OVS</sub>	Maximum Overshoot Voltage		–	V <sub>HIGH</sub> + 0.3	V
V <sub>UDS</sub>	Minimum Undershoot Voltage		–0.3	–	V
V <sub>RB</sub>	Ring Back Voltage	See <i>Figure 8</i> . Measure SE	–	0.2	V
<b>SRC</b>					
T <sub>DC</sub>	SRCT and SRCC Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	100 MHz SRCT and SRCC Period	Measured at crossing point V <sub>OX</sub>	9.9970	10.003	ns
T <sub>PERIODSS</sub>	100 MHz SRCT and SRCC Period, SSC	Measured at crossing point V <sub>OX</sub>	9.9970	10.0533	ns

**AC Electrical Specifications** (continued)

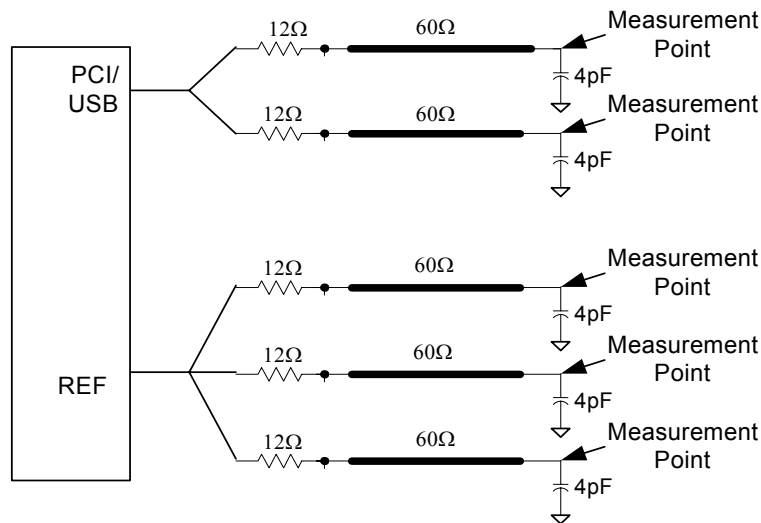
Parameter	Description	Condition	Min.	Max.	Unit
T <sub>CCJ</sub>	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	125	ps
L <sub>ACC</sub>	SRCT/C Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–	300	ppm
T <sub>R</sub> / T <sub>F</sub>	SRCT and SRCC Rise and Fall Times	Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V	175	700	ps
T <sub>RFM</sub>	Rise/Fall Matching	Determined as a fraction of 2*(T <sub>R</sub> – T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> )	–	20	%
ΔT <sub>R</sub>	Rise Time Variation		–	125	ps
ΔT <sub>F</sub>	Fall Time Variation		–	125	ps
V <sub>HIGH</sub>	Voltage High	Math averages <i>Figure 8</i>	660	850	mv
V <sub>LOW</sub>	Voltage Low	Math averages <i>Figure 8</i>	–150	–	mv
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		250	550	mV
V <sub>OVS</sub>	Maximum Overshoot Voltage		–	V <sub>HIGH</sub> + 0.3	V
V <sub>UDS</sub>	Minimum Undershoot Voltage		–0.3	–	V
V <sub>RB</sub>	Ring Back Voltage	See <i>Figure 8</i> . Measure SE	–	0.2	V
T <sub>SKEW</sub>	Any SRCT/C to SRCT/C Clock Skew	Measured at Crossing point V <sub>OX</sub>	–	250	ps
<b>PCI/PCIF</b>					
T <sub>DC</sub>	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.9910	30.0090	ns
T <sub>PERIOD</sub>	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	29.9910	30.1598	ns
T <sub>HIGH</sub>	PCIF and PCI high time	Measurement at 2.4V	12.0	–	ns
T <sub>LOW</sub>	PCIF and PCI low time	Measurement at 0.4V	12.0	–	ns
T <sub>R</sub> / T <sub>F</sub>	PCIF and PCI Edge Rate	Measured between 0.8V and 2.0V	0.5	2.0	V/ns
T <sub>SKEW</sub>	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	500	ps
T <sub>CCJ</sub>	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
<b>DOT</b>					
T <sub>DC</sub>	DOT96T and DOT96C Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	DOT96T and DOT96C Period	Measured at crossing point V <sub>OX</sub>	10.4135	10.4198	ns
T <sub>CCJ</sub>	DOT96T/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	250	ps
L <sub>ACC</sub>	DOT96T/C Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–	300	ppm
T <sub>R</sub> / T <sub>F</sub>	DOT96T and DOT96C Rise and Fall Times	Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V	175	700	ps
T <sub>RFM</sub>	Rise/Fall Matching	Determined as a fraction of 2*(T <sub>R</sub> – T <sub>F</sub> )/(T <sub>R</sub> + T <sub>F</sub> )	–	20	%
ΔT <sub>R</sub>	Rise Time Variation		–	125	ps
ΔT <sub>F</sub>	Fall Time Variation		–	125	ps
V <sub>HIGH</sub>	Voltage High	Math averages <i>Figure 8</i>	660	850	mv
V <sub>LOW</sub>	Voltage Low	Math averages <i>Figure 8</i>	–150	–	mv
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		250	550	mV
V <sub>OVS</sub>	Maximum Overshoot Voltage		–	V <sub>HIGH</sub> + 0.3	V
V <sub>UDS</sub>	Minimum Undershoot Voltage		–0.3	–	V
V <sub>RB</sub>	Ring Back Voltage	See <i>Figure 8</i> . Measure SE	–	0.2	V
<b>USB</b>					
T <sub>DC</sub>	Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	Period	Measurement at 1.5V	20.8271	20.8396	ns
T <sub>HIGH</sub>	USB high time	Measurement at 2.4V	8.094	10.036	ns
T <sub>LOW</sub>	USB low time	Measurement at 0.4V	7.694	9.836	ns

**AC Electrical Specifications** (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_R / T_F$	USB Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
$T_{CCJ}$	USB Cycle to Cycle Jitter	Measurement at 1.5V	-	350	ps
<b>REF</b>					
$T_{DC}$	REF Duty Cycle	Measurement at 1.5V	45	55	%
$T_{PERIOD}$	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
$T_R / T_F$	REF Edge Rate	Measured between 0.8V and 2.0V	0.5	2.0	V/ns
$T_{CCJ}$	REF Cycle to Cycle Jitter	Measurement at 1.5V	-	1000	ps
<b>ENABLE/DISABLE and SETUP</b>					
$T_{STABLE}$	Clock Stabilization from Power-up		-	1.8	ms
$T_{SS}$	Stopclock Set-up Time		10.0	-	ns
$T_{SH}$	Stopclock Hold Time		0	-	ns

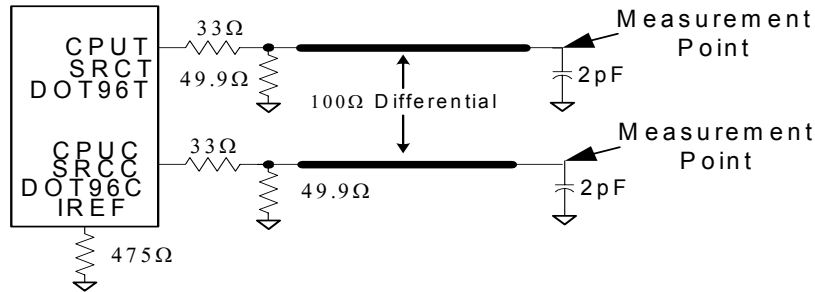
**Test and Measurement Set-up**
**For PCI Single-ended Signals and Reference**

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.

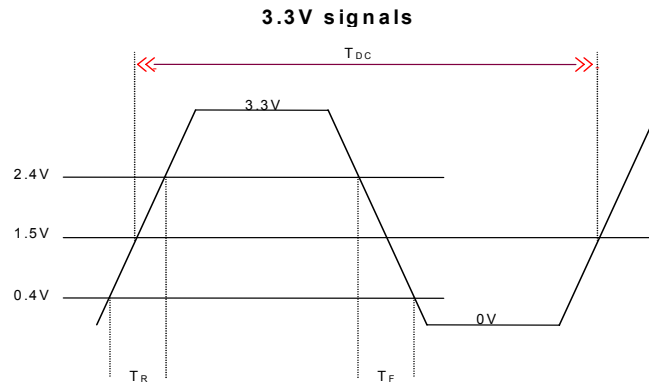

**Figure 7. Single-ended Load Configuration**

**For Differential CPU, SRC and DOT96 Output Signals**

The following diagram shows the test load configuration for the differential CPU and SRC outputs.



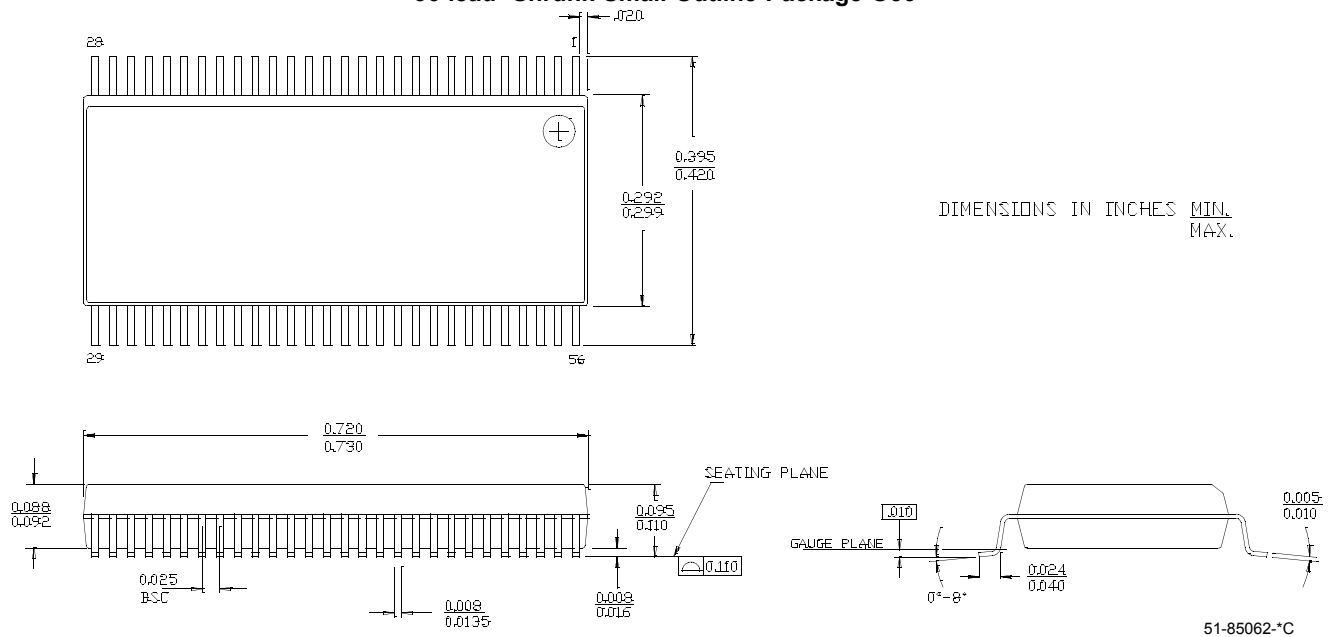
**Figure 8. 0.7V Single-ended Load Configuration**



**Figure 9. Single-ended Output Signals (for AC Parameters Measurement)**

**Ordering Information**

Part Number	Package Type	Product Flow
<b>Standard</b>		
CY28412OC	56-pin SSOP	Commercial, 0° to 70°C
CY28412OCT	56-pin SSOP – Tape and Reel	Commercial, 0° to 70°C
<b>Lead-free</b>		
CY28412OXC	56-pin SSOP	Commercial, 0° to 70°C
CY28412OXCT	56-pin SSOP – Tape and Reel	Commercial, 0° to 70°C

**Package Drawing and Dimensions**
**56-lead Shrunken Small Outline Package O56**


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**Document History Page**

Document Title: CY28412 Clock Generator for Intel® Grantsdale Chipset				
Document Number: 38-07612				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	131327	12/08/03	RGL	New data sheet
*A	208217	See ECN	RGL	Corrected Theta JA/JC values Added T <sub>CCJ2</sub> specs in the AC Electrical Specs table Added T <sub>SKEW2</sub> specs in the AC Electrical Specs table Fixed <i>Figure 7</i> 0.7V Single-ended Load Config Changed max PD supply current from 70 to 75 mA in the AC Electrical Specs table
*B	249075	See ECN	RGL	Fixed the loading diagram Changed the Revision ID Changed the power supply current for Hi-Z to 2 mA
*C	305733	See ECN	RGL	Changed Single-ended outputs from Rise /Fall times to Edge rate Changed Byte 1 Bit 7 from Reserved to Enable Center Spread