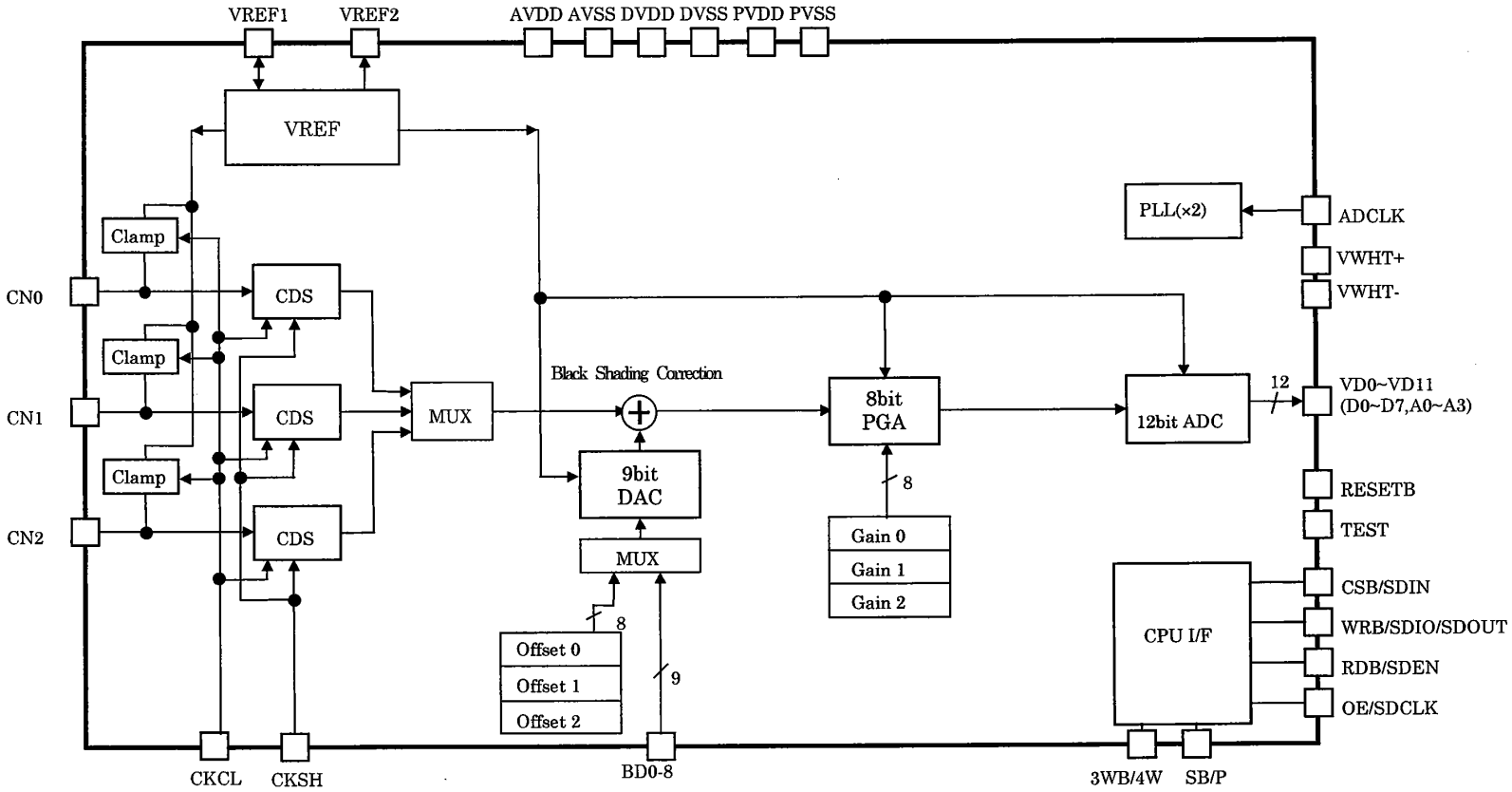
= PRELIMINARY = AK8412

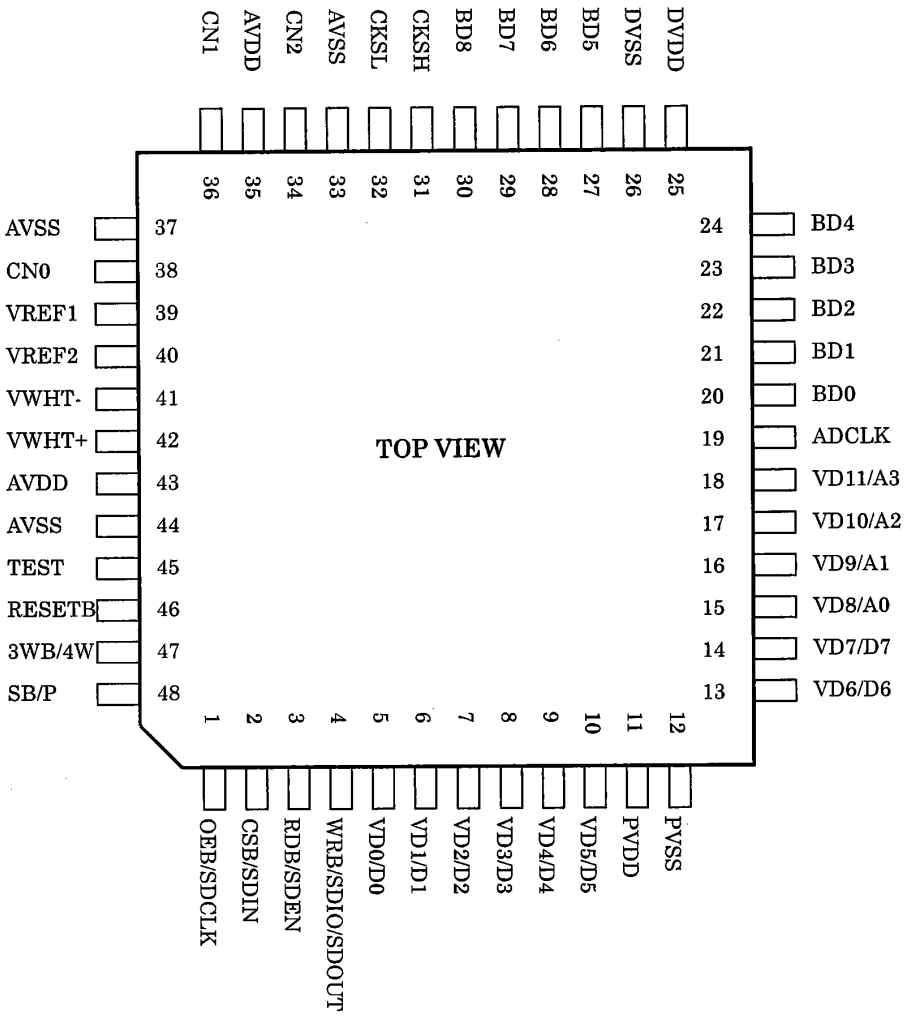
1ch/3ch sensor(CIS/CCD) Analog Pre-Processor

Features

- Processing speed:
  1ch : 10M sample/sec
  2ch : 5M x 2 sample/sec
  3ch : 3.3M x 3 sample/sec
- Input signal level 2Vp-p(typ.)
- Input signal polarity can be selected(CCD/CIS)
- 3ch simultaneously sampling CDS(Correlated Double Sampling) Circuit
- 2 black shading correction modes
  Pixel rate Black shading correction (9bit, ±250mV)
  Offset cancellation (8bit, ±250mV,3 independent offset)
- Gain adjustment
  x 1- x 4 Gain adjustment(8bit,3 independent gain)
- Total performance(CDS ~ Video ADC)
  12bit, No missing codes
  DNL:0.5LSB(typ.)
  INL:3.0LSB(typ.)
  Input reference Noise: 1 LSBrms(typ.) (PGA Gain=1)
- 3.3V/5V Digital I/O compatibility
- Serial/Parallel I/F
- Low power consumption : 300mW(typ.)
- 48 pin LQFP(0.5mm pitch,7 x 7 mold)


VREF1
VREF2
AVDD AVSS DVDD DVSS PVDD PVSS
VREF
PLL(×2)
ADCLK
VWHT+
VWHT-
Clamp
CN0
CDS
Clamp
CN1
CDS
MUX
Black Shading Correction
8bit PGA
12bit ADC
12
VD0~VD11
(D0~D7,A0~A3)
Clamp
CN2
CDS
9bit DAC
8
RESETB
TEST
MUX
Gain 0
Gain 1
Gain 2
CSB/SDIN
WRB/SDIO/SDOUT
RDB/SDEN
OE/SDCLK
CPU I/F
8
Offset 0
Offset 1
Offset 2
9
CKCL
CKSH
BD0-8
3WB/4W
SB/P

Pin Assignment



Pin Description

Pin name	Pin No	I/O	Function
			Shading memory I/F
BD0-8	20-24 27-30	I	Pixel rate Black shading data, with internal pull-up resisters.
			CPU I/F
OEB/ SDCLK	1	I	Output Enable signal/ Serial clock input
RDB/SDEN	3	I	Read signal(Parallel)/Serial enable(Serial)
WRB/SDIO/ SDOUT	4	I/O	Write signal(Parallel)/Serial data input and output(3 Wire serial)/Serial data output(4 Wire serial)
CSB/SDIN	2	I	Chip select signal(Parallel)/Serial data input(Serial 4 Wire)
3WB/4W	47	I	Serial I/F mode select (L: 3 Wire / H: 4 Wire)
SB/P	48	I	Interface mode select (L: Serial / H: Parallel)
			Video output data I/F
VD0-7/D0-7	5-10 13-14	I/O	SB/P=L Video output data SB/P=H OEB=L Video output data SB/P=H OEB=H CPU data bus
VD8-11/A0-3	15-18	I/O	SB/P=L Video output data SB/P=H OEB=L Video output data SB/P=H OEB=H CPU Address Input
ADCLK	19	I	ADC clock(Clock rate is the same with sensor data rate)
			Sampling clock
CKCL	32	I	Clamp clock
CKSH	31	I	Sample / Hold clock
			Other digital pin
RESETB	46	I	Reset. Please reset after power on. After RESETB rise, wait time for PLL pull-in (1ms) is necessary.
TEST	45	I	Test pin. For normal operation, pull down to DVSS externally.

Pin name		I/O	Function
Analog pin			
CN0	38	I	Sensor signal input In case of using 1ch/2ch/3ch sensor, please input sensor signal to this pin.
CN1	36	I	Sensor signal input In case of using 2ch/3ch sensor, please input sensor signal to this pin.
CN2	34	I	Sensor signal input In case of using 3ch sensor, please input sensor signal to this pin.
VREF1	39	I/O	Internal clamp voltage buffer output(CDS or Clamp mode) / External clamp level input(DC connect mode) When this pin is output, external capacitor is necessary
VREF2	40	O	Reference voltage buffer output. External capacitor is necessary.
VWHT+ VWHT-	41 42	O	White side reference voltage buffer output for video ADC External capacitor is necessary for each pin.
Power supply			
DVDD	25		Digital supply (5V±5%)
DVSS	26		Digital ground
PVDD	11		Digital Output pad supply (VD0 - VD11, SDIO) (3.15-5.25V)
PVSS	12		Digital Output pad ground (VD0 - VD11, SDIO)
AVDD	35 43		Analog supply (5V±5%)
AVSS	33 37 44		Analog ground

Sensor Interface Mode

AK8412 supports three modes of sensor interface. Please choose most appropriate one according to the sensor.

(1) CDS mode(Correlated Double Sampling)

This mode is for interfacing with CCD, which outputs the reference level at pixel by pixel. AK8412 includes two sets of sample and hold circuit to each channel, one is for sampling the reference level and another is for sampling video signal. As difference between these two levels is treated as actual signal, affect by temperature variation etc. is eliminated. For keeping the input signal dynamic range, a weak clamp circuit, which recovers the droop at pixel by pixel. In this mode please choose 0.1micro farad capacitor.

(2) Clamp mode

This mode is for interfacing with CCD with sample hold and so on, which doesn't output reference level at pixel by pixel. In this mode a strong clamp circuit and only a sample hold circuit for sampling video signal is utilized for each channel. Clamp timing can be defined by the supplied CKCL. In this mode please choose around 1 micro farad capacitor. Please take care of droop voltage and necessary clamp time in this mode.

(3)DC connect mode

This mode is for interfacing with CIS and so on. In this mode only a sample hold circuit for sampling video signal is utilized for each channel. So connect sensor output to signal input pin directly, and pull CKCL pin down to DVSS. And in this mode VREF1 pin is input. Please supply an appropriate reference voltage to this pin.

■ CDS overview

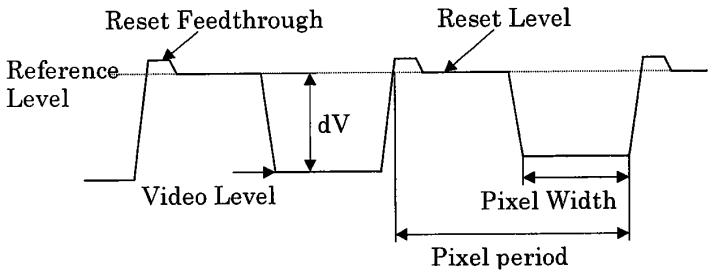


Fig.1 CCD Video Sensor Output Signal

CCD Video Sensor Output Signal is shown in Fig.1.The dV is the difference Reset Level-Video Level. The dV defines Sensor input. This is the circuit called CDS(Correlated Double Sampler). kT/C noise of CCD Video Sensor is eliminated. White noise of CCD Video Sensor is reduced.

CDS circuit diagram and Sample Hold Timing are shown below.

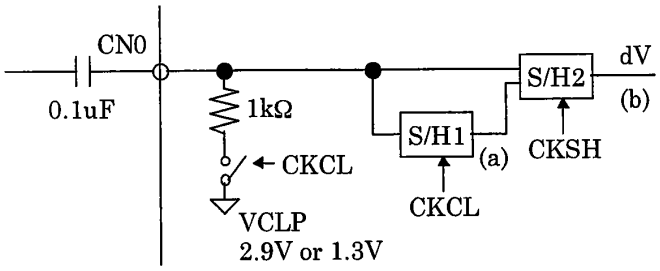


Fig.2 CDS Circuit

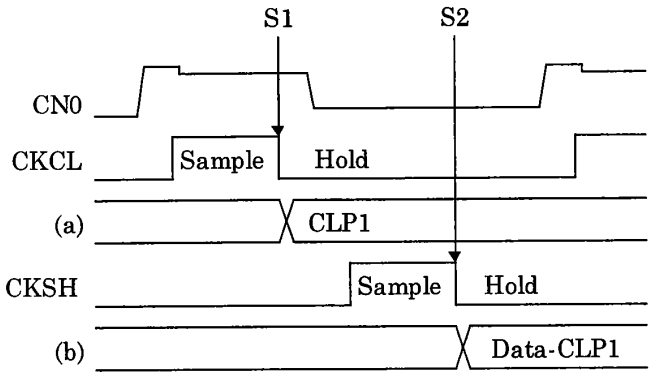


Fig.3 Sample Hold Timing

CDS circuit operation in Fig.2,3 is as follows.
During CKCL is High ,The Reset Level is sampled. At S1(CKCL falling edge),circuit S/H1 hold the Reset Level from CCD Video Sensor.
During CKSH is High ,The Video Level is sampled. At S2(CKSH falling edge)),circuit S/H2 hold the Video Level from CCD Video Sensor.
At this time ,the difference Reset Level-Video Level calculated and it defines Sensor input.

Registers

Addr.	R/W	init (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
0	R/W	10	Clamp Mode		Black correction range		Signal Polarity	PGA Enable	Black Correction Mode	Black correc-tion range ratio detect Enable
1	R/W	XX	X	X	Processing channel order			Channel Mode select Channel select		
2	R/W	80	offset0(CN0)							
3	R/W	80	offset1(CN1)							
4	R/W	80	offset2(CN2)							
5	R/W	00	PGA gain0(CN0)							
6	R/W	00	PGA gain1(CN1)							
7	R/W	00	PGA gain2(CN2)							
8	R/W	XX	Black correction range ratio							

Register description

R0 register

D7,D6: Clamp Mode

Select the Clamp mode.

D7	D6	Processing mode	VREF1
0	0	CDS	Internal
0	1	Clamp	Internal
1	0	DC connect (after reset)	External

Typical usage of CDS mode is for CCD, Clamp mode is for CCD with sample and hold circuit, and DC connect is for CIS.

D5,D4: Black correction range

Select the black shading correction range.

D5	D4	Correction range
0	0	Clamp level ±100mV
0	1	Clamp level ±150mV (after reset)
1	0	Clamp level ±200mV
1	1	Clamp level ±250mV

D3: Signal Polarity

Select the Sensor signal polarity.

0: Negative : Normally CCD (after reset)

1: Positive : Normally CIS

D2:PGA Enable

Enable PGA

0: Enable (after reset)

1: Disable (= unity gain)

D1: Black shading correction Mode

Select the Black shading Mode.

0: Offset cancel Mode (after reset)

1: Pixel to Pixel correction Mode

D0: Black correction range ratio detect Enable

Enable the Black correction range ratio detect mode.

0: Disable (after reset)

1: Enable

This mode is only for users who utilize pixel to pixel type black correction.

R1 register

D5,D4,D3: Processing channel order

Set the sampling order.

3ch mode

D5	D4	D3	Processing order
0	0	0	CN0→CN1→CN2
0	0	1	CN2→CN0→CN1
0	1	X	CN1→CN2→CN0
1	0	0	CN0→CN2→CN1
1	0	1	CN1→CN0→CN2
1	1	X	CN2→CN1→CN0

2ch mode

D5	D4	D3	Processing order
X	X	0	CN0→CN1
X	X	1	CN1→CN0

(Note) This register is not initialized by reset.

D2,D1,D0: Channel Mode and Enable

Channel Mode select (Normal operation)

D2	D1	D0	Mode
1	1	1	3 Channel
0	1	1	2 Channel
0	0	1	1 Channel

(Note1) Please set only above table value. Another value cause VD0-11 unexpected result.

(Note2) This register is not initialized by reset.

Channel Enable (Black correction range ratio detect mode :R0D0=1)

D2	D1	D0	channel
0	0	1	CN0
0	1	0	CN1
1	0	0	CN2

(Note) This register is not initialized by reset.

At the black correction range ratio detect mode, you can enable only one channel by setting 1 to corresponded bit in this register.

R2,R3,R4 register : offset data

It is possible to set the offset data for each channel. (after reset : 80h)

D7-D0	offset
11111111	-250mV
11111110	:
:	:
10000000	0 mV
:	:
00000000	250mV

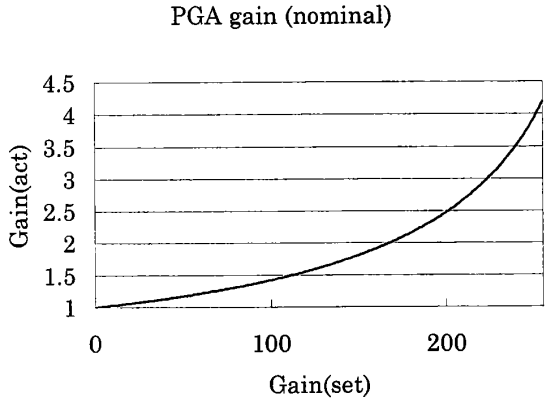
Black correction range = ±250mV

R5,R6,R7 register : PGA gain data

It is possible to set the gain data for each channel. (after reset : 00h)

Equation between actual gain and set data is as follows.

Gain(act) = 335/(335-Gain(set))



R8 register : Black correction range ratio

Black correction range ratio, that is the ratio of black correction circuit range and video ADC range. This data can be utilized for calculating pixel to pixel black shading data, which is automatically set after the black correction range ratio detect mode is executed. This data is no meaning for users who don't use pixel to pixel black shading correction mode.

Black correction mode

AK8412 supports two types of correction mode. One is offset cancel mode, which adjusts only DC offset. Another is pixel to pixel correction mode.

(1) Offset cancel mode

The offset voltage per channel can be adjusted by R2/R3/R4 registers. Please adjust it to appropriate level by monitoring ADC output. Upper 8 bits of Black Correction Circuit are used. Code 80H is nothing dealt with. Code 00H is addition of maximum voltage to input signal. Code FFH is subtraction of maximum voltage from input signal.

(2) Pixel to pixel type correction

In this mode, pixel to pixel correction data is necessary. This section describes an example of detecting it. Please follow to the procedure described below.

[1] Detect of temporary ratio of ADC full scale and Black correction circuit.

(A) Set PGA gain0 to unity gain(R5=0).

(B) Set to the Black correction range ratio detect mode enable(R0/D0=1).
This mode is for calibrating the ratio ADC full scale and Black correction circuit full scale, which will be used calculating pixel to pixel black shading data.

(C) CN0 input is fixed to internal reference level, and 1/2*(ADC range) is added to internal ADC input automatically.

(D) This mode is executed automatically by above operations. When this mode will be completed, R0/D0 bit will be reset(0). So after you confirms R0/D0 status, read R8 register and store this data in your system.

[2] Rough black correction data detect

(A) Set PGA gain0, PGA gain1, and PGA gain2 to unity gain(R5/R6/R7=0).

(B) Set Black correction mode bit to Offset cancel mode(R0/D1=0).

(C) Set Black shading data offset0,1,2(R2/3/4) to 00H.

(D) Scan the document with LED off or scan black reference with LED on, a series of data of 1 line should be data(n)(n=1~n0, n0:pixel count of a sensor).

(E) Get rough black correction data from following equation.

$$\text{Rough Black Correction Data}(n) = 511/(R8\times 16) \times \text{data}(n)$$

[3] PGA Gain detect

(A) Set Black correction mode bit to pixel to pixel mode(R0/D1=1).

(B) Scan white reference document, with supplying Rough black correction data(n) pixel by pixel. By the ADC output, please choose appropriate gains, PGA gain0, PGA gain1, PGA gain2. In two channel mode, PGA gain0 and PGA gain1. In one channel mode, PGA gain0 only.

[4] Detect of ratio of ADC full scale and Black correction circuit by each channel.

(A) Set PGA gain0 to the detected one(R5).

(B) Set to the Black correction range ratio detect mode enable(R0/D0=1).
This mode is for calibrating the ratio ADC full scale and Black correction circuit full scale, which will be used calculating pixel to pixel black shading data.

(C) CN0 inputs are fixed to internal reference level, and 1/2× (ADC range) is added to internal ADC input automatically.

(D) This mode is executed automatically by above operations. When this mode will be completed, R0/D0 bit will be reset(0). So after you confirms R0/D0 status, read R8 register and store this data in your system.

(E) Depending on channel number is used, please repeat (A)~(D) procedure per channel. Get three ratio at maximum depending channel number.

[5] Precise black correction data detect

(A) Set PGA gain0, PGA gain1, and PGA gain2 to the detected ones(R5/R6/R7).

(B) Set Black correction mode bit to Offset cancel mode(R0/D1=0).

(C) Set Black shading data offset0,1,2(R2/3/4) to 00H.

(D) Scan the document with LED off or scan black reference with LED on, a series of data of 1 line should be data(n)(n=1~n0, n0:pixel count of a sensor) per channel.

(E) Get Precise black correction data from following equation.

$$\text{Precise Black Correction Data}(n) = 511/(R8\times 16) \times \text{data}(n)$$

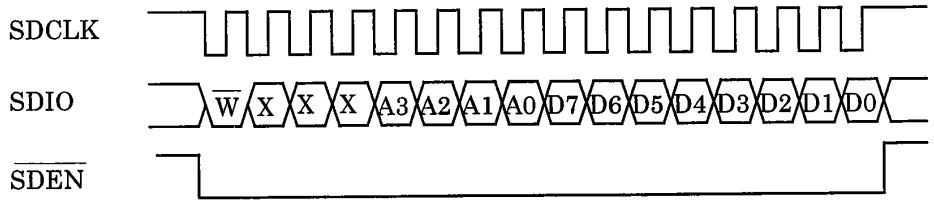
(F) In three channel mode, you get three sets of data. In two channels two sets of data. In one channel mode, one set of data. On actual scanning of document, set Black correction mode bit to pixel to pixel mode(R0/D1=1). Scan the document with feeding the calculated black shading data through BD0~BD8 at the defined timing in AC timing specifications.

Note: This way to get pixel to pixel correction data is only an example, does not assure the performance.

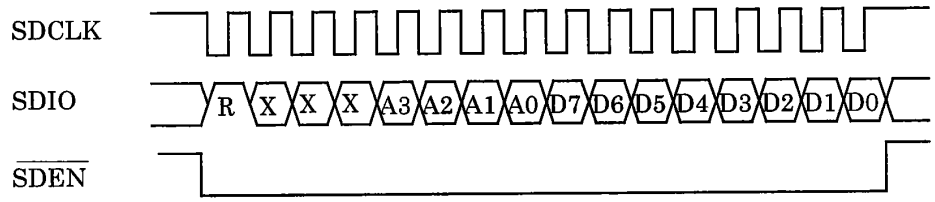
Serial I/F Timing

1. 3 Wire serial I/F

(1)Write to AK8412

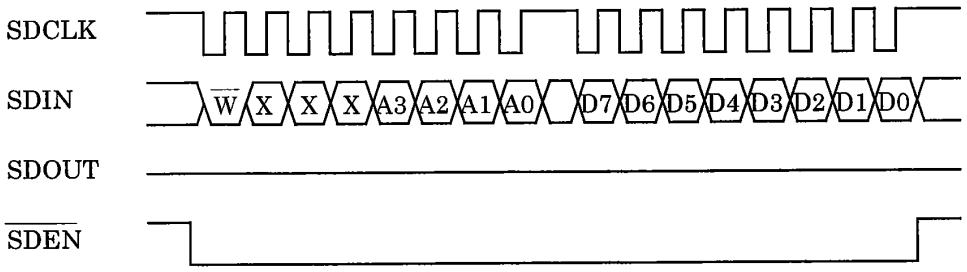


(2)Read from AK8412

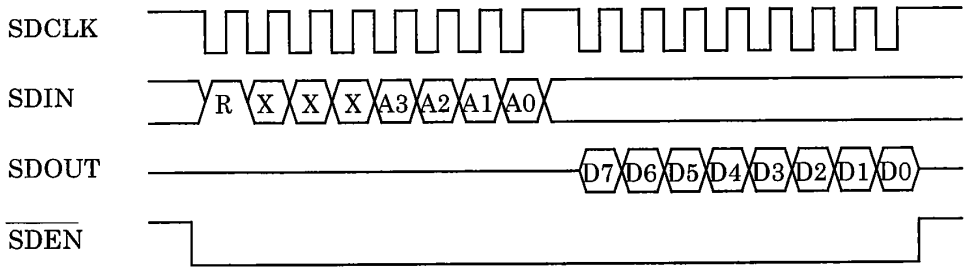


2. 4 Wire serial I/F

(1)Write to AK8412



(2)Read from AK8412



Absolute maximum rating

All voltage defined to their corresponding ground,AVSS,DVSS,PVSS=0V

Parameters	Sym.	Min.	max.	Unit	Remarks
Supply voltage					Must be VA≥VD
Digital	VD	-0.3	6.5	V	at all time.
	VP	-0.3	6.5	V	
Analog	VA	-0.3	6.5	V	
Digital applied voltage	VTD	-0.3	VD+0.3	V	
	VTP	-0.3	VP+0.3	V	
Analog applied voltage	VTA	-0.3	VA+0.3	V	
Operating temp.	Ta	0	70	°C	
Storage temp.	Tstg	-55	125	°C	
Soldering temp. and time	Tsol	260°C,10sec			

Recommended operating condition

Parameters	Sym.	min.	typ.	max.	Unit	Remarks
Supply voltage						Must be VA≥VD
Digital	VD	4.75		5.25	V	at all time.
	VP	3.15		5.25	V	
Analog	VA	4.75		5.25	V	
Operating temp.	Ta	0		70	°C	

Electronic specification

■ DC specification

(Unless otherwise specified,VD,VA=5V±5%,VP=3.15~5.25V,Ta=0~70°C)

Parameters	Sym.	Pins	min.	typ.	Max.	Unit	Conditions
Supply current	ID	DVDD,PVDD		5	10	mA	CDS mode
Digital	IA	AVDD		55	75	mA	No load
Analog							
	ID	DVDD,PVDD		5	10	mA	DC connect
	IA	AVDD		50	70	mA	Clamp mode
							No load
High level input voltage	VIH	Digital input pins	2.4			V	
Low level input voltage	VIL	Digital input pins			0.8	V	
High level output voltage	VOH	Digital output pins	PVDD -0.5			V	IOH= -0.5mA
Low level output voltage	VOL	Digital output pins			0.5	V	IOL=2mA
Leakage current	IL	Digital input pins	-10		10	μA	VI=DVDD VI=DVSS
	ILPU	BD 0-8	-100		10	μA	

■ Analog specification

(Unless otherwise specified, VD,VA=5V±5%,VP=3.15~5.25V, Ta=0~70°C)

Parameters	min.	typ.	Max.	Unit	Remark
Analog input					
Maximum signal input level	1.8	2.0	2.2	Vp-p	
Sampling rate	1.5 0.75 0.5		10 5 3.3	Mpix/s	1ch mode 2ch mode 3ch mode
Input capacitance			20	pF	CN0-CN2
Input resistance	1			MΩ	CN0-CN2(When internal clamp switch is OFF) AVSS+0.5V < VIN < AVDD-0.5V
Black shading correction circuit					
Correction range		±100 ~ ±250		mV	Programmable by ±50mV units
Minimum correction range	VREF1±50	VREF1±100		mV	range =±100mV
	VREF1±100	VREF1±150		mV	range =±150mV
	VREF1±150	VREF1±200		mV	range =±200mV
	VREF1±200	VREF1±250		mV	range =±250mV
Resolution		9		bit	(Note1)
Integral Nonlinearity (by 10bit ADC)		±1	±2	LSB	range=±100mV
		±2	±4	LSB	range =±150mV
		±3	±6	LSB	range =±200mV
ADCLK≤7.5MHz		±4	±8	LSB	range =±250mV
		±5	±10	LSB	range =±100mV
		±15	±30	LSB	range =±150mV
		±25	±50	LSB	range =±200mV
ADCLK=7.5~10MHz		±35	±70	LSB	range =±250mV
Voltage reference					
VREF1 output voltage	1.15	1.3	1.45	V	Signal polarity: Positive
	2.6	2.9	3.2	V	Signal polarity: Negative
VREF1 input voltage	0		1.6	V	Signal polarity: Positive
	2		3.6	V	Signal polarity: Negative
VREF2 voltage	1.95	2.2	2.45	V	
VWHT+ voltage	2.45	2.7	2.95	V	
VWHT- voltage	1.45	1.7	1.95	V	
Clamp circuit					
Clamp Switch ON resistance			100	Ω	Clamp mode Analog input=2.0V
			1.5	kΩ	CDS mode
Sample and hold circuit					
Droop voltage			10	mV	Clamp mode C=2uF MCLK=10MHz VCLP-2V 8000pixels
Residual offset voltage after clamp recovery			20	mV	Clamp mode C=2uF MCLK=10MHz VCLP-2V 8000pixels Recovery clamp=100uS (Note2)

(Unless otherwise specified, VD,VA=5V±5%,VP=3.15~5.25V, Ta=0~70°C)

Parameters	min.	typ.	Max.	Unit	Remark
PGA circuit					
Resolution		8		bit	(Note3)
Minimum Gain range	0.95	1.0	1.05		
Maximum Gain range	4.0	4.2	4.4		
Video ADC					
Resolution		12		bit	No code missing
Maximum signal input level	1.8	2.0	2.2	Vp-p	Maximum code appears in this range.
Minimum signal input level	VREF1-50		VREF1+50	mV	Minimum code appears in this range.
Integral Nonlinearity (INL)		±3.0	±6.0	LSB	
Differential Nonlinearity (DNL)		±0.5	±1.0	LSB	
Noise and Crosstalk					
Total Output Noise PGA min		1		LSBrms	CDS mode
Total Output Noise PGA max		1.5		LSBrms	CDS mode
Channel-Channel Crosstalk (Dynamic)		0.5		LSB	ADCLK=10MHz Sinusoidal Input Signal 200kHz,1.4Vpp
Channel-Channel Crosstalk (Static)			8	LSB	(Note4)
PLL					
pull in time			1	ms	

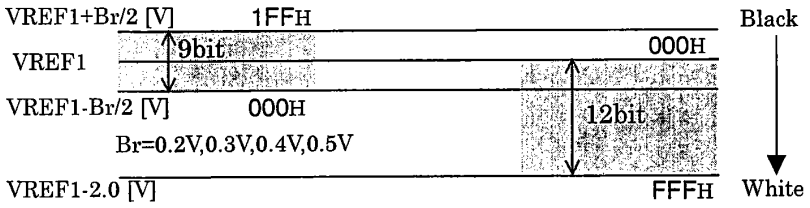
(Note1) The monotonicity of code at a multiple of 8 is degraded. Please don't use the codes, which are multiple of 8. The monotonicity of code except a multiple of 8 is guaranteed.

(Note2) Not production tested. Parameters guaranteed by design and characterization.

(Note3) The monotonicity of code 127 and 128 is degraded. Please don't use these two codes.

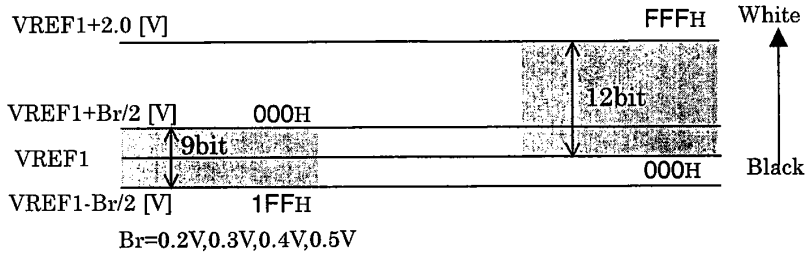
(Note4) Input of measured channel is 0Vpp or 2Vpp. Channel-Cannel Crosstalk (Static) is the difference between ADC code with the other two channel inputs at 0Vpp and ADC codes with the other channel inputs at 2Vpp.

■ Level Diagram



Black correction range ADC range

polarity = NEG



Black correction range ADC range

polarity = POS

■ Digital AC timing

(Unless otherwise specified, VD,VA=5V±5%, VP=3.15~5.25V, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	max.	unit	Condition
1	ADCLK cycle time(T)	ADCLK	100			ns	
2	ADCLK low level width	ADCLK	30			ns	
3	ADCLK high level width	ADCLK	30			ns	
4	CKCL pulse width	CKCL	25			ns	
5	CKSH cycle time	CKCL CKSH	300			ns	3ch mode
			200			ns	2ch mode
			100			ns	1ch mode
6	CKSH pulse width	CKSH	35			ns	
7	CKSH↑delay time (to CKCL↓)	CKSH	0			ns	
8	CKSH set up time (to ADCLK↑)	CKSH	25		T-10	ns	
9	CKSH hold time (to ADCLK↑)	CKSH	10			ns	
10	CN0-2 set up time (to CKCL↓)	CN0-2	25			ns	
11	CN0-2 hold time (to CKCL↓)	CN0-2	10			ns	
12	CN0-2 set up time (to ADCLK↑)	CN0-2	25			ns	
13	CN0-2 hold time (to ADCLK↑)	CN0-2	10			ns	
14	CKCL delay time (to CKSH↓)	CKCL	0			ns	
15	VD0-VD11 delay time (to ADCLK↑)	VD0-VD11			35	ns	C=20pF
16	BD0-8 set up time (to ADCLK↑)	BD0-8	20		T -20	ns	
17	BD0-8 hold time (to ADCLK↑)	BD0-8	20		T -20	ns	

(Unless otherwise specified, VD,VA=5V±5%, VP=3.15~5.25V, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	Max.	unit	Condition
18	/CS set up time (to /WR↓,/RD↓)	/CS	20			ns	
19	/CS hold time (to /WR↑,/RD↑)	/CS	0			ns	
20	A0-A3 set up time (to /WR↓,/RD↓)	A0-A3	20			ns	
21	A0-A3 hold time (to /WR↑,/RD↑)	A0-A3	0			ns	
22	/WR pulse width	/WR	20			ns	
23	D0-D7 set up time (to /WR↑)	D0-D7	20			ns	
24	D0-D7 hold time (to /WR↑)	D0-D7	0			ns	
25	/RD pulse width	/RD	20			ns	
26	D0-D7 delay time (to /RD↓)	D0-D7			30	ns	C=20pF
27	D0-D7 hold time (to /RD↑)	D0-D7	0			ns	
28	VD0-VD11→Hi-Z delay time(to /OE↑)	VD0-VD11			25	ns	
29	VD0-VD11 Hi-Z→output time(to /OE↓)	VD0-VD11			25	ns	
30	/OE set up time (to /WR↓, /RD↓)	/OE	20			ns	
31	/OE hold time (to /WR↑,/RD↑)	/OE	0			ns	

(Unless otherwise specified, VD,VA=5V±5%, VP=3.15~5.25V, Ta=0~70°C)

No.	Parameters	Pins	min.	typ.	Max.	unit	Condition
32	SDCLK cycle time	SDCLK	80			ns	
33	SDCLK low level width	SDCLK	40			ns	
34	SDCLK high level width	SDCLK	40			ns	
35	serial access cycle time	SDCLK	1360			ns	
36	SDIO,SDIN set up time (to SDCLK↑)	SDIO SDIN	20			ns	
37	SDIO,SDIN hold time (to SDCLK↑)	SDIO SDIN	20			ns	
38	/SDEN set up time (to SDCLK↓)	/SDEN	40			ns	
39	/SDEN hold time (to SDCLK↑)	/SDEN	40			ns	
40	/SDEN high level width	/SDEN	40			ns	
41	SDIO,SDOUT delay time (to SDCLK↓)	SDIO SDOUT			30	ns	C=20pF
42	SDIO,SDOUT hold time (to /SDEN↑)	SDIO SDOUT	0			ns	C=20pF
43	/RESET	/RESET	20			ns	

(1)CDS mode timing

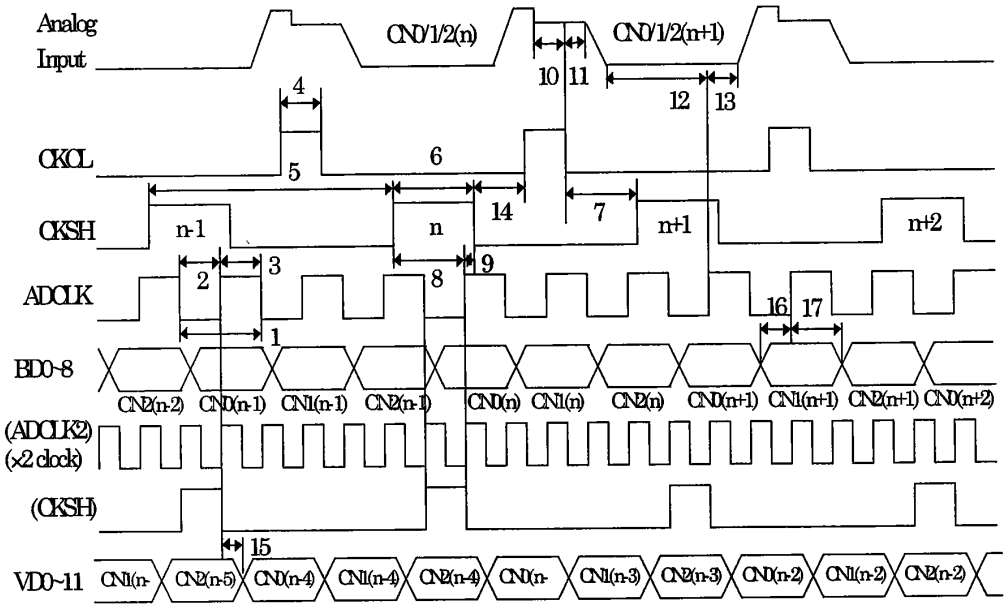


Fig.4 3Channel Mode (CDS)

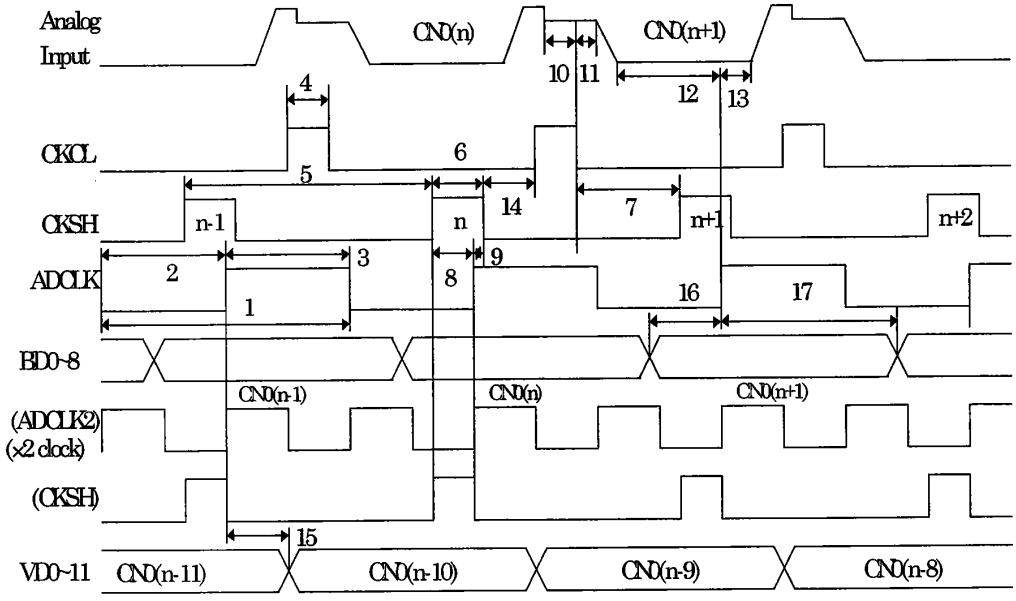


Fig.5 1Channel Mode (CDS)

(1)CDS mode timing

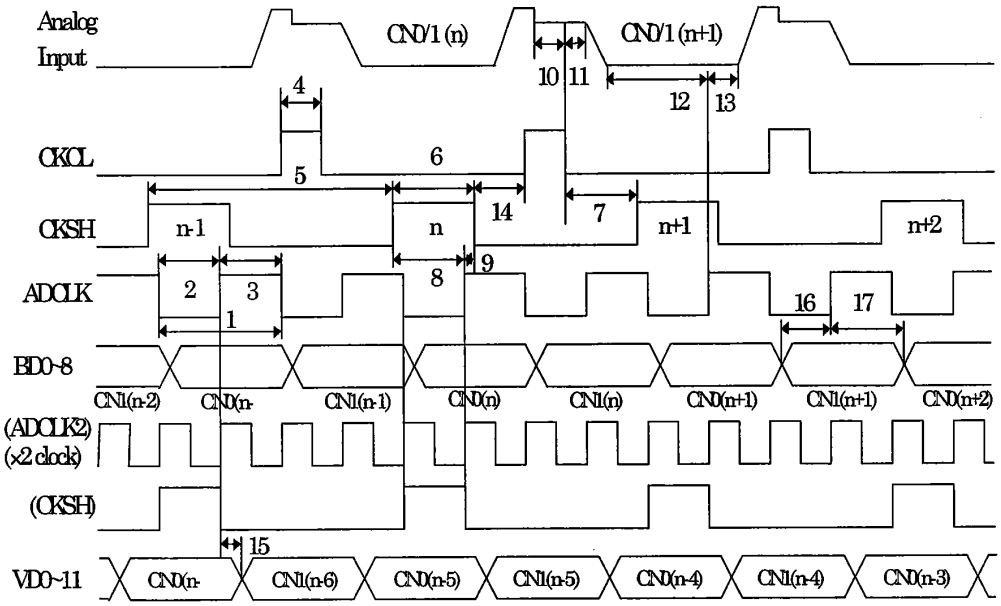


Fig.6 2Channel Mode (CDS)

(2)DC connect mode timing

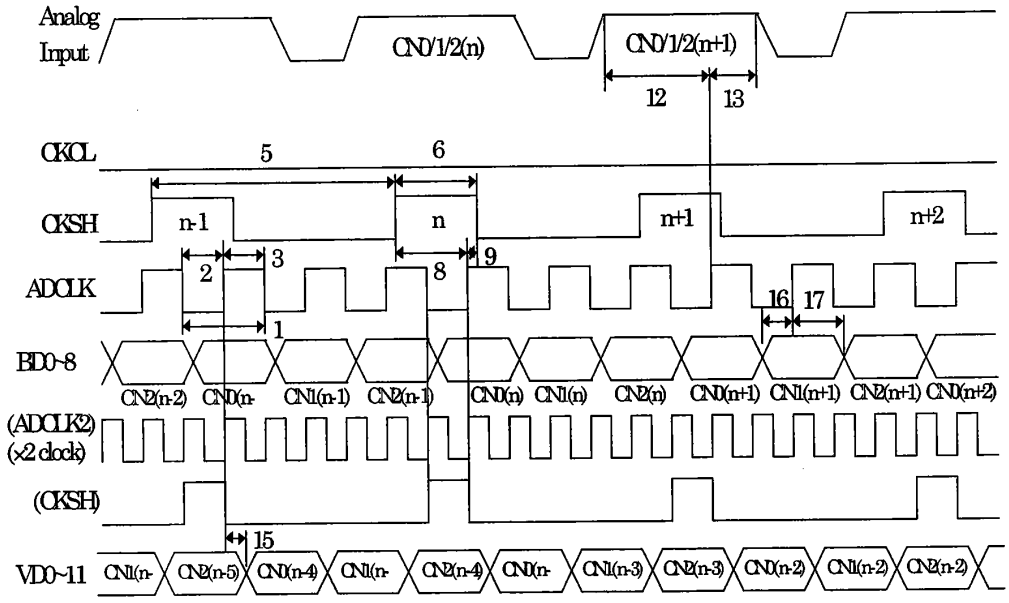


Fig.7 3Channel Mode (DC connect)

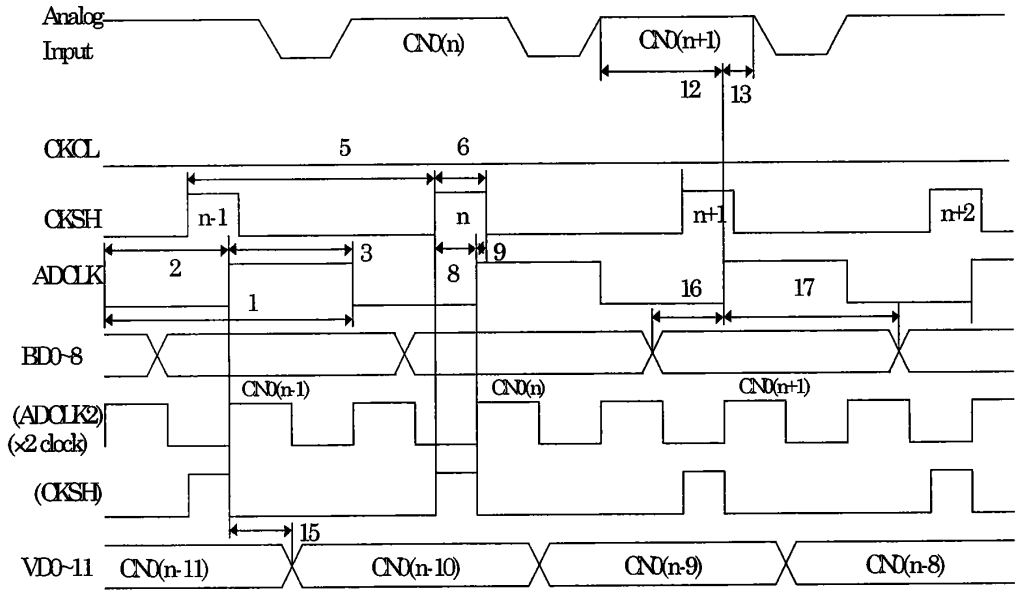


Fig. 8 1Channel Mode (DC connect)

(2)DC connect mode timing

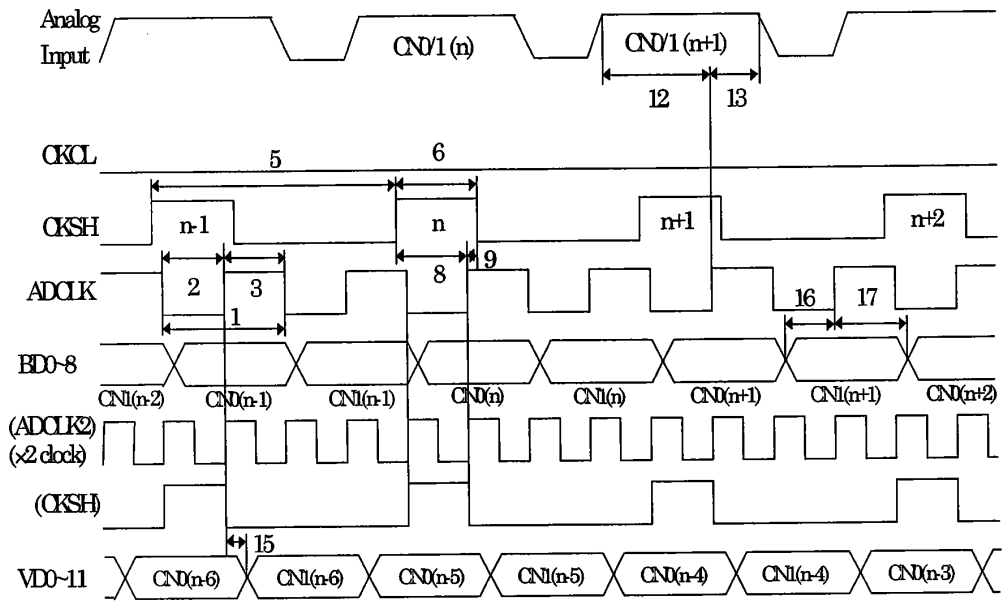


Fig.9 2Channel Mode (DC connect)

(3)Line Clamp mode for CIS timing

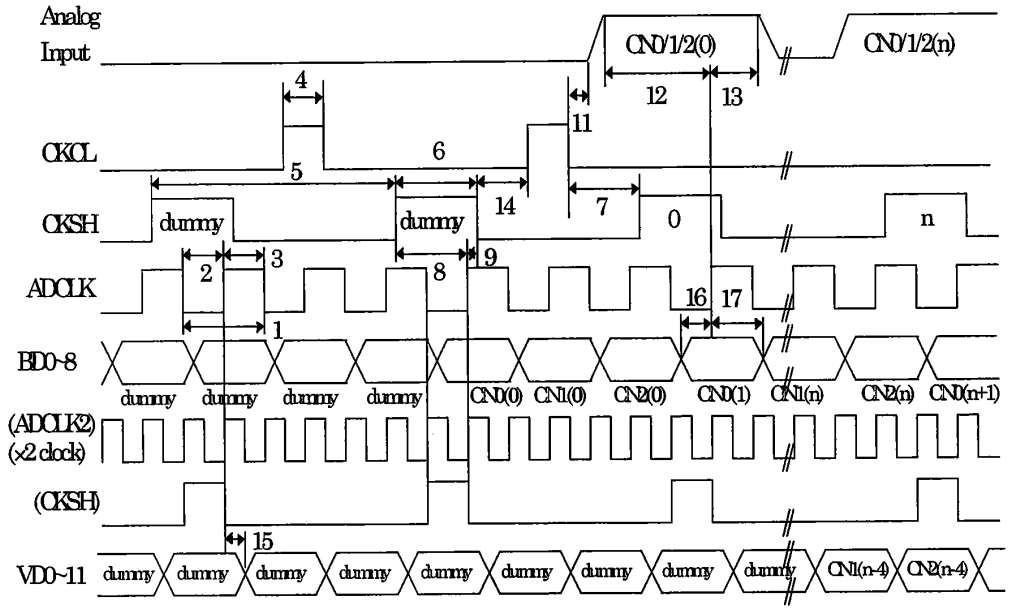


Fig.10 3Channel Mode (Line Clamp for CIS)

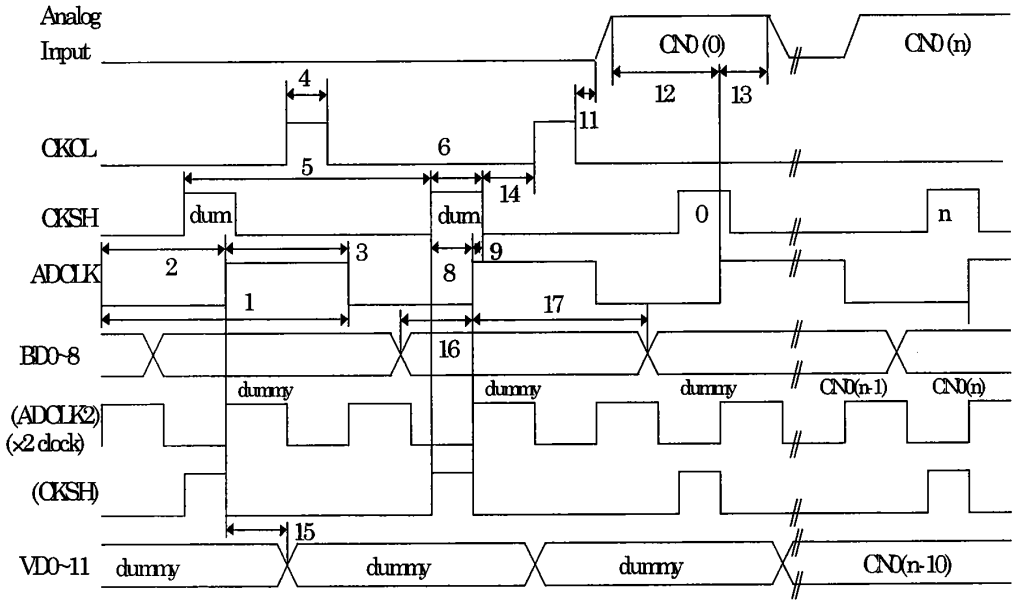


Fig.11 1Channel Mode (Line Clamp for CIS)

(3)Line Clamp mode for CIS timinig

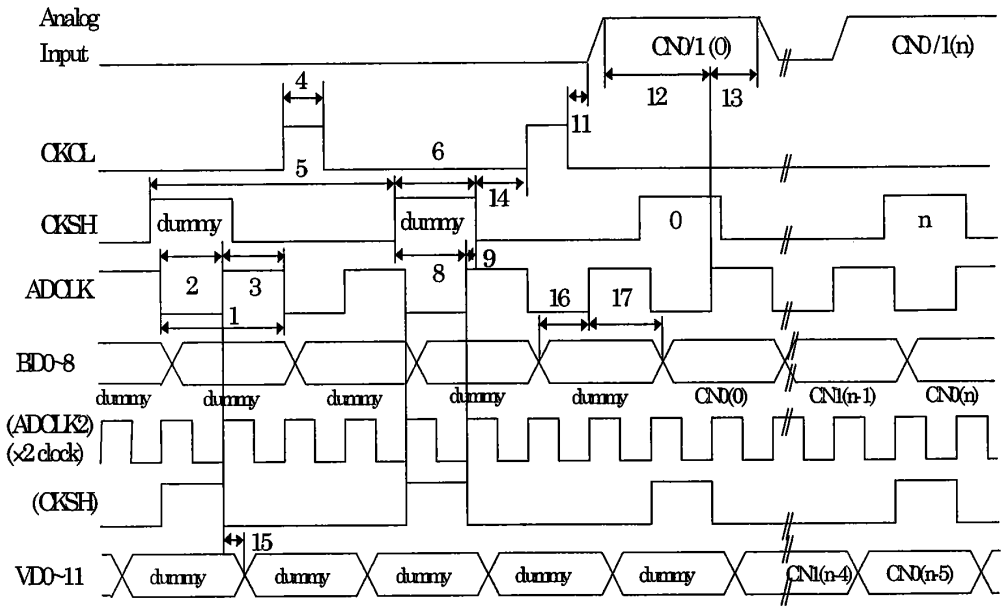


Fig.12 2Channel Mode (Line Clamp for CIS)

(4)Line Clamp mode for CCD timing

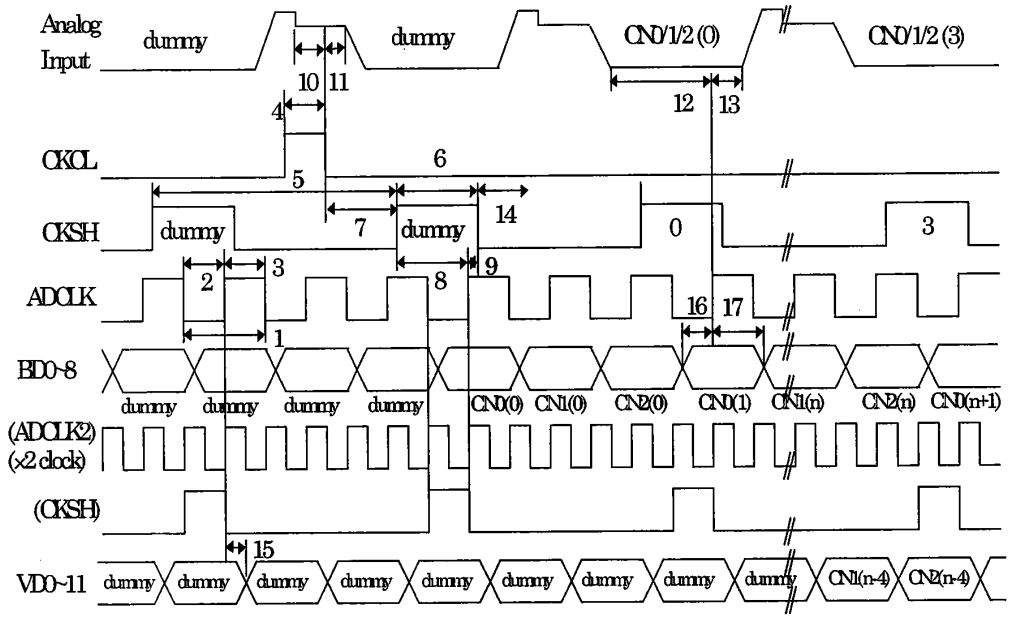


Fig.13 3Channel Mode (Line Clamp for CCD)

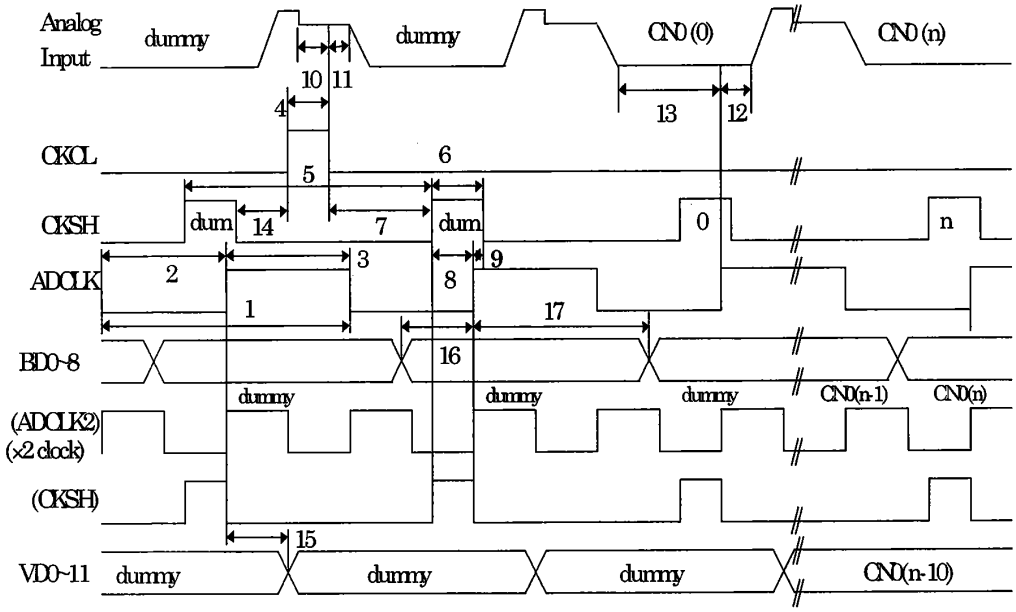


Fig.14 1Channel Mode (Line Clamp for CCD)

(4)Line Clamp mode for CCD timing

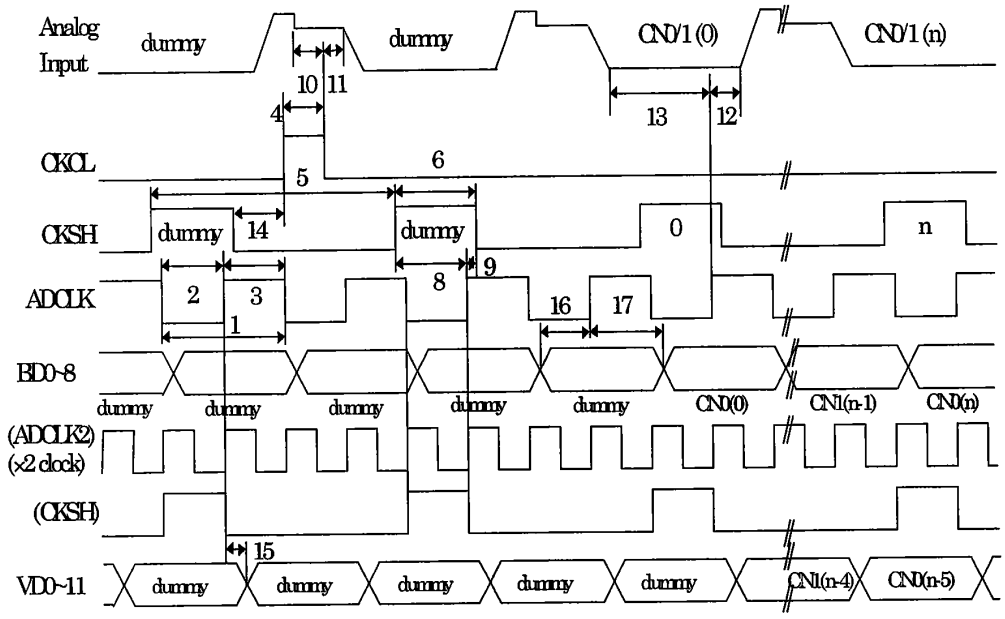


Fig.15 2Channel Mode (Line Clamp for CCD)

(Note 1) ( ) of signal name in Fig.1-.15 shows internal node signal.

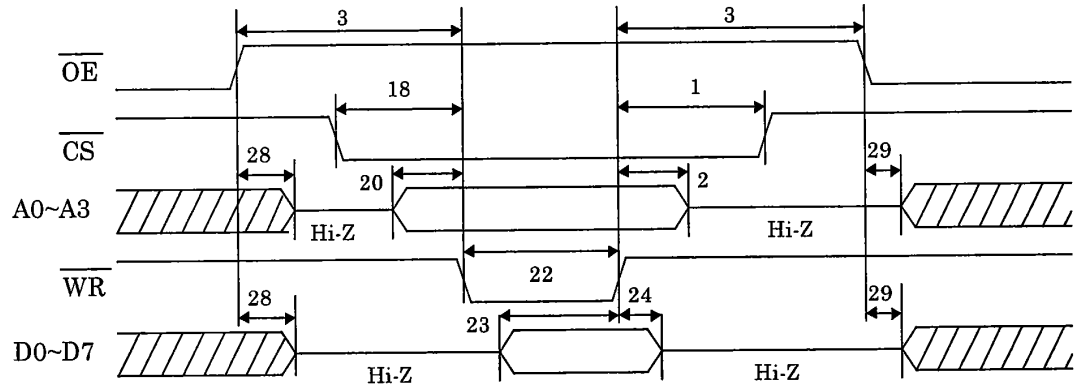


Fig.16 Register Write(Parallel I/F)

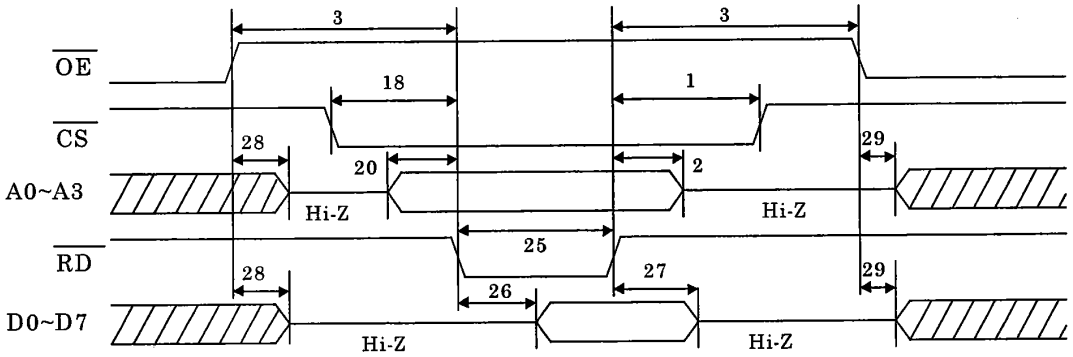


Fig.17 Register Read(Parallel I/F)

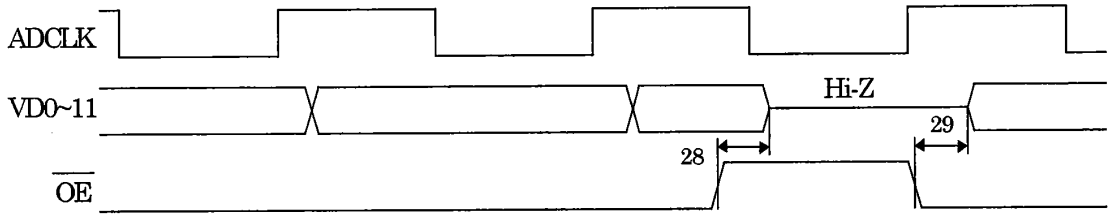


Fig.18 Video Data Disable

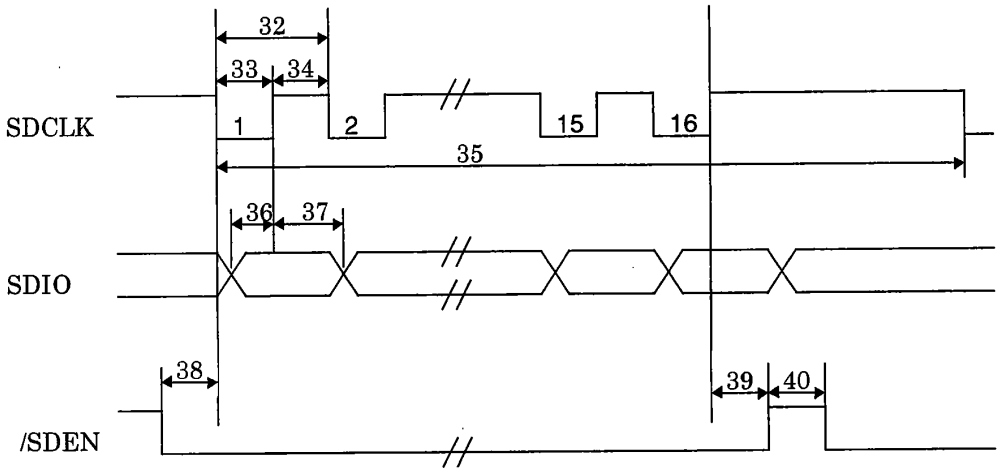


Fig.19 Register Write(3 Wire Serial I/F)

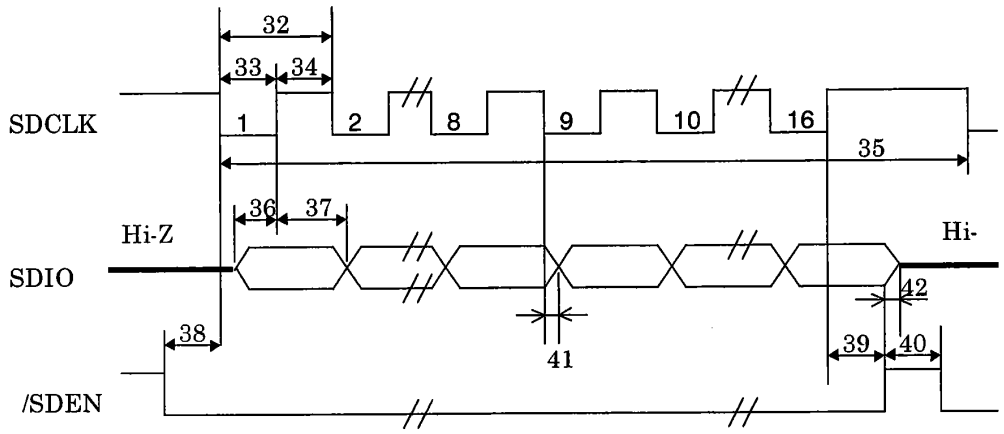


Fig.20 Register Read(3 Wire Serial I/F)

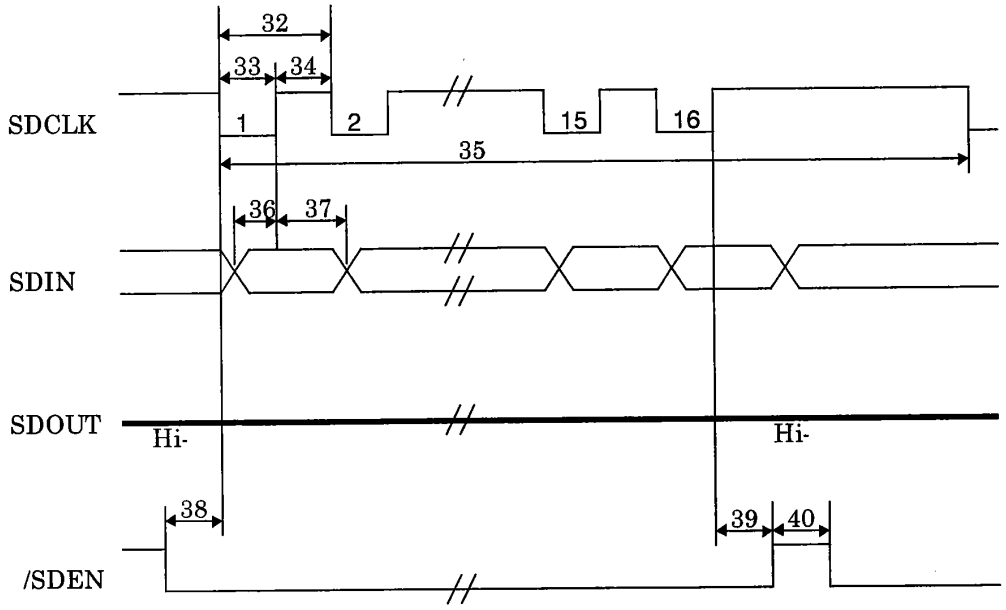


Fig.21 Register Write(4 Wire Serial I/F)

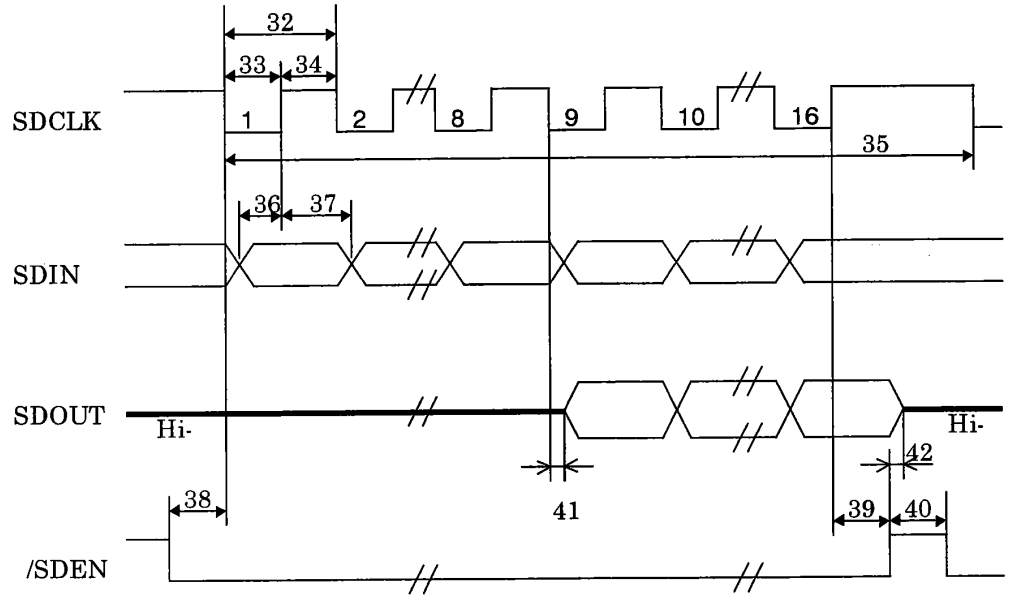


Fig.22 Register Read(4 Wire Serial I/F)

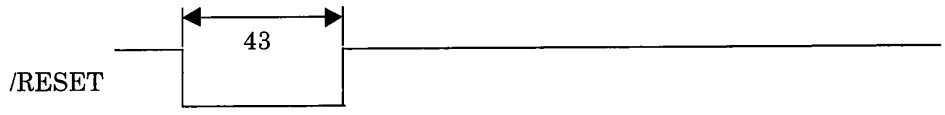
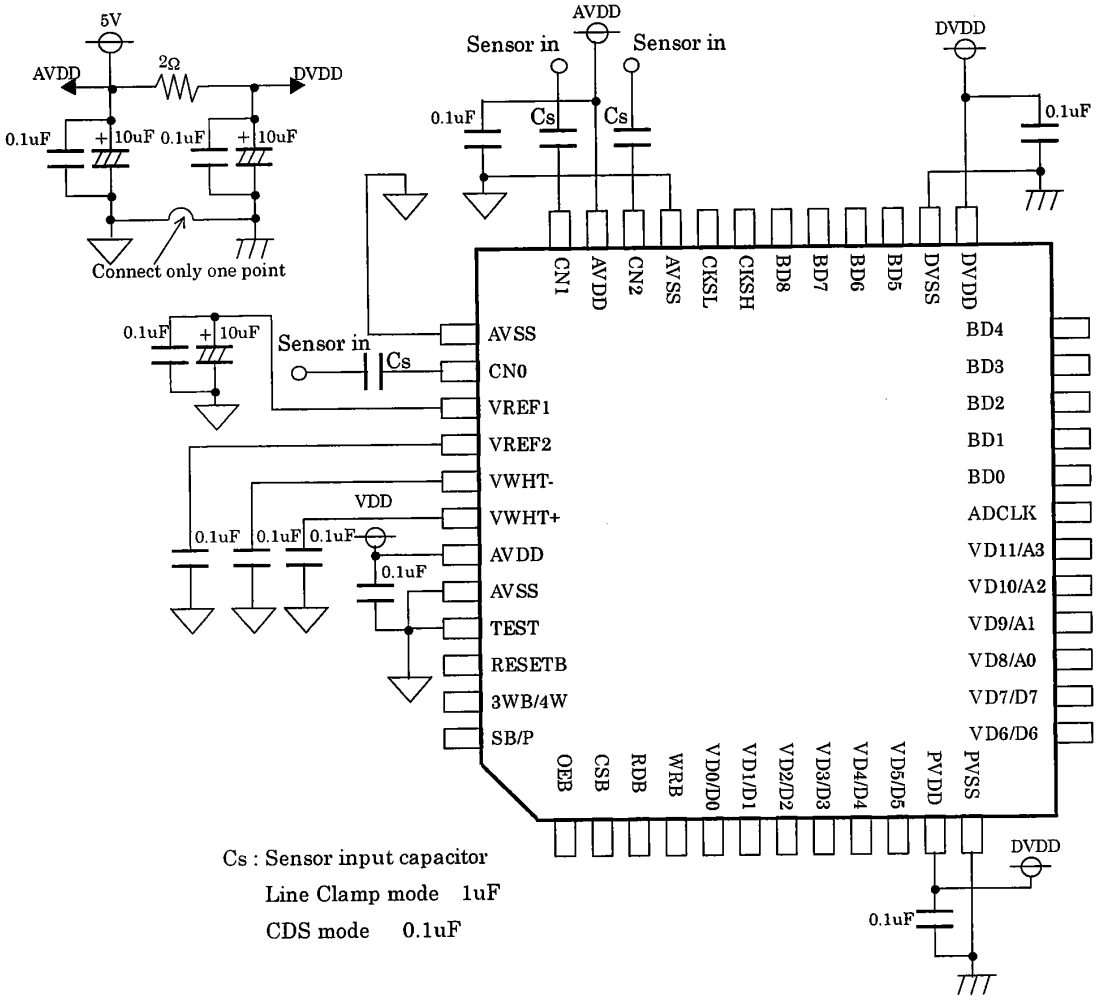


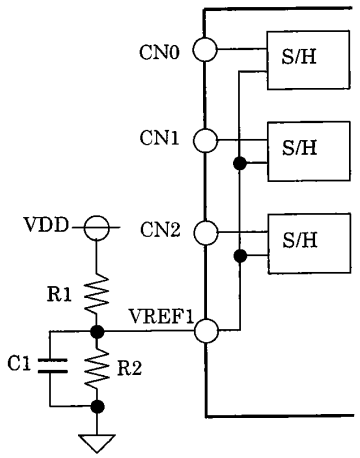
Fig. 23 Reset Pulse

Recommended Circuit



Cs : Sensor input capacitor
Line Clamp mode 1uF
CDS mode 0.1uF

VREF1 input (DC connect mode)



C1 = 0.1uF
R1+R2 = about 2KΩ

Package

■ Marking

(1)Pin 1 indicated(The chamfered corner indicates pin number 1.)

(2)Date code:XXXXXXX(7 digits)

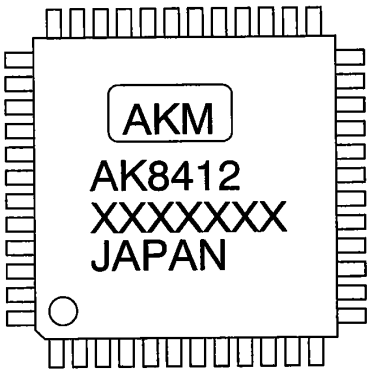
Higher order four digits: week code

Lower order three digits: In-house control code

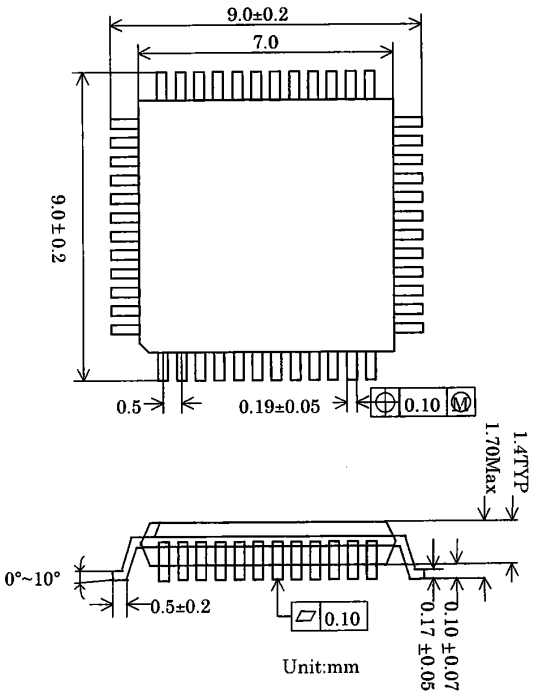
(3)Marking code: AK8412

(4)Manufacturing Country Name Indication: JAPAN

(5)Asahi Kasei Logo



■ Package



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  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
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