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- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

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TDC1044A

Monolithic Video A/D Converter

4-Bit, 25 Msp/s

Features

- 4-bit resolution
- 1/4 LSB non-linearity
- Sample-and-hold circuit not required
- 25 Msp/s conversion rate
- Selectable output format
- 16-lead DIP and 20-lead PLCC packages

Applications

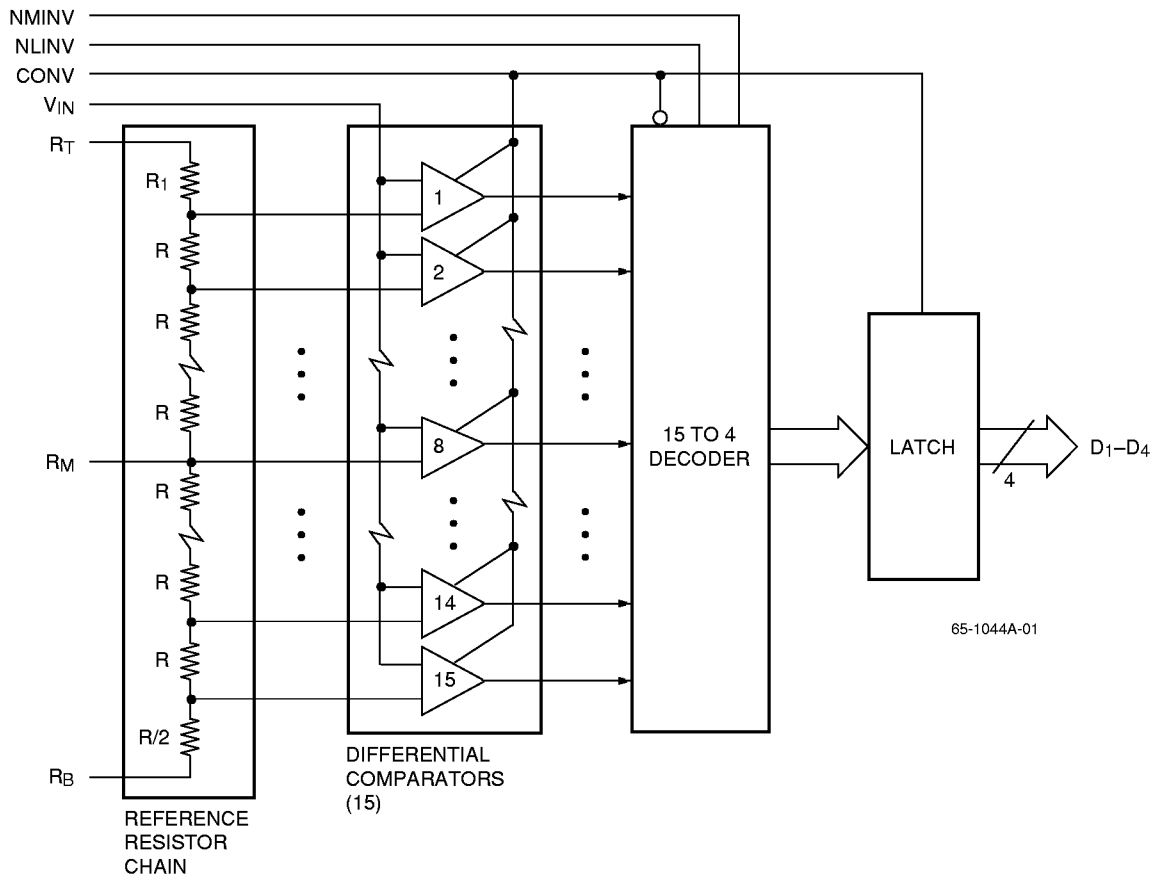
- Digital communications
- Video special effects
- Radar data conversion
- Medical imaging

Description

The TDC1044A is a 25 Msp/s (Megasample per second) full-parallel analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5 MHz into 4-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1044A. All digital inputs and outputs are TTL compatible.

The TDC1044A consists of 15 latching comparators, encoding logic, and an output register. A single convert signal controls the conversion operation. Output formats are true/inverted binary or true/inverted offset two's complement codes.

Block Diagram



Functional Description

General Information

The TDC1044A has three functional sections: a comparator array, encoding logic, and an output register. The comparator array compares the input signal with 15 reference voltages to produce an N-of-15 thermometer code. All the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on. Encoding logic converts the N-of-15 code into binary or two's complement coding and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output register holds the output constant between updates.

Power

The TDC1044A operates from two power supply voltages, +5.0V and -5.2V. The return for ICC (the current drawn from the +5.0V supply) is DGND. The return for IEE (the current drawn from the -5.2V supply) is AGND. All power and ground pins must be connected.

Reference

The TDC1044A converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RB}$ into digital form. V_{RB} (the voltage applied to R_B at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to R_B at the top of the reference resistor chain) should be between +0.1V and -1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT} - V_{RB}$) must be between 0.4V and 1.3V.

Nominal voltages are $V_{RT} = 0.00V$ and $V_{RB} = -1.00V$. These voltages may be varied dynamically up to 10MHz. Due to slight variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required.

A reference middle, R_M , is also provided; this may be used as an input to adjust the mid-scale point in order to improve integral linearity. This point may also be used as a tap to supply a mid-scale voltage to offset the analog input. If V_{RM} is used as an output, it must be connected to a high input impedance device which has small input current. Noise at this point may adversely affect the performance of this device.

Controls

Two function control pins, NMINV and NLINV, set the output format to be either straight binary or offset two's complement, in either true or inverted sense, according to Table 1. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to VCC for a logic "1" and DGND for a logic "0."

NMINV controls the MSB, D1; NLINV controls the three LSBs: D2, D3 and D4.

Convert

The TDC1044A requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within t_{STO} after a rising edge of CONV. The coded result is translated to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. New data becomes valid after a maximum delay time, t_D .

Analog Input

The TDC1044A uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, the source impedance of the driving circuit must be less than 25 Ohms. Within the range of V_{EE} to +0.5V, the input signal will not damage the device. If the input signal is at a voltage between V_{RT} and V_{RB} , the output will be a binary code between 0 and 15 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

TDC1044A outputs are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. Data becomes valid after a maximum delay time (t_D) after the rising edge of CONV. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

No Connects

Pin 3 of the TDC1044A is labeled No Connect (NC), and has no connection to the chip. Connect this pin to AGND for best noise performance.

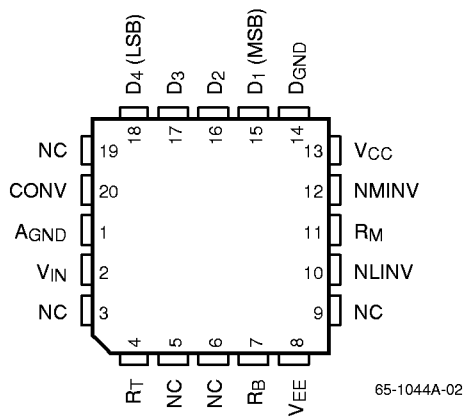
Table 1. Output Coding¹

| Range | Binary | | Offset Two's Complement | |
|-----------|------------------------|----------|-------------------------|----------|
| | True | Inverted | True | Inverted |
| -1.00V FS | NMINV = 1 NLINV = 1 | 0 0 | 0 1 | 1 0 |
| 0.000V | 0000 | 1111 | 1000 | 0111 |
| -0.067V | 0001 | 1110 | 1001 | 0110 |
| -0.133V | 0010 | 1101 | 1010 | 0101 |
| -0.200V | 0011 | 1100 | 1011 | 0100 |
| -0.267V | 0100 | 1011 | 1100 | 0011 |
| -0.333V | 0101 | 1010 | 1101 | 0010 |
| -0.400V | 0110 | 1001 | 1110 | 0001 |
| -0.467V | 0111 | 1000 | 1111 | 0000 |
| -0.533V | 1000 | 0111 | 0000 | 1111 |
| -0.600V | 1001 | 0110 | 0001 | 1110 |
| -0.667V | 1010 | 0101 | 0010 | 1101 |
| -0.733V | 1011 | 0100 | 0011 | 1100 |
| -0.800V | 1100 | 0011 | 0100 | 1011 |
| -0.867V | 1101 | 0010 | 0101 | 1010 |
| -0.933V | 1110 | 0001 | 0110 | 1001 |
| -1.000V | 1111 | 0000 | 0111 | 1000 |

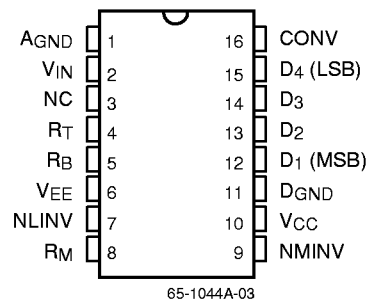
Note:

1. Input voltages are at code centers.

Pin Assignments



20 Lead PLCC



16 Lead DIP

Pin Descriptions

| Pin Name | Pin Number | | Value | Description |
|---------------------|------------|----------------|-----------|----------------------------|
| | DIP | PLCC | | |
| Power | | | | |
| VCC | 10 | 13 | +5.0V | Positive Supply Voltage |
| VEE | 6 | 8 | -5.2V | Negative Supply Voltage |
| DGND | 11 | 14 | 0.0V | Digital Ground |
| AGND | 1 | 1 | 0.0V | Analog Ground |
| Reference | | | | |
| RT | 4 | 4 | 0.0V | Reference Resistor, Top |
| RM | 8 | 11 | -0.5V | Reference Resistor, Middle |
| RB | 5 | 7 | -1.0V | Reference Resistor, Bottom |
| Control | | | | |
| NMINV | 9 | 12 | TTL | Not MSB Invert |
| NLINV | 7 | 10 | TTL | Not LSB Invert |
| Convert | | | | |
| CONV | 16 | 20 | TTL | Convert |
| Analog Input | | | | |
| VIN | 2 | 2 | 0V to -1V | Analog Input Signal |
| Output | | | | |
| D1 | 12 | 15 | TTL | MSB Output |
| D2 | 13 | 16 | TTL | |
| D3 | 14 | 17 | TTL | |
| D4 | 15 | 18 | TTL | LSB Output |
| NC | 3 | 3, 5, 6, 9, 19 | AGND | No Connect |

Absolute Maximum Ratings

(beyond which the device may be damaged)¹

| Type | Parameter | Min | Max | Unit |
|-----------------|--|------|------|------|
| Supply Voltages | VCC (measured to DGND) | -0.5 | 7.0 | V |
| | VEE (measured to AGND) | +0.5 | -7.0 | V |
| | AGND (measured to DGND) | -0.5 | +0.5 | V |
| Input Voltages | CONV, NMINV, NLINV (measured to DGND) | -0.5 | +5.5 | V |
| | VIN, VRT, VRB (measured to AGND) | +0.5 | VEE | V |
| | VRT (measured to VRB) | -2.2 | +2.2 | V |
| Output | Applied voltage (measured to DGND) ² | -0.5 | +5.5 | V |
| | Applied current, externally forced ^{3,4} | -1.0 | +6.0 | mA |
| | Short circuit duration (single output in high state to ground) | | 1 | sec |
| Temperature | Operating, ambient | -55 | +125 | °C |
| | Operating, junction | | +150 | °C |
| | Lead, soldering (10 seconds) | | +300 | °C |
| | Storage | -65 | +150 | °C |

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating Conditions

| Parameter | Min. | Nom. | Max. | Units | |
|-----------|--|------|------|-------|----|
| VCC | Positive Supply Voltage (measured to DGND) | 4.75 | 5.0 | 5.25 | V |
| VEE | Negative Supply Voltage (measured to AGND) | -4.9 | -5.2 | -5.5 | V |
| VAGND | Analog Ground Voltage (measured to DGND) | -0.1 | 0.0 | 0.1 | V |
| tPWL | CONV Pulse Width, LOW | 17 | | | ns |
| tPWH | CONV Pulse Width, HIGH | 17 | | | ns |
| VIL | Input Voltage, Logic LOW | | | 0.8 | V |
| VIH | Input Voltage, Logic HIGH | 2.0 | | | V |
| IOL | Output Current, Logic LOW | | | 4.0 | mA |
| IOH | Output Current, Logic HIGH | | | -400 | μA |
| VRT | Most Positive Reference | -1.9 | 0.0 | 0.1 | V |
| VRB | Most Negative Reference | -2.1 | -1.0 | -0.1 | V |
| VRT – VRB | Reference Differential | 0.2 | 1.0 | 2.0 | V |
| VIN | Input Voltage | VRB | | VRT | V |
| TA | Ambient Temperature, Still Air | 0 | | 70 | °C |

Electrical Characteristics

Within specified operating conditions

| Parameter | | Test Conditions | Min. | Max. | Units |
|------------------|----------------------------------|--|------|------|-------|
| I _{CC} | Positive Supply Current | V _{CC} = Max, static ¹ | | 15 | mA |
| I _{EE} | Negative Supply Current | V _{EE} = Max, static | | | |
| | | T _A = 0°C to 70°C | | -50 | mA |
| | | T _A = 70°C | | -40 | mA |
| I _{REF} | Reference Current | V _{RT} , V _{RB} = Nom | | 2 | mA |
| R _{REF} | Total Reference Resistance | | 500 | | Ohms |
| R _{IN} | Input Equivalent Resistance | V _{RT} , V _{RB} = Nom, V _{IN} = V _{RB} | 250 | | Kohms |
| C _{IN} | Input Capacitance | | | 25 | pF |
| I _{CB} | Input Constant Bias Current | V _{EE} = Max | | 40 | μA |
| I _{IL} | Input Current, Logic LOW | V _{CC} = Max, V _I = 0.5V | | | |
| | | CONV | | -0.8 | mA |
| | | NMINV, NLINV | | -0.8 | mA |
| I _{IH} | Input Current, Logic HIGH | V _{CC} = Max, V _I = 2.4V | | 200 | μA |
| I _I | Input Current, Max Input Voltage | V _{CC} = Max, V _I = 5.5V | | 1.0 | mA |
| V _{OL} | Output Voltage, Logic LOW | V _{CC} = Min, I _{OL} = Max | | 0.5 | V |
| V _{OH} | Output Voltage, Logic HIGH | V _{CC} = Min, I _{OH} = Max | 2.4 | | V |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max, One pin to ground, one second duration, Output HIGH | | -300 | mA |
| C _I | Digital Input Capacitance | T _A = 25°C, F = 1 MHz | | 15 | pF |

Note:

1. Worst case: all digital inputs and outputs LOW.

Switching Characteristics

Within specified operating conditions

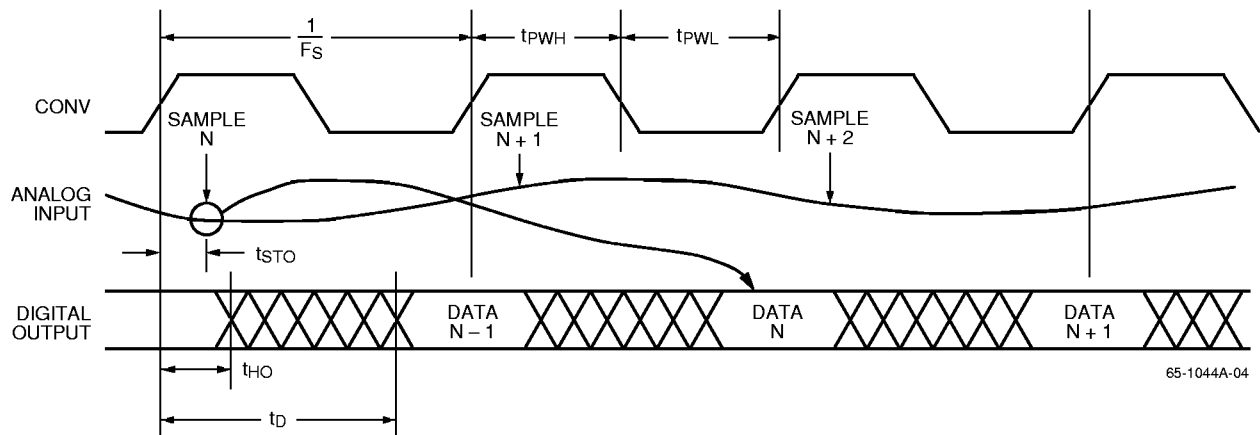
| Parameter | Test Conditions | Min. | Max. | Units |
|------------------|--------------------------|--|------|-------|
| F _S | Maximum Conversion Rate | V _{CC} = Min, V _{EE} = Min | 25 | MspS |
| t _{STO} | Sampling Time Offset | V _{CC} = Min, V _{EE} = Min | | 10 ns |
| t _D | Digital Output Delay | V _{CC} = Min, V _{EE} = Min, Load 1 | | 30 ns |
| t _{HO} | Digital Output Hold Time | V _{CC} = Max, V _{EE} = Max, Load 1 | 5 | ns |

System Performance Characteristics

Within specified operating conditions

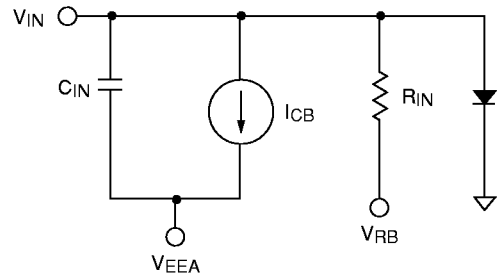
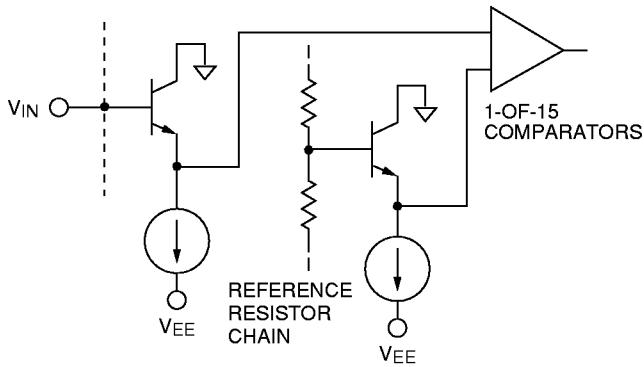
| Parameter | Test Conditions | Min. | Max. | Units | |
|-----------|--------------------------------------|----------------|------|-------|-----------|
| ELI | Linearity Error Integral Independent | VRB = Nom | | 1.6 | % |
| ELD | Linearity Error Differential | | | 1.6 | % |
| CS | Code Size | VRT, VRB = Nom | 75 | 125 | % Nominal |
| EOT | Offset Error Top | VIN = VRT | | +30 | mV |
| EOB | Offset Error Bottom | VIN = VRB | | +40 | mV |
| Tco | Offset Error Temperature Coefficient | | | ±20 | µV/°C |
| BW | Bandwidth, Full Power Input | | 12.5 | | MHz |
| tTR | Transient Response, Full Scale | | | 10 | ns |
| EAP | Aperture Error | | | 30 | ps |

Timing Diagram



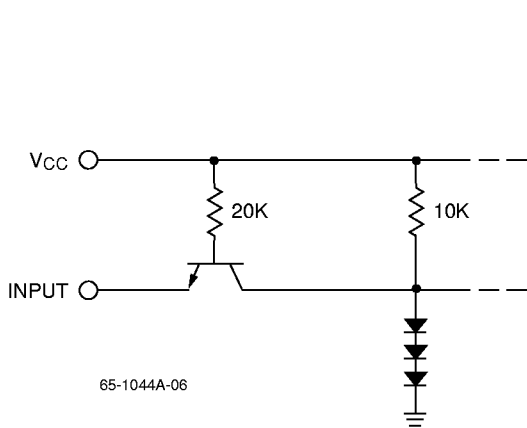
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Equivalent Circuits



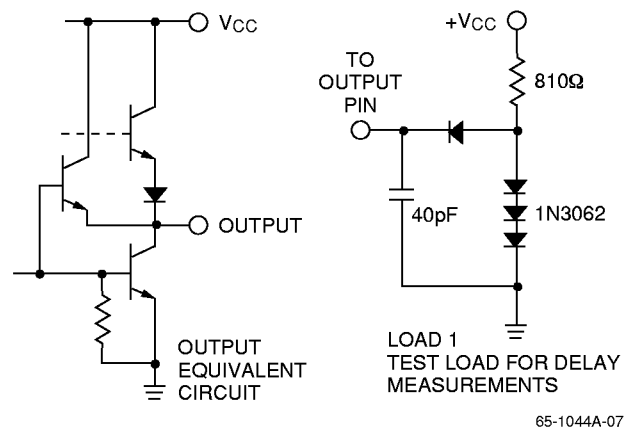
65-1044A-05

Figure 1. Simplified Analog Input Equivalent Circuit



65-1044A-06

Figure 2. Digital Input Equivalent Circuit



65-1044A-07

Figure 3. Output Circuits

Applications Discussion

Calibration

To calibrate the TDC1044A, adjust V_{RT} and V_{RB} to set the 1st and 15th thresholds to the desired voltages. Assuming a 0V to -1V desired range, continuously strobe the converter with -0.0033V (1/2 LSB from 0.000V) on the analog input, and adjust V_{RT} for output toggling between codes 0000 and 0001. Then apply -0.976V (1/2 LSB from -1.000V) and adjust V_{RB} for toggling between codes 1110 and 1111. Instead of adjusting V_{RT} , R_T can be connected to analog ground and the 0V end of the range calibrated with an amplifier offset control. R_B is a convenient point for gain adjustment that is not in the analog signal path.

Typical Interface Circuit

The TDC1044A does not require a special input buffer amplifier to drive the analog input because of its low input capacitance. A terminated low-impedance transmission line (<100 Ohms) connected to the V_{IN} terminal of the device is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain stability. The typical interface circuit in Figure 4 shows a simple amplifier and voltage reference circuit that may be used with the device. U2 is a wide-band operational amplifier with a gain factor of -1. As the video

input increases from zero to one volt, V_{IN} of the TDC1044A decreases from zero to -1 volt. With true binary selected ($N_{MINV} = 1$ and $N_{LINV} = 1$), output codes increase from 0000 to 1111.

A small value resistor, R_{12} , serves to isolate the small input capacitance of the A/D converter from the amplifier output and insure frequency stability. Pulse and frequency response of the amplifier are optimized by variable capacitor C_{12} . The reference voltage for the TDC1044A is generated by amplifier U3. System gain is adjusted by varying R_9 , which controls the reference voltage level to the A/D converter.

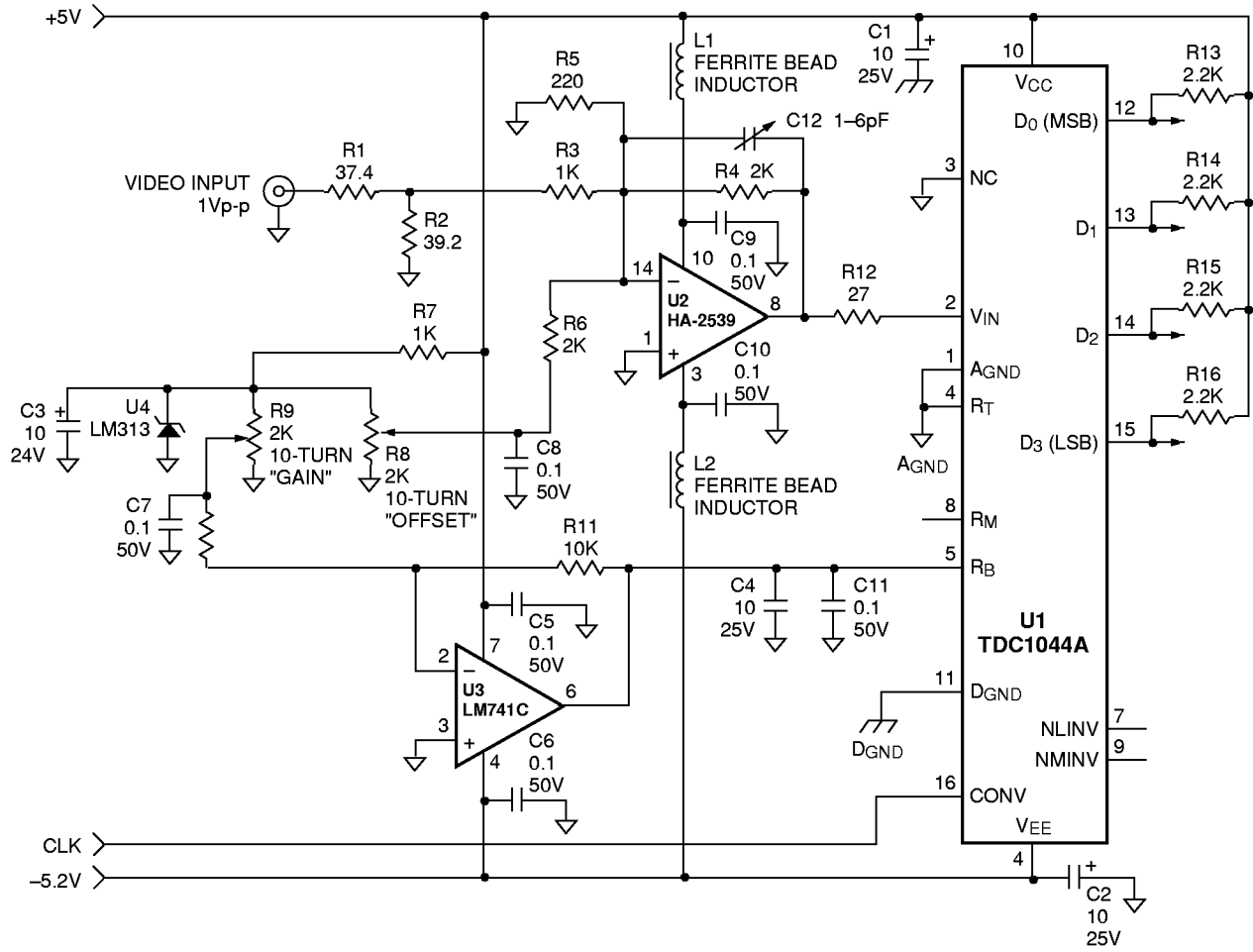
Input voltage range and input impedance for the circuit are determined by resistors R_1 and R_2 . Formulas for calculating values for these input resistors are:

$$R_1 = \frac{1}{\left(\frac{2V_R}{Z_{IN}}\right) - \frac{1}{1000}}$$

and

$$R_2 = Z_{IN} - \left(\frac{1000 R_1}{1000 + R_1}\right)$$

where V_R is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R_3 . As shown, the circuit is set up for 1Vp-p 75 Ohm video input.



65-1044A-08

Figure 4. Typical Interface Circuit

Notes:

Notes:

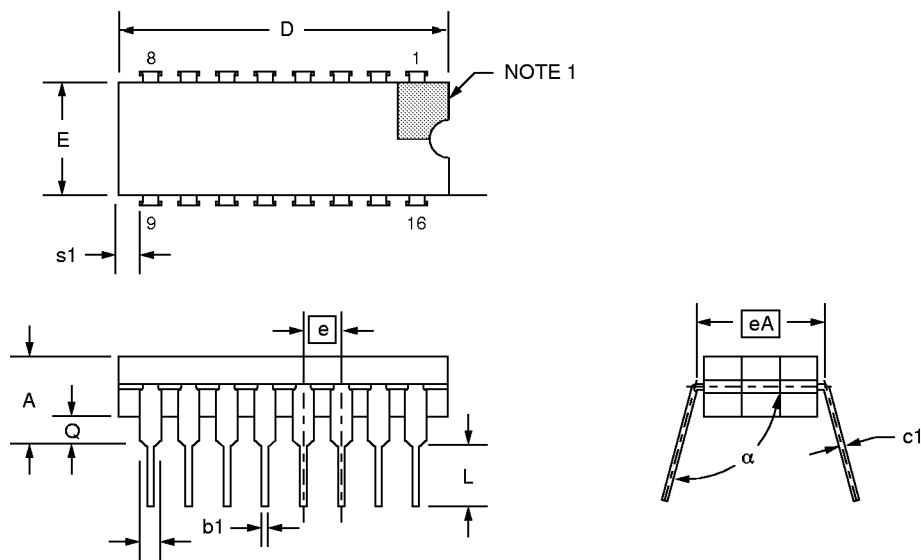
Mechanical Dimensions

16-Lead Ceramic DIP Package

| Symbol | Inches | | Millimeters | | Notes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----------|------|-------------|-------|-------|---|------|------|-------|-------|---|---|------|------|------|------|---|---|----------|--|----------|--|------|----|----------|--|----------|--|---|---|------|------|------|------|--|---|------|------|-----|------|---|----|------|---|-----|---|---|----------|-----|------|-----|------|--|
| | Min. | Max. | Min. | Max. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | — | .200 | — | 5.08 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b1 | .014 | .023 | .36 | .58 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| b2 | .050 | .065 | 1.27 | 1.65 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| c1 | .008 | .015 | .20 | .38 | 8 | D | .745 | .840 | 18.92 | 21.33 | 4 | E | .220 | .310 | 5.59 | 7.87 | 4 | e | .100 BSC | | 2.54 BSC | | 5, 9 | eA | .300 BSC | | 7.62 BSC | | 7 | L | .115 | .160 | 2.92 | 4.06 | | Q | .015 | .060 | .38 | 1.52 | 3 | s1 | .005 | — | .13 | — | 6 | α | 90° | 105° | 90° | 105° | |
| D | .745 | .840 | 18.92 | 21.33 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | .220 | .310 | 5.59 | 7.87 | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e | .100 BSC | | 2.54 BSC | | 5, 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| eA | .300 BSC | | 7.62 BSC | | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | .115 | .160 | 2.92 | 4.06 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Q | .015 | .060 | .38 | 1.52 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| s1 | .005 | — | .13 | — | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| α | 90° | 105° | 90° | 105° | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within $\pm .010$ (.25mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (leads number 1, 8, 9, and 16).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when " α " is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Fourteen spaces.



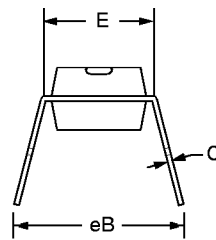
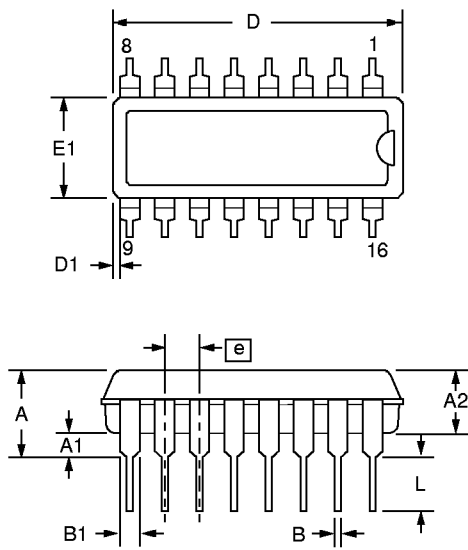
Mechanical Dimensions (continued)

16-Lead Plastic DIP Package

| Symbol | Inches | | Millimeters | | Notes |
|--------|----------|------|-------------|-------|-------|
| | Min. | Max. | Min. | Max. | |
| A | — | .210 | — | 5.33 | |
| A1 | .015 | — | .38 | — | |
| A2 | .115 | .195 | 2.93 | 4.95 | |
| B | .014 | .022 | .36 | .56 | |
| B1 | .045 | .070 | 1.14 | 1.78 | |
| C | .008 | .015 | .20 | .38 | 4 |
| D | .745 | .840 | 18.92 | 21.33 | 2 |
| D1 | .005 | — | .13 | — | |
| E | .300 | .325 | 7.62 | 8.26 | |
| E1 | .240 | .280 | 6.10 | 7.11 | 2 |
| e | .100 BSC | | 2.54 BSC | | |
| eB | — | .430 | — | 10.92 | |
| L | .115 | .160 | 2.92 | 4.06 | |
| N | 16 | | 16 | | 5 |

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



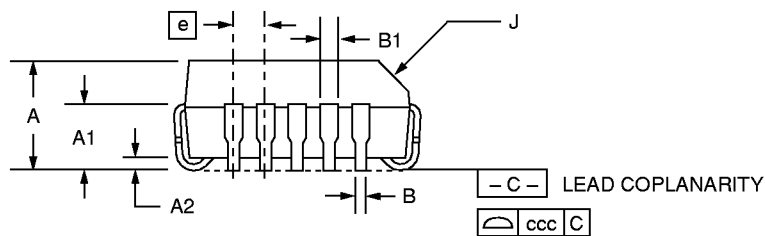
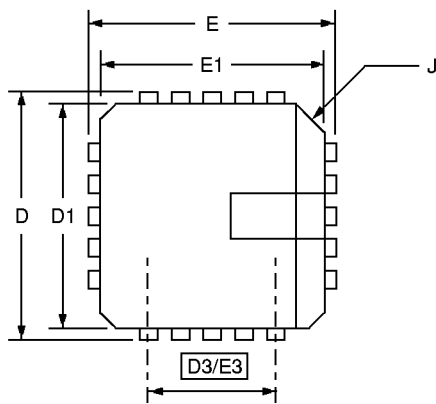
Mechanical Dimensions (continued)

20-Lead PLCC Package

| Symbol | Inches | | Millimeters | | Notes |
|--------|----------|------|-------------|-------|-------|
| | Min. | Max. | Min. | Max. | |
| A | .165 | .180 | 4.19 | 4.57 | |
| A1 | .090 | .120 | 2.29 | 3.05 | |
| A2 | .020 | — | .51 | — | |
| B | .013 | .021 | .33 | .53 | |
| B1 | .026 | .032 | .66 | .81 | |
| D/E | .385 | .395 | 9.78 | 10.03 | |
| D1/E1 | .350 | .356 | 8.89 | 9.04 | 3 |
| D3/E3 | .200 BSC | | 5.08 BSC | | |
| e | .050 BSC | | 1.27 BSC | | |
| J | .042 | .048 | 1.07 | 1.22 | 2 |
| ND/NE | 5 | | 5 | | |
| N | 20 | | 20 | | |
| ccc | — | .004 | — | 0.10 | |

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .245" (.101mm)



Ordering Information

| Product Number | Temperature Range | Screening | Package | Package Marking |
|----------------|-------------------|------------|---------------------|-----------------|
| TDC1044AB9C | 0°C to 70°C | Commercial | 16-Lead Ceramic DIP | 1044AB9C |
| TDC1044AN9C | 0°C to 70°C | Commercial | 16-Lead Plastic DIP | 1044AN9C |
| TDC1044AR4C | 0°C to 70°C | Commercial | 20-Lead PLCC | 1044AR4C |

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.