HI1176

Pb-Free and RoHS Compliant

NOT RECOMMENDED FOR NEW DESIGNS
See HI1179

October 25, 2005

8-Bit, 20 MSPS, Flash A/D Converter

Features

- **Resolution ±0.5 LSB (DNL) 8-Bit**
- **Maximum Sampling Frequency . . . . . 20 MSPS**
- **Low Power Consumption at 20 MSPS (Typ) (Reference Current Excluded) 60mW**
- **Built-In Sync Clamp Function**
- **Built-In Monostable Multivibrator for Clamp Pulse Generation**
- **Built-In Sync Pulse Polarity Selection Function**
- **Clamp Pulse Direct Input Possible**
- **Built-In Clamp ON/OFF Function**
- **Built-In Reference Voltage Self Bias Circuit**
- **Input CMOS Compatible**
- **Three-State TTL Compatible Output**
- **Single +5V Power Supply**
- **Low Input Capacitance (Typ) 11pF**
- **Reference Impedance (Typ) 300Ω**
- **Direct Replacement for the Sony CXD1176**

Description

The HI1176 is an 8-bit, CMOS analog-to-digital converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 20 MSPS. For higher sampling rates, refer to the pin-for-pin compatible HI1179 data sheet, document number 3666.

Applications

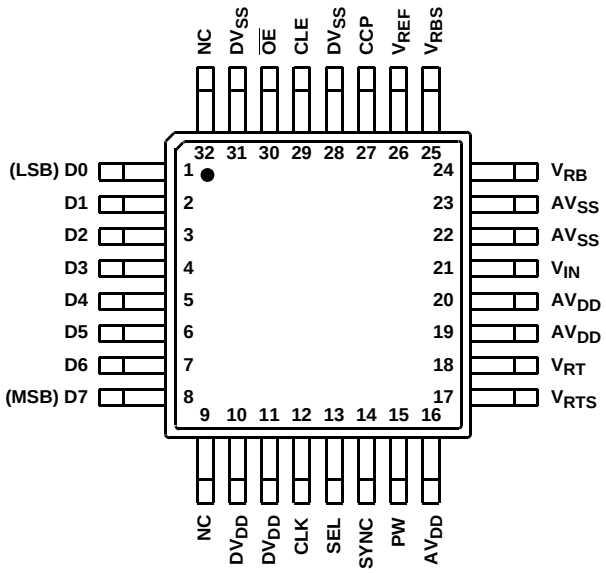
- **Video Digitizing**
- **Image Scanners**
- **Low Cost High Speed Data Acquisition Systems**
- **Multimedia**

Ordering Information

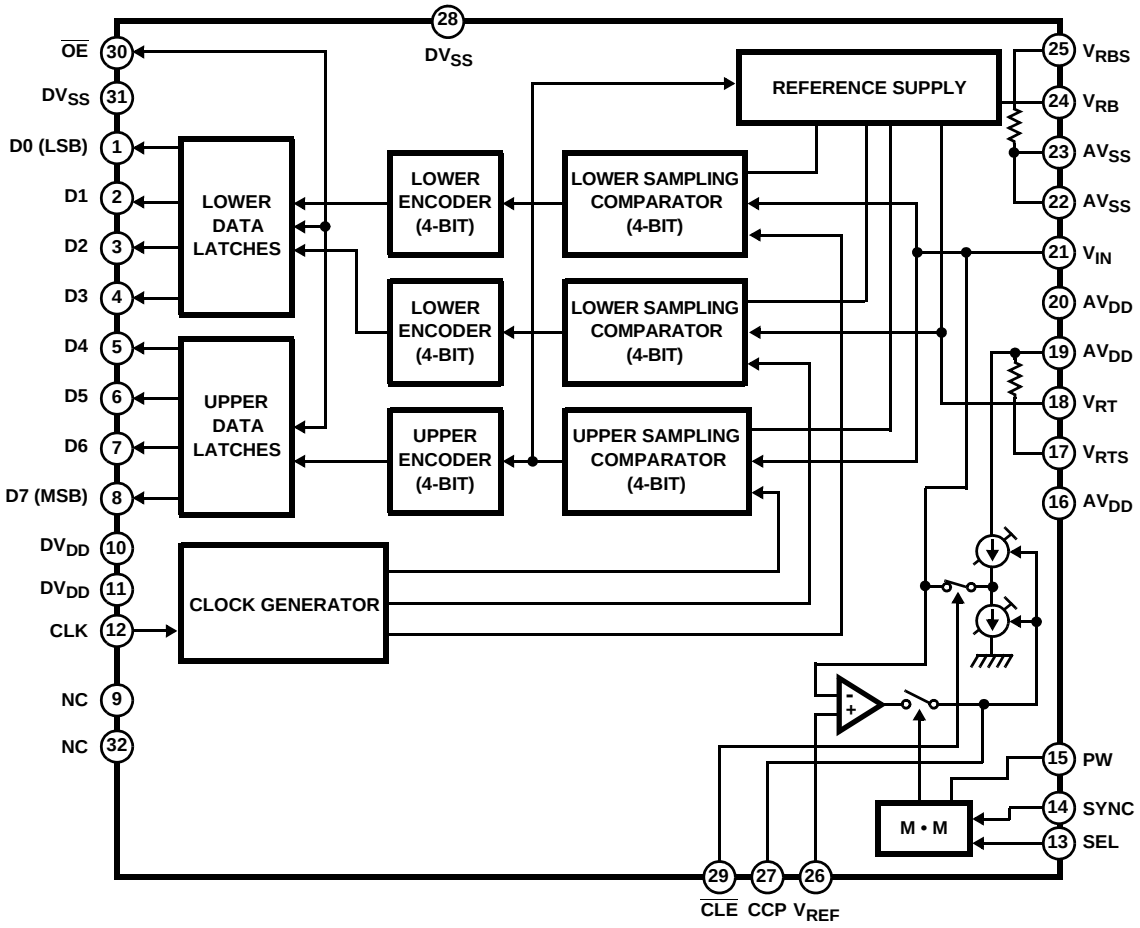
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI1176JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S
HI1176-EV	25	Evaluation Board	

Pinout

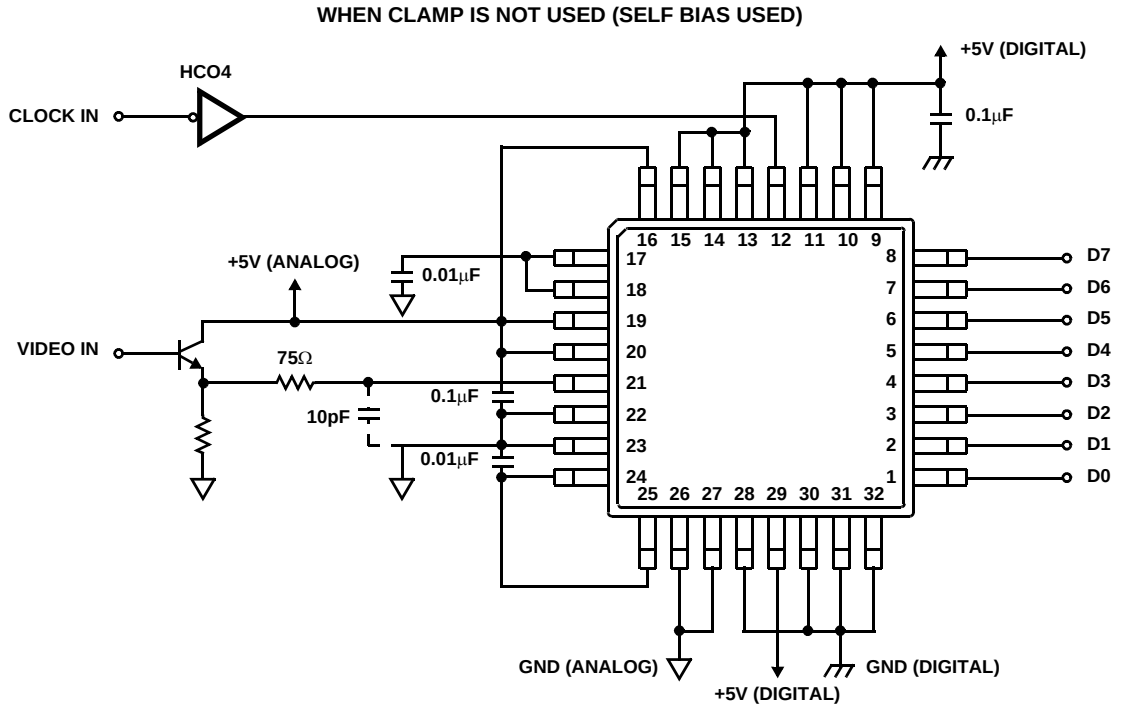
HI1176
(MQFP)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Analog Input Voltage, V_{IN} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Input Voltage, CLK . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V

Operating Conditions (Note 1)

Temperature Range, T_A . . . . . -40^oC to 85^oC
Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} . . . . . +4.75V to +5.25V
|DGND-AGND| . . . . . 0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . 0V and Above
V_{RT} . . . . . 2.8V and Below
Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT} ($1.8V_{P-P}$ to AV_{DD})
Clock Pulse Width
t_{PW1} . . . . . 25ns (Min)
t_{PW0} . . . . . 25ns (Min)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	122

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

f_C = 20 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25^oC (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Offset Voltage E_{OT}		-60	-40	-20	mV
E_{OB}		+20	+40	+60	mV
Integral Non-Linearity, INL	f_C = 20 MSPS, V_{IN} = 0.5V to 2.5V	-	±0.5	±1.3	LSB
Differential Non-Linearity, DNL	f_C = 20 MSPS, V_{IN} = 0.5V to 2.5V	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise Ratio, SINAD $\frac{\text{RMS Signal}}{\text{Signal-To-Noise + Distortion Ratio, SINAD}}$	f_S = 20MHz, f_{IN} = 1MHz	-	46	-	dB
	f_S = 20MHz, f_{IN} = 3.58MHz	-	46	-	dB
Maximum Conversion Speed, f_C	V_{IN} = 0.5V to 2.5V, f_{IN} = 1kHz Ramp	20	35	-	MSPS
Minimum Conversion Speed		-	-	0.5	MSPS
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, f_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Sampling Delay, t_{DS}		-	4	-	ns
ANALOG INPUTS					
Analog Input Bandwidth (-1dB), BW		-	18	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1.5V + $0.07V_{RMS}$	-	11	-	pF

Electrical Specifications f_C = 20 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE INPUT						
Reference Pin Current, I_{REF}			4.5	6.6	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}			230	300	450	Ω
INTERNAL VOLTAGE REFERENCES						
Self Bias						
V_{RB}	Short V_{RB} and V_{RBS}, Short V_{RT} and V_{RTS}		0.48	0.52	0.56	V
V_{RT} - V_{RB}			1.96	2.08	2.22	V
DIGITAL INPUTS						
Digital Input Voltage						
V_{IH}			4.0	-	-	V
V_{IL}			-	-	1.0	V
Digital Input Current						
I_{IH}	V_{DD} = Max	V_{IH} = V_{DD}	-	-	5	µA
I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS						
Digital Output Current						
I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = Min	V_{OH} = V_{DD} -0.5V	-1.1	-	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	-	-	mA
Digital Output Current						
I_{OZH}	$\overline{OE}$ = V_{DD}, V_{DD} = Max	V_{OH} = V_{DD}	-	-	16	µA
I_{OZL}		V_{OL} = 0V	-	-	16	µA
TIMING CHARACTERISTICS						
Output Data Delay, t_{DL}			-	18	30	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	f_C = 20 MSPS, NTSC Ramp Wave Input		-	12	18	mA
CLAMP CHARACTERISTICS						
Clamp Offset Voltage, E_{OC}	V_{IN} = DC, PWS = 3µs	V_{REF} = 0.5V	0	+20	+40	mV
		V_{REF} = 2.5V	-50	-30	-10	mV
Clamp Pulse Width (Sync Pin Input), t_{CPW}	C = 100pF, R = 130kΩ on Pin 15		1.75	2.75	3.75	µs
Clamp Pulse Delay, t_{CPD}			-	25	-	ns

NOTE:

1. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

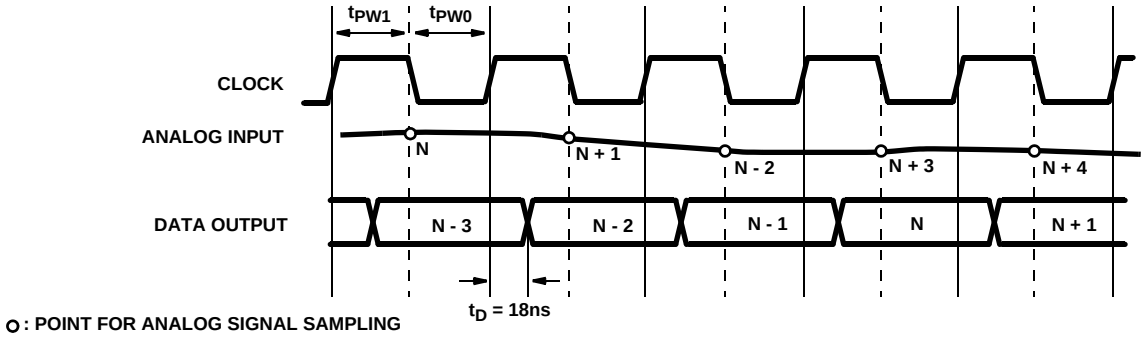


FIGURE 1.

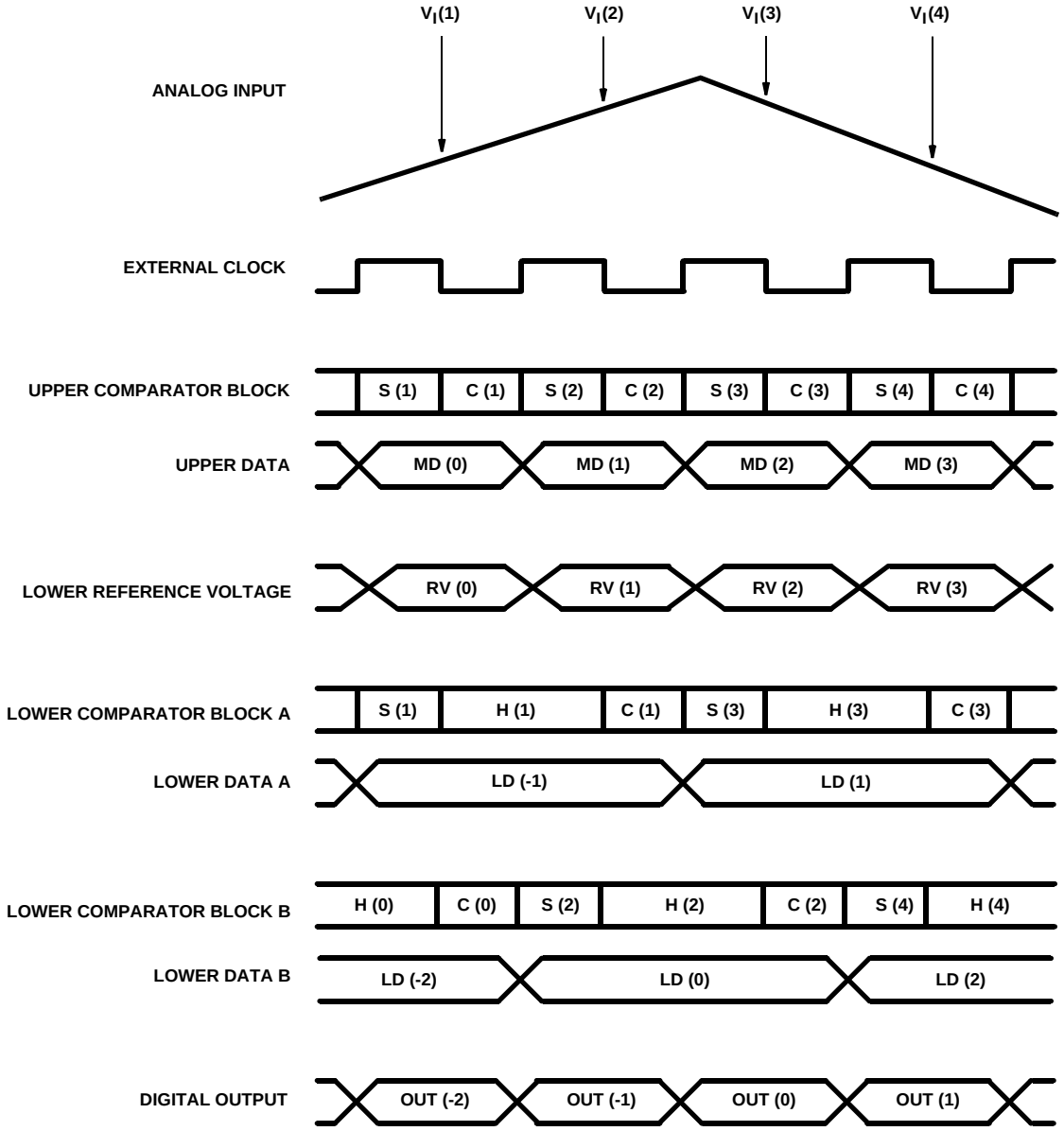


FIGURE 2.

Typical Performance Curves

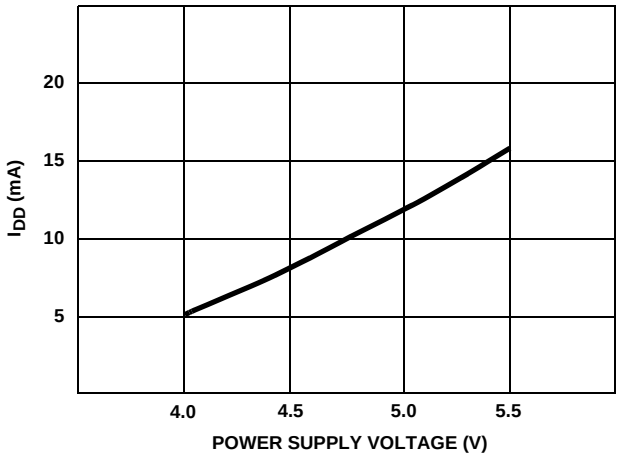


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

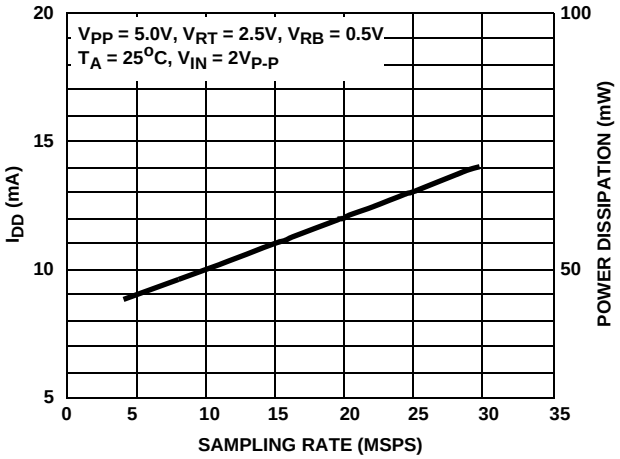


FIGURE 4. SUPPLY CURRENT AND POWER vs SAMPLING RATE

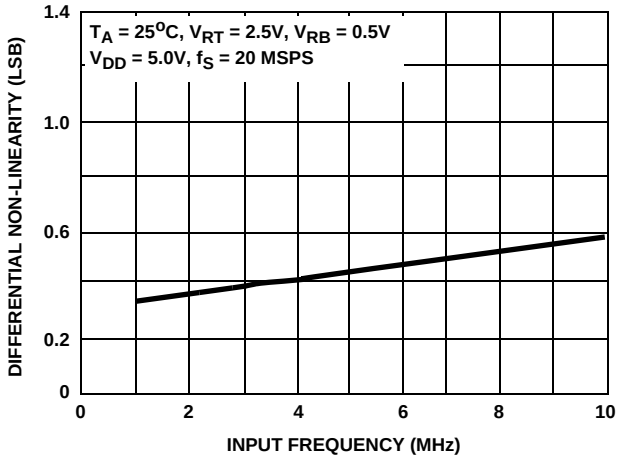
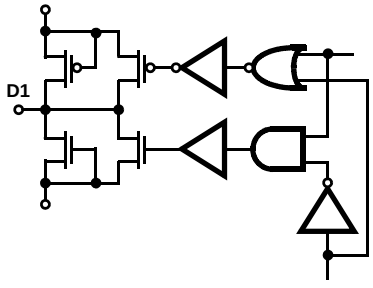
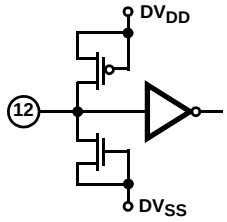
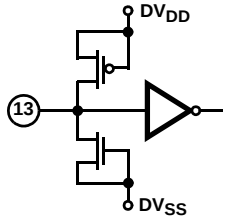
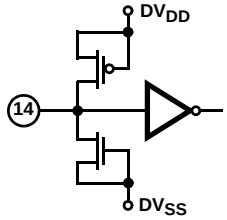
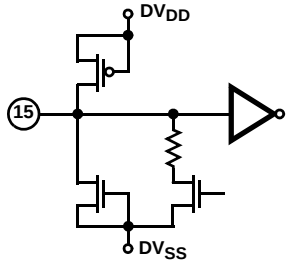
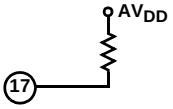
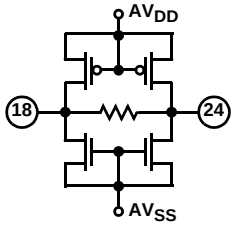


FIGURE 5. DIFFERENTIAL NON-LINEARITY vs INPUT FREQUENCY

Pin Descriptions

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1-8	D0 to D7		D0 (LSB) to D7 (MSB) Output.
10, 11	DV_{DD}		Digital +5V.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
12	CLK		Clock Input.
13	SEL		When SEL is low, the falling edge of Pin 14 (sync) triggers the monostable. When SEL is high, the rising edge of Pin 14 (sync) triggers the monostable.
14	SYNC		Trigger pulse input to the monostable multivibrator. Trigger polarity can be controlled by Pin 13 (SEL).
15	PW		When a clamp pulse is generated by the monostable, the pulse width is determined by the external R and C. When the clamp pulse is directly input, it is input to Pin 15 (PW).
16, 19, 20	AV_{DD}		Analog +5V.
17	V_{RTS}		When shorted with V_{RT}, generates approx. +2.6V.
18	V_{RT}		Reference Voltage (Top).
24	V_{RB}		Reference Voltage (Bottom).

Pin Descriptions (Continued)

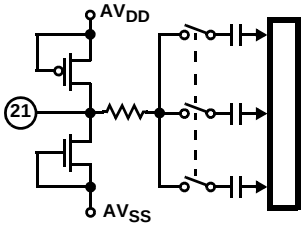
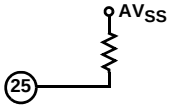
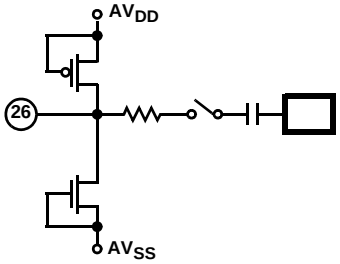
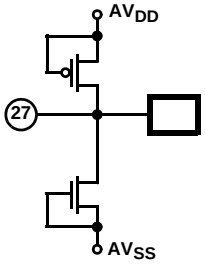
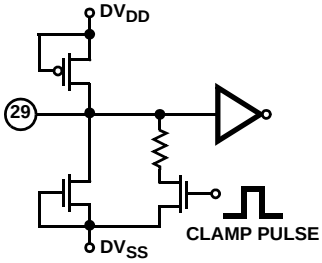
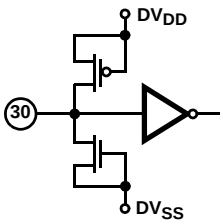
PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	V_{IN}		Analog Input.
22, 23	AV_{SS}		Analog Ground.
25	V_{RBS}		When shorted with V_{RB}, generates approx. +0.5V.
26	V_{REF}		Clamp Reference Voltage Input.
27	CCP		Integrates the voltage for clamp control.
28, 31	DV_{SS}		Digital GND.
29	$\overline{CLE}$		When $\overline{CLE}$ is low, clamp function is activated. When $\overline{CLE}$ is high, clamp function is OFF and only the usual A/D converter function is active. By connecting $\overline{CLE}$ pin to DV_{DD} via a several hundred Ω resistance, the clamp pulse can be tested.
30	$\overline{OE}$		When $\overline{OE}$ is low, data is valid. When $\overline{OE}$ is high, D0 to D7 pins are high impedance.

TABLE 1. A/D OUTPUT CODE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
V_{RT}	255	1	1	1	1	1	1	1	1
	•					•			
•	•					•			
•	•					•			
•									
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•									
•	•					•			
•	•					•			
	•					•			
V_{RB}	0	0	0	0	0	0	0	0	0

Detailed Description

The HI1176 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling/autozero (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between V_{RT}-V_{RB} is constantly applied to the upper 4-bit comparator group. $V_I(1)$ is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples $V_I(1)$ on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input.

Reference Input

The range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal bias generator will set V_{RTS} to 2.5V and V_{RBS} to 0.5V. These can be used as the part reference by shorting V_{RT} and V_{RTS} and V_{RB} to V_{RBS}. The analog input range of the A/D will now be from 0.5V to 2.5V. If a V_{RB} below +0.5V is used the linearity of the part will be degraded.

Bypass V_{RT} and V_{RB} to analog ground with a 0.1µF capacitor.

Clamp Operation

The HI1176 provides a clamp option that allows the user to clamp a portion of the analog input to a voltage set by the V_{REF} pin. The clamp function is enabled by bringing $\overline{CLE}$ low. An internal monostable multivibrator is provided that can be used to generate the clamp pulses. The monostable pulse width is determined by the external R and C connected to the PW pin. The trigger to the monostable is applied on the SYNC pin. The edge that triggers the monostable is determined by the SEL pin. When SEL is low the falling edge will trigger the monostable and when SEL is high the rising edge will trigger the monostable. Figure 6 shows the HI1176 configured for this mode of operation. The clamp pulse is latched by the ADC sampling clock. This is not necessary to the operation of the clamp function but if this is not done then a slight beat might be generated as vertical sag according to the relation between the sampling frequency and the clamp frequency.

The HI1176 can also be configured to operate with an external clamp pulse. In this case a negative going pulse is input to the PW pin. V_{IN} will now be clamped during the low period of the clamp pulse to the voltage on the V_{REF} pin. Figure 7 shows the HI1176 configured for this mode of operation.

Figure 1 illustrates the operation of HI1176 when the clamp function is not used.

Typical Application Circuits

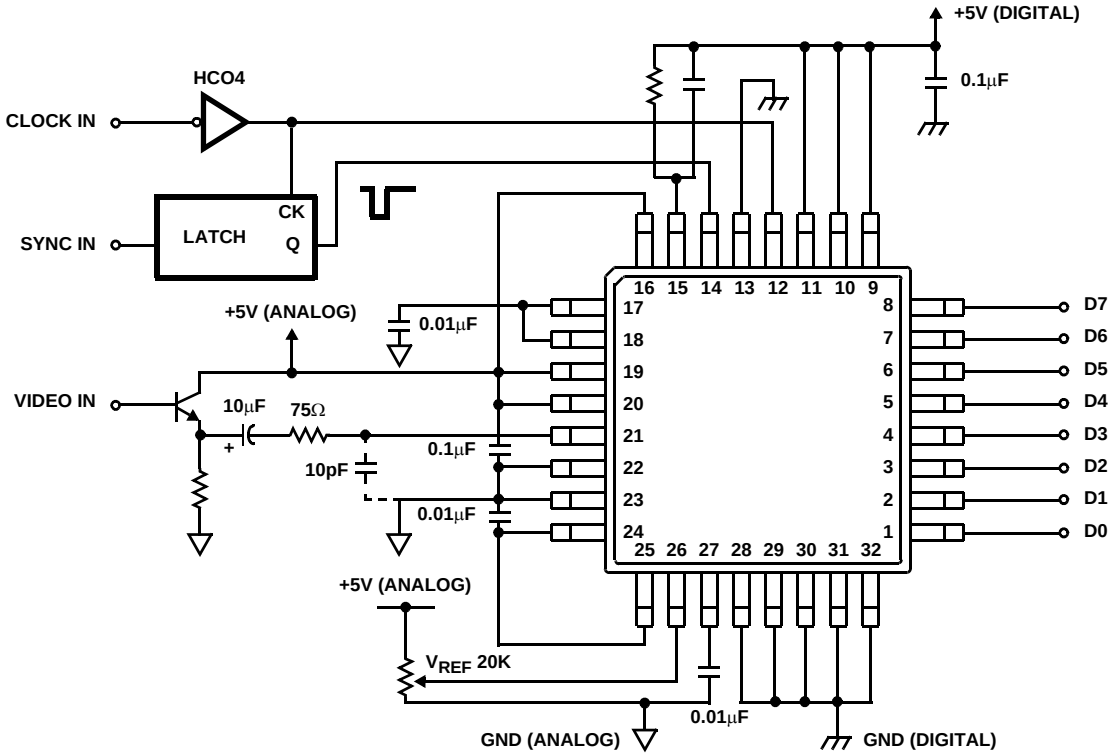


FIGURE 6. PEDESTAL CLAMP IS EXECUTED BY SYNC PULSE (SELF BIAS USED)

Typical Application Circuits (Continued)

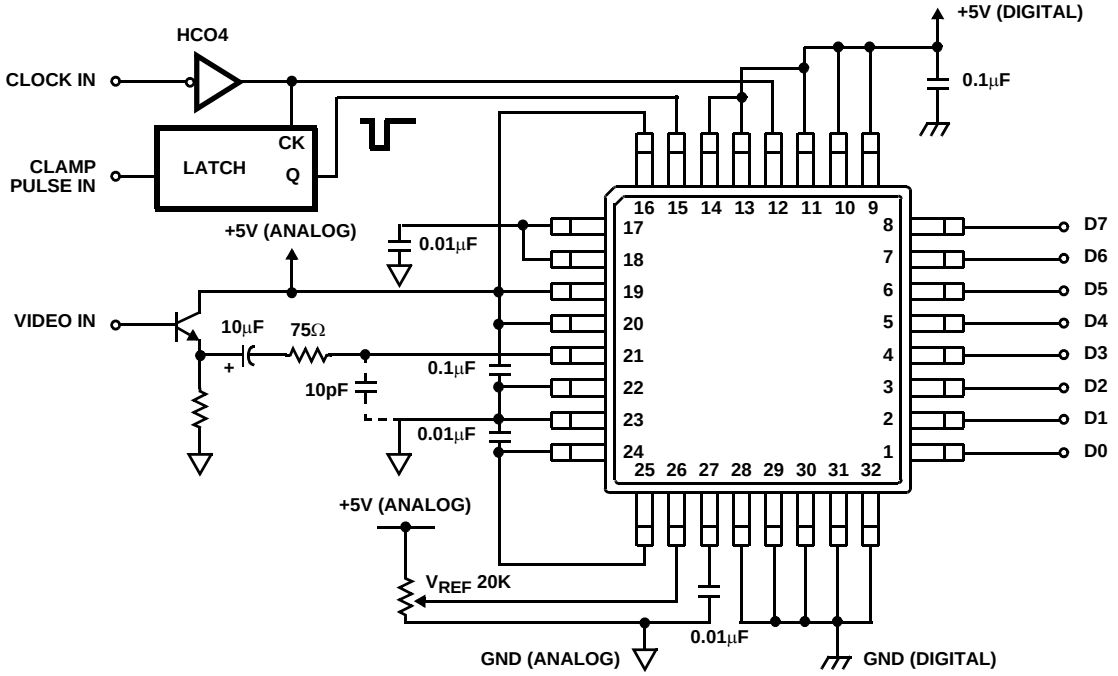


FIGURE 7. CLAMP PULSE IS DIRECTLY INPUT (SELF BIAS USED)

Test Circuits

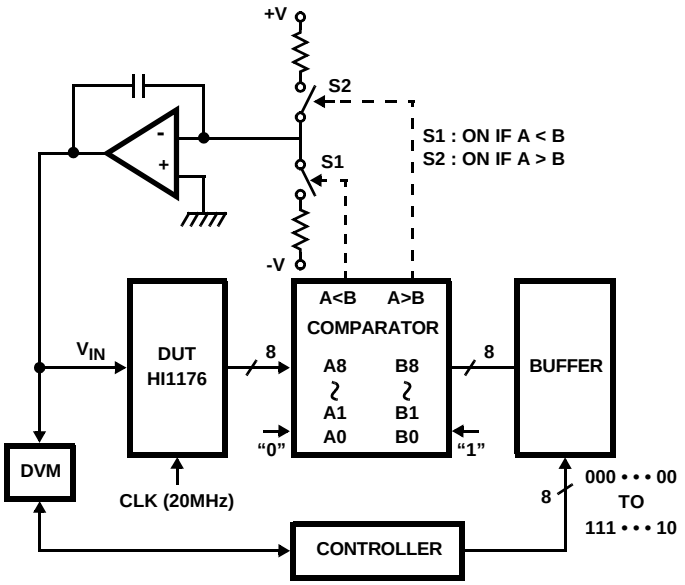


FIGURE 8. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

Test Circuits

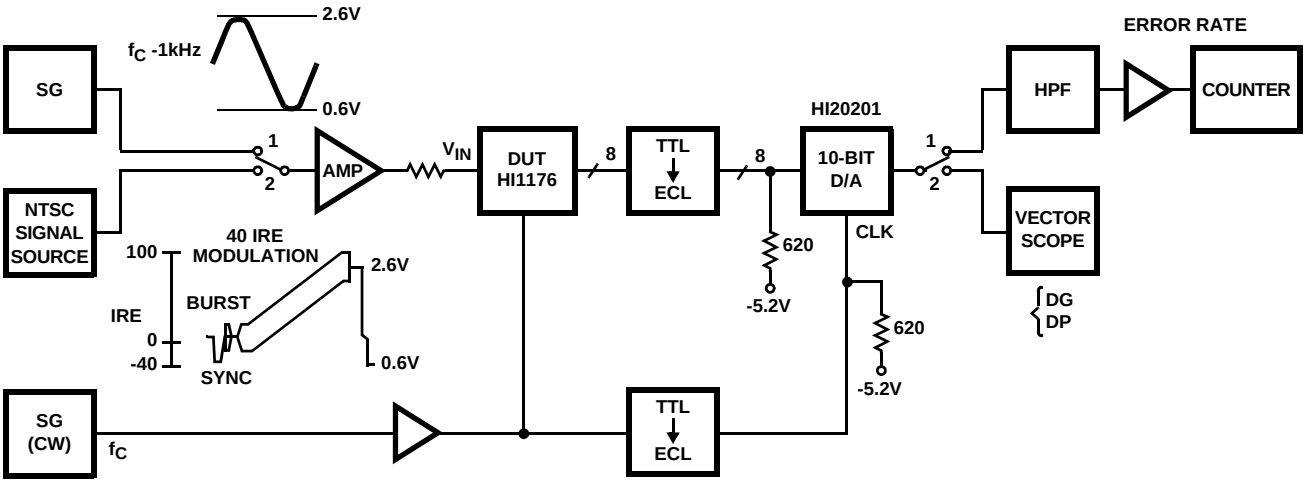


FIGURE 9. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

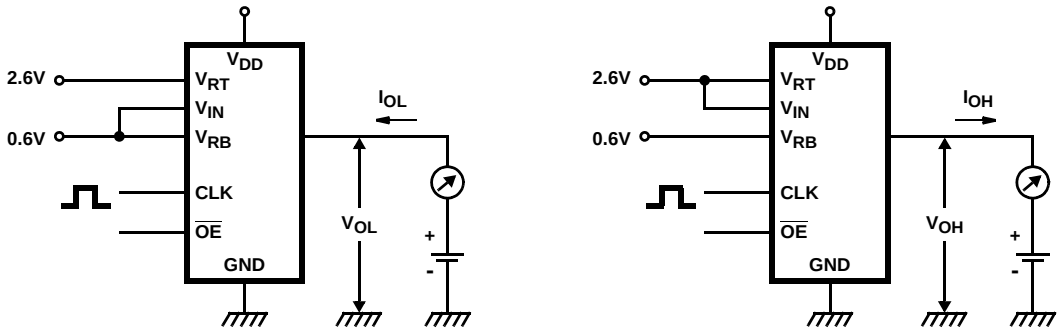


FIGURE 10. DIGITAL OUTPUT CURRENT TEST CIRCUIT