ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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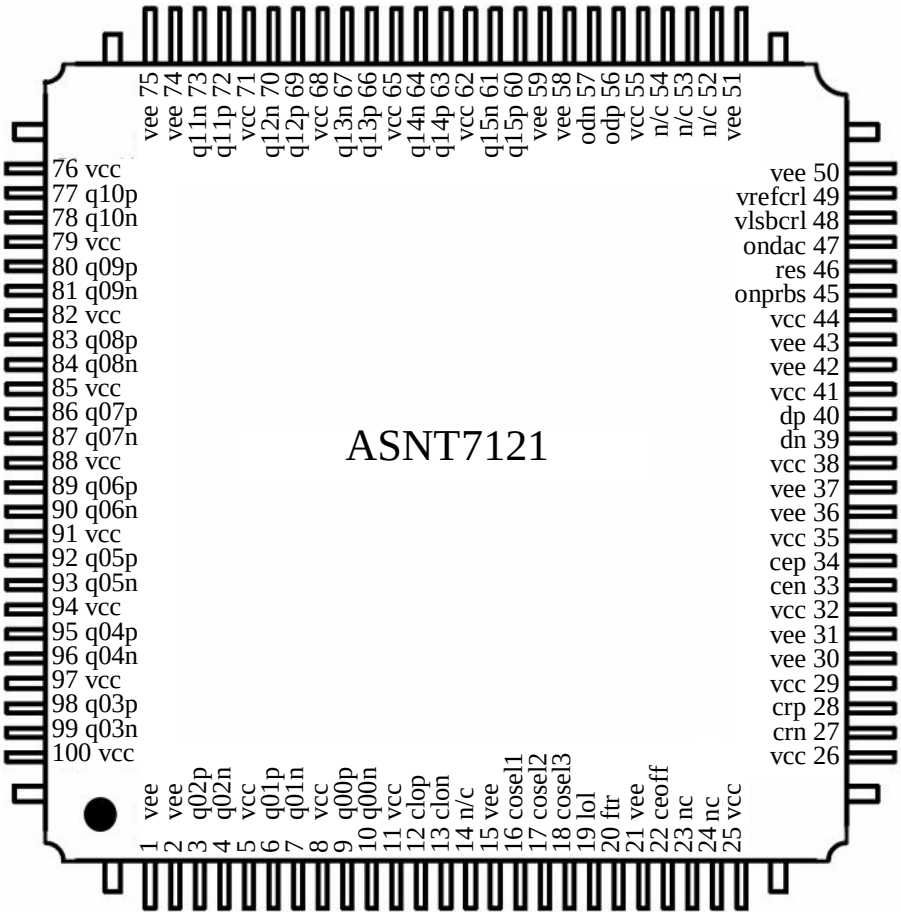
ASNT7121-KMA
15*GS/s*, 4-bit Flash Analog-to-Digital Converter with PRBS

- 20*GHz* analog input bandwidth
- Selectable clocking mode: external high-speed clock or internal PLL with external reference clock
- Broadband operation in external clocking mode: DC-15*GS/s*
- On-chip PLL with a central frequency of 10*GHz*
- Optional external preset of the internal clock divider
- Internal demultiplexer 4-to-16 for the output data rate reduction
- Selectable on-chip PRBS 2^7-1 generator for output interface alignment
- Differential CML input clock buffer and linear input data buffer
- Proprietary low-power LVDS output interface
- Selectable output clock frequency and polarity
- Selectable on-chip digital-to-analog converter for self-testing
- Single +3.5*V* power supply
- Power consumption: 2.8*W*
- Custom 100-pin metal-ceramic package



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DESCRIPTION

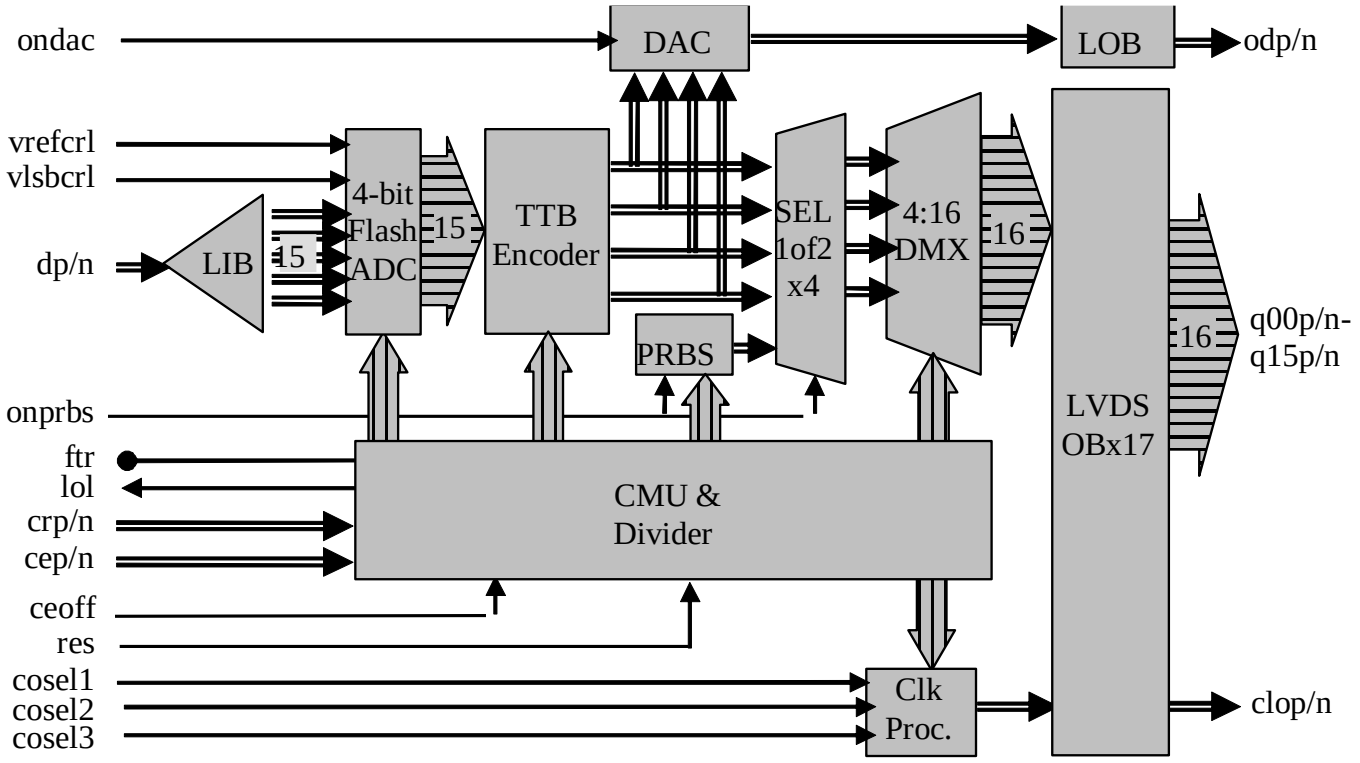

Fig. 1. Functional Block Diagram

The ASNT7121-KMA is a 4-bit flash analog to digital converter (ADC) featuring high sampling rate and wide analog front-end bandwidth. The ADC system shown in Fig. 1 includes a linear input buffer (LIB) with a tree architecture and a CML-type input interface with internal 50*Ohm* single-ended terminations to vcc. The buffer delivers 15 matching copies of the input analog data signal dp/dn to the 4-bit flash ADC. The ADC creates 15 samples of the input data in thermometer code, which are then converted by a thermometer-to-binary encoder (TTB Encoder) into 4-bit binary words with a data rate *f*. The encoded data is demultiplexed into 16-bit wide words with a data rate *f*/4 and sent to the output through 16 low-power LVDS buffers. The output parallel interface can be aligned using a selectable PRBS generator that substitutes the encoded data with a test pattern. An optional digital-to-analog converter (DAC) can be used for the control of the ADC's operation.

All operations are synchronized by the internal clock multiplication unit (CMU) based on a PLL (phase-locked loop) with an integrated divider. The block can operate in two different modes: clock multiplication (PLL is on) and clock division (PLL is off). In both modes, the divider generates internal clock signals divided by 2, 4, 8, and 16. The generated clocks divided by 4, 8, and 16 are sent to the LVDS output clop/clon through a clock processor that selects the desired speed (cosel1, cosel2 control signals) and polarity (cosel3 control signal) of the output clock. In the CMU's second operational mode, the divider can be preset by external signal res to allow synchronization of parallel-connected ADCs. A PLL lock control output lol is also provided.

The part operates from a single +3.5*V* power supply. All external control signals are compatible with the 2.5*V* CMOS interface.

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Linear Input Buffer (LIB)

The system includes a linear input buffer (LIB) with a tree-type architecture that delivers 15 matching copies of the wide-band input differential analog data signal dp/dn to the 4-bit flash section. Symmetry is closely followed in both schematic and layout to ensure minimal aperture jitter.

Clock Multiplication Unit (CMU) & Divider

The PLL-based CMU with external loop filter connected to the pin ftr as shown in Fig. 2 can operate in two different modes. In the first "clock multiplication" mode (ceoff="1"), the CMU multiplies the external reference clock crp/crn with the speed of *f*/16 by means of a PLL with a central frequency of *f* and a wide tuning range of the internal VCO (voltage-controlled oscillator). The generated clock is processed by the divider in order to generate internal clock signals divided by 2, 4, 8, and 16.

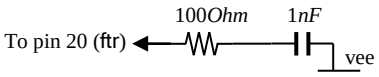

Fig. 2. Recommended External Loop Filter Schematic

In the second "clock division" mode (ceoff="0"), the PLL is disabled and the internal clocks are generated from the external high-speed clock cep/cen. To align multiple ADCs in parallel, the divider should be preset by the active-high CMOS control signal res.

HS External Clock Input Buffer

The high-speed external clock input buffer can accept high-speed clock signals at its differential CML input port cep/cen. It can also accept a single-ended signal with a threshold voltage applied to the unused pin. HS CIB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended termination of 50*Ohm* to vcc for each input line.

LS Reference Clock Input Buffer

The low-speed reference clock input buffer is a proprietary LVDS buffer with internal 100*Ohm* differential termination between its inputs crp/crn. The buffer exceeds the requirements of standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. It is designed to accept differential signals with amplitudes above 100*mV* peak-to-peak (p-p), a wide range of DC common mode voltages, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*.

4-bit Flash Analog to Digital Converter (ADC) with Encoder

This block samples the incoming analog data with the clock signal provided by the CMU in order to generate a 4-bit output digital signal (Bit 0 – Bit 3) with MSB corresponding to Bit 3. The threshold voltages (V_{th}) of the ADS can be adjusted through analog signals vrefcrl and vlsbcrl as shown in Table 1.

Table 1. Threshold Adjustment Options

Control signal		Adjusted value	
Name	**Range**	**Name**	**Range**
vrefcrl	vcc-1.0*V* -> vcc	$V_{th\ 15}$	vcc -0.5*V* -> vcc -0.15*V*
vlsbcrl	vcc -0.6*V* -> vcc -0.2*V*	$V_{th\ (X+1)} - V_{th\ X}$	550*uV* -> 55*mV*

As can be seen, vrefcrl shifts the DC levels of all the threshold voltages simultaneously by the same amount while vlsbcrl alters the voltage range of the least significant bit (LSB).

If no external voltages are applied to vrefcrl and vlsbcrl, it is recommended that both pins are AC-terminated by 50*Ohm* to vee through a DC block!

Demultiplexer (4:16 DMX)

This block deserializes the 4-bit words from the ADC into 16-bit output words as shown in Table 2.

Table 2. Demultiplexer Bit Order

Serialized input words	First				Second				Third				Fourth			
ADC bits (3 is MSB)	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
DMX output bits	00	04	08	12	01	05	09	13	02	06	10	14	03	07	11	15

PRBS Generator (PRBS) and Selector (SEL 1of2x4)

The on-chip selectable generator provides a full 127-bit long pseudo-random binary sequence (PRBS) signal according to the polynomial ($x^7 + x^6 + 1$), where x^D represents a delay of D clock cycles. This is implemented as a linear feedback shift register (LSFR) in which the outputs of the seventh and sixth flip-flops are combined together by an XOR function and provided as an input to the first flip-flop of the register. The block is activated by the external 2.5*V* CMOS signal onprbs (onprbs="0" – default state – PRBS generator off, onprbs="1" – PRBS generator on). The same signal controls the selector SEL1of2x4 in such a way that the following demultiplexer receives either the PRBS signal when the generator is activated or the encoded signal from the ADC if the generator is disabled.

Clock Processor (Clk Proc)

To increase the adaptability of the designed ADC, a clock processor that provides a low-speed output clock signal with the options specified in Table 3, is included.

Table 3. Output Clock Options

External control signals			**Output clock signal**	
cosel1	cosel2	cosel3	**Speed**	**Inversion**
1	1	1	c4	Yes
1	1	0	c4	No
0	1	1	c8	Yes
0	1	0	c8	No
x	0	1	c16	Yes
x	0	0	c16	No

Digital to Analog Converter (DAC)

A DAC block is included to perform a quick test of the ADC's functionality. When activated by the external control signal (ondac="1"), it converts the digital data into a step-wise copy of the input signal that is sent to the output odp/odn through a linear differential output buffer. The circuit is not consuming any power when disabled (ondac="0").

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LVDS Output Buffers

The 16-bit differential digital data words q00p/q00n to q15p/q15n are delivered to the output through an array of proprietary low power LVDS buffers. The low speed differential clock clop/clon also utilizes a similar LVDS output buffer. The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

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TERMINAL FUNCTIONS

Pin #	Pin name	Pin type	Pin #	Pin name	Pin type	Pin #	Pin name	Pin type
1	vee	GND	35	vcc	3.5V	69	q12p	LVDS outputs
2	vee	GND	36	vee	GND	70	q12n	
3	q02p	LVDS outputs	37	vee	GND	71	vcc	3.5V
4	q02n		38	vcc	3.5V	72	q11p	LVDS outputs
5	vcc	3.5V	39	dn	HS CML inputs	73	q11n	
6	q01p	LVDS outputs	40	dp		74	vee	GND
7	q01n		41	vcc	3.5V	75	vee	GND
8	vcc	3.5V	42	vee	GND	76	vcc	3.5V
9	q00p	LVDS outputs	43	vee	GND	77	q10p	LVDS outputs
10	q00n		44	vcc	3.5V	78	q10n	
11	vcc	3.5V	45	onprbs	CMOS input	79	vcc	3.5V
12	clop	LVDS outputs	46	res	CMOS input	80	q09p	LVDS outputs
13	clon		47	ondac	CMOS input	81	q09n	
14	n/c		48	vlsbcrl	Control voltages	82	vcc	3.5V
15	vee	GND	49	vrefcrl		83	q08p	LVDS outputs
16	cosel1	CMOS input	50	vee	GND	84	q08n	
17	cosel2	CMOS input	51	vee	GND	85	vcc	3.5V
18	cosel3	CMOS input	52	n/c		86	q07p	LVDS outputs
19	lol	Control output	53	n/c		87	q07n	
20	ftr	Filter	54	n/c		88	vcc	3.5V
21	vee	GND	55	vcc	3.5V	89	q06p	LVDS outputs
22	ceoff	CMOS input	56	odp	LS CML outputs	90	q06n	
23	n/c		57	odn		91	vcc	3.5V
24	n/c		58	vee	GND	92	q05p	LVDS outputs
25	vcc	3.5V	59	vee	GND	93	q05n	
26	vcc	3.5V	60	q15p	LVDS outputs	94	vcc	3.5V
27	crn	LVDS inputs	61	q15n		95	q04p	LVDS outputs
28	crp		62	vcc	3.5V	96	q04n	
29	vcc	3.5V	63	q14p	LVDS outputs	97	vcc	3.5V
30	vee	GND	64	q14n		98	q03p	LVDS outputs
31	vee	GND	65	vcc	3.5V	99	q03n	
32	vcc	3.5V	66	q13p	LVDS outputs	100	vcc	3.5V
33	cen	HS CML inputs	67	q13n				
34	cep		68	vcc	3.5V			

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	3. 4	3.5	3.6	*V*	±3%
vee		0.0		*V*	External ground
*I*vcc		815/800		*mA*	With PRBS enabled/disabled
Power consumption		2.85/2.80		*W*	With PRBS enabled/disabled
Junction temperature	-25	50	125	*°C*	
Analog Input Data (dp/dn)					
Bandwidth	0.0		20	*GHz*	
CM Level	vcc-0.8		vcc	*V*	Must match for both inputs
Linearity range		±110		*mV*	Differential or SE, p-p
HS Input Clock (cep/cen)					
Frequency	DC		15	*GHz*	
Swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty Cycle	40	50	60	*%*	
LS Reference Input Clock (crp/crn)					
Frequency	560		688	*MHz*	1/16 of VCO frequency
CM Level	0.2		vcc	*V*	
Voltage Swing	100		800	*mV*	Differential
Duty Cycle	40	50	60	*%*	
Output Data (q00p/q00n to q15p/q15n)					
Data Rate	DC		3.75	*Gbps*	
CM Level		1.2		*V*	Nominal for LVDS interface
Amplitude range	250		350	*mV*	
Rise/Fall Times		TBD		*ps*	20%-80%
LS Output Clock (clop/clon)					
Frequency	*f*/4	*f*/8	*f*/16	*GHz*	Selectable. Here *f* is the PLL or HS input clock frequency
CM Level		1.2		*V*	Nominal for LVDS interface
Amplitude range	250		350	*V*	
Jitter		TBD		*ps*	
Duty Cycle		50		*%*	
DAC Output (odp/odn)					
Voltage Swing	250		350	*mV*	Single-ended. p-p
CM Level		vcc-(voltage swing)/2		*V*	
Analog Control Signals (vrfcrl, vlsbcrl)					
Voltage range				*V*	see Table 1
CMOS Control Signals (cosel1/2/3, ceoff, res, ondac, onprbs)					
Logic "1" level	vee+2.3		vee+2.5	*V*	
Logic "0" level			vee+0.2	*V*	
Frequency			3.5	*GHz*	

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ELECTRICAL SPECIFICATIONS

Parameter	Conditions	Min	Typical	Max	Units
ENOB (5GS/s)	fin = 3.9GHz		3.39		*bits*
ENOB (10GS/s)	fin = 7.8GHz		3.23		*bits*
SFDR (5GS/s)	fin = 3.9GHz		30.13		*dBFS*
SFDR (10GS/s)	fin = 7.8GHz		28.78		*dBFS*
SINAD (5GS/s)	fin = 3.9GHz		-22.15		*dB*
SINAD (10GS/s)	fin = 7.8GHz		-21.19		*dB*
DNL		-0.2		0.2	*lsbs*
INL		-0.2		0.2	*lsbs*

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings presented in Table 4 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (vee).

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		4.0	*V*
Power Consumption		3.0	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Case Temperature		+100	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

PACKAGE INFORMATION

The chip die is housed in a custom 100-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is power for a positive supply.

The part's identification label is ASNT7121-KMA. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

Thermal resistance of junction to case bottom pad is 4°*C/W*.

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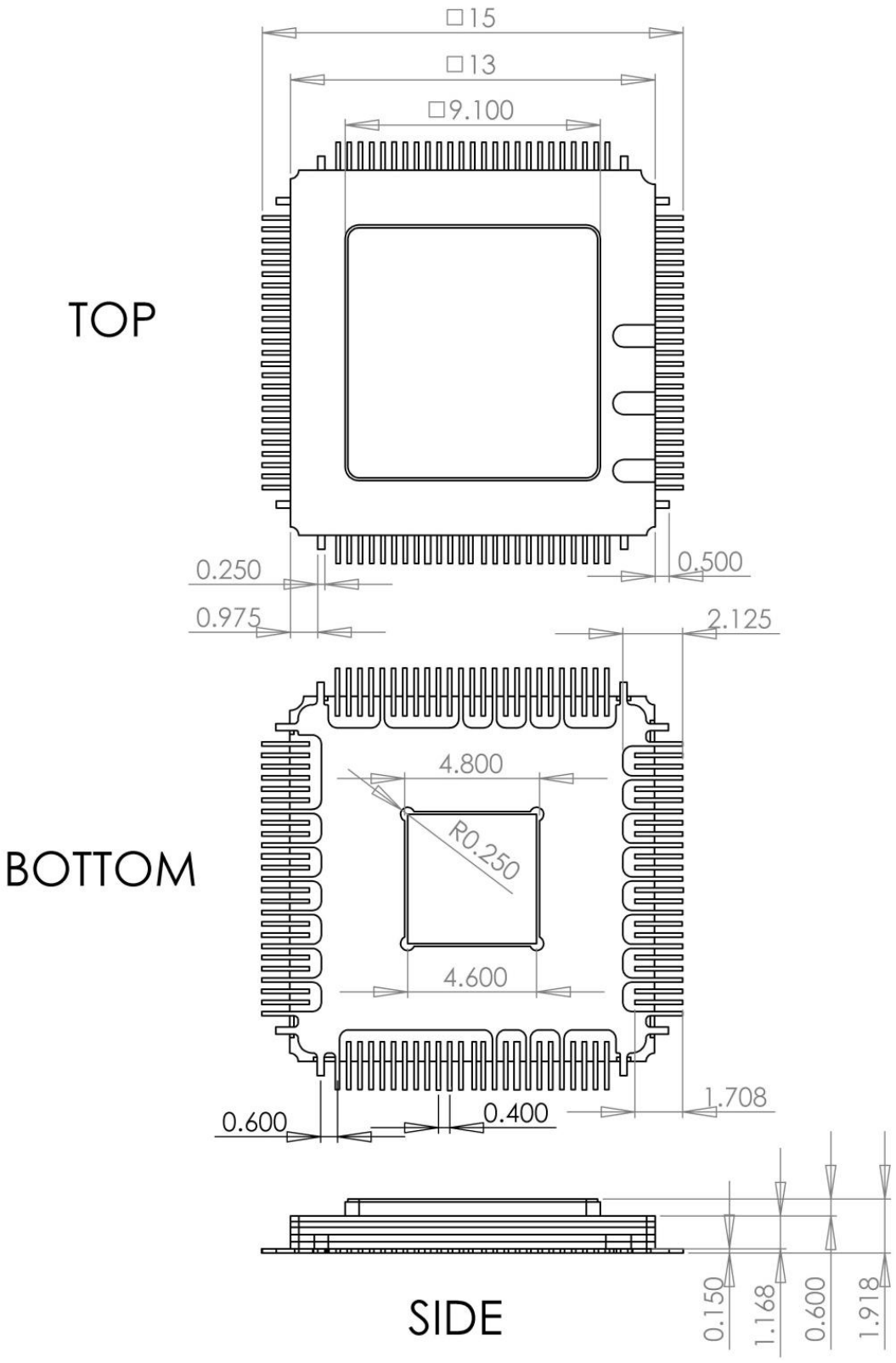

Fig. 3. CQFP 100-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.5.2	02-2020	Updated Package Information
1.4.2	07-2019	Updated Letterhead
1.4.1	09-2015	Clock Multiplication Unit (CMU) & Divider section edited
1.3.1	08-2015	Corrected PRBS polynomial Removed prbsres function (Pinout diagram, block diagram, description, Terminal Functions table, Electrical Characteristics table) Removed cpcsel function (Pinout diagram, block diagram, description, Terminal Functions table, Electrical Characteristics table)
1.2.1	08-2015	Updated Electrical Specifications
1.1.1	07-2015	Updated title Revised Electrical Characteristics Revised Absolute Maximum Ratings section
1.0.1	07-2015	Added Electrical Specifications table Revised package information section
1.0.0	09-2014	Preliminary release