

### Features

- Differential Linearity Error  $\pm 0.5$  LSB or Less
- Integral Linearity Error  $\pm 0.5$  LSB or Less
- Built-In Integral Linearity Compensation Circuit
- High-Speed Operation with Maximum Conversion Rate (Min) ..... 75 MSPS
- Low Input Capacitance (Typ) ..... 17pF
- Wide Analog Input Bandwidth (Min for Full Scale Input) 150MHz
- Single Power Supply ..... -5.2V
- Low Power Consumption (Typ) ..... 580mW
- Low Error Rate
- Operable at 50% Clock Duty Cycle
- Capable of Driving 50 $\Omega$  Loads
- Direct Replacement for CXA1386

### Applications

- Video Digitizing
- RGB Graphics Processing
- HDTV (High Definition TV)
- Radar Systems
- Communication Systems
- Direct RF Down-Conversion
- Digital Oscilloscopes

### Description

The HI1386 is an 8-bit, high-speed flash analog-to-digital converter IC capable of digitizing analog signals at a maximum rate of 75 MSPS. The digital I/O levels of this A/D converter are compatible with ECL 100K/10KH/10K.

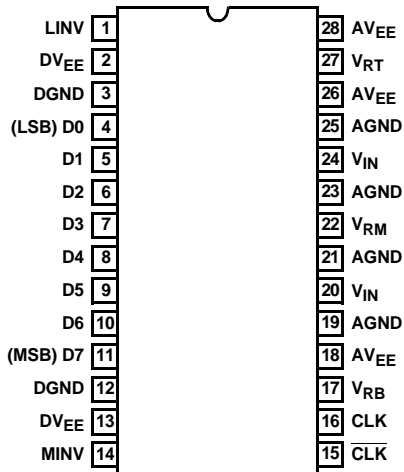
The HI1386 is available in the commercial and industrial temperature range and is supplied in 28 lead plastic DIP and 44 lead ceramic LCC packages.

### Part Number Information

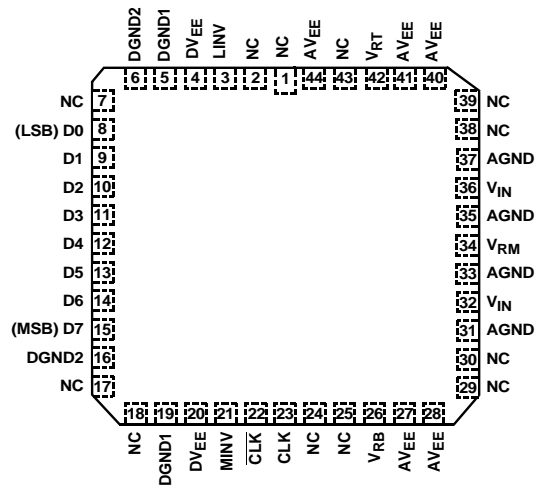
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE    | PKG. NO. |
|-------------|------------------|------------|----------|
| HI1386JCP   | -20 to 75        | 28 Ld PDIP | E28.6A-S |
| HI1386AIL   | -20 to 100       | 44 Ld CLCC | J44.B    |

### Pinouts

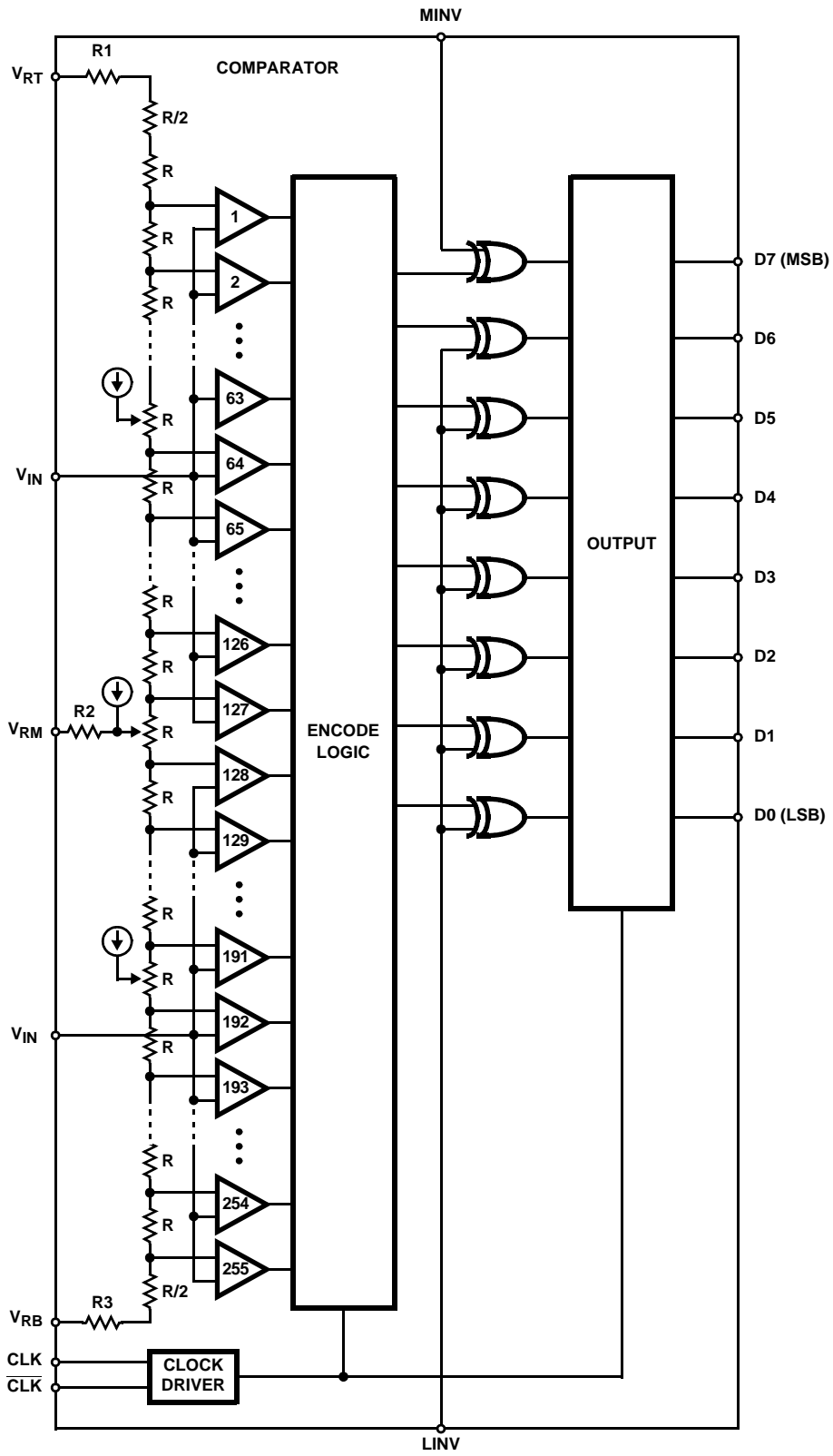
HI1386 (PDIP)  
TOP VIEW



HI1386 (CLCC)  
TOP VIEW



Functional Block Diagram



**Pin Descriptions**

| PIN NUMBER     |                    | SYMBOL                  | I/O | STANDARD VOLTAGE LEVEL  | EQUIVALENT CIRCUIT | DESCRIPTION  |
|----------------|--------------------|-------------------------|-----|---|--------------------|--|
| DIP            | LCC                |                         |     |   |                    |  |
| 19, 21, 23, 25 | 31, 33, 35, 37     | AGND                    | -   | 0V  |                    | Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND, DGND1, and DGND2.  |
| 18, 26, 28     | 27, 28, 40, 41, 44 | AV <sub>EE</sub>        | -   | -5.2V   |                    | Analog V <sub>EE</sub> -5.2V (Typ). Internally connected to DV <sub>EE</sub> (Resistance: 4Ω to 6Ω). Bypass with 0.1μF to AGND.  |
| 16             | 23                 | CLK                     | I   | ECL   |                    | CLK Input.   |
| 15             | 22                 | $\overline{\text{CLK}}$ |     |   |                    | Input Complementary to CLK. When open pulled down to -1.3V. Device is operable without $\overline{\text{CLK}}$ input, but use of complementary inputs of CLK and $\overline{\text{CLK}}$ is recommended to obtain stable high speed operation. |
| 3, 12          | -                  | DGND                    | -   | 0V  |                    | Digital GND (used for internal circuits and output transistors).   |
| -              | 5, 19              | DGND1                   | -   | 0V  |                    | Digital GND (used for internal circuits and output transistors).   |
| -              | 6, 16              | DGND2                   | -   | 0V  |                    | Digital GND (used for output buffers).   |
| 2, 13          | 4, 20              | DV <sub>EE</sub>        | -   | -5.2V   |                    | Digital V <sub>EE</sub> . Internally connected to AV <sub>EE</sub> (resistance: 4Ω to 6Ω). Bypass with 0.1μF to DGND   |
| 4              | 8                  | D0                      | O   | ECL   |                    | LSB of Data Outputs. External pull-down resistor is required.  |
| 5              | 9                  | D1                      |     |   |                    | Data Outputs. External pull-down resistors are required.   |
| 6              | 10                 | D2                      |     |   |                    |  |
| 7              | 11                 | D3                      |     |   |                    |  |
| 8              | 12                 | D4                      |     |   |                    |  |
| 9              | 13                 | D5                      |     |   |                    |  |
| 10             | 14                 | D6                      |     |   |                    |  |
| 11             | 15                 | D7                      |     | MSB of Data Outputs. External pull-down resistor is required. |                    |  |

**Pin Descriptions** (Continued)

| PIN NUMBER |        | SYMBOL   | I/O | STANDARD VOLTAGE LEVEL | EQUIVALENT CIRCUIT | DESCRIPTION  |
|------------|--------|----------|-----|------------------------|--------------------|--|
| DIP        | LCC    |          |     |                        |                    |  |
| 1          | 3      | LINV     | I   | ECL                    |                    | Input Pin for D0 (LSB) to D6 Output Polarity Inversion (see A/D Output Code Table). Pulled low when left open.                                 |
| 14         | 21     | MINV     | I   | ECL                    |                    | Input Pin for D7 (MSB) Output Polarity Inversion (see A/D Output Code Table). Pulled low when left open.                                       |
| 20, 24     | 32, 36 | $V_{IN}$ | I   | $V_{RT}$ to $V_{RB}$   |                    | Analog Input Pins. These two pins must be connected externally, since they are not internally connected. See Application Note for precautions. |
| 17         | 26     | $V_{RB}$ | I   | -2V                    |                    | Reference Voltage (Bottom). Typically -2V. Bypass with a 0.1 $\mu$ F and 10 $\mu$ F to AGND.   |
| 22         | 34     | $V_{RM}$ | I   | $V_{RB}/2$             |                    | Reference Voltage Mid Point. Can be used as a pin for integral linearity compensation.   |
| 27         | 42     | $V_{RT}$ | I   | 0V                     |                    | Reference Voltage (Top) Typically 0V.  |

**Absolute Maximum Ratings**  $T_A = 25^\circ\text{C}$

|   |                |
|---|----------------|
| Supply Voltage ( $V_{EE}$ , $DV_{EE}$ )   | -7V to +0.5V   |
| Analog Input Voltage ( $V_{IN}$ )         | -2.7V to +0.5V |
| Reference Input Voltage                   |                |
| $V_{RT}$ , $V_{RB}$ , $V_{RM}$            | -2.7V to +0.5V |
| $ V_{RT} - V_{RB} $                       | 2.5V           |
| Digital Input Voltage                     |                |
| CLK, $\overline{\text{CLK}}$ , MINV, LINV | -4V to +0.5V   |
| $ \text{CLK} - \overline{\text{CLK}} $    | 2.7V           |
| $V_{RM}$ Pin Input Current ( $I_{VRM}$ )  | -3mA to +3mA   |
| Digital Output Current ( $ID0$ to $ID7$ ) | -30mA to 0mA   |

**Operating Conditions**

|                             |                 |
|-----------------------------|-----------------|
| Temperature Ranges (Note 4) |                 |
| PDIP Package ( $T_A$ )      | -20°C to 75°C   |
| CLCC Package ( $T_C$ )      | -20°C to 100°C  |
| Supply Voltage              |                 |
| $V_{EE}$ , $DV_{EE}$        | -5.5V to -4.95V |
| $V_{EE} - DV_{EE}$          | -0.05V to 0.05V |
| AGND - DGND                 | -0.05V to 0.05V |
| Reference Input Voltage     |                 |
| $V_{RT}$                    | -0.1V to 0.1V   |
| $V_{RB}$                    | -2.2V to -1.8V  |

**Thermal Information**

|   |                    |                    |
|---|--------------------|--------------------|
| Thermal Resistance (Typical, Note 1)            | $\theta_{JA}$ °C/W | $\theta_{JC}$ °C/W |
| PDIP Package                                    | 58                 | N/A                |
| CLCC Package                                    | 45                 | 11                 |
| Maximum Junction Temperature                    |                    |                    |
| CLCC Package                                    |                    | 175°C              |
| PDIP Package                                    |                    | 150°C              |
| Maximum Storage Temperature Range ( $T_{STG}$ ) |                    | -65°C to 150°C     |
| Maximum Lead Temperature (Soldering 10s)        |                    | 300°C              |

|                                |                      |
|--------------------------------|----------------------|
| Analog Input Voltage, $V_{IN}$ | $V_{RB}$ to $V_{RT}$ |
| Pulse Width of Clock           |                      |
| $t_{PW1}$                      | 6.6ns (Min)          |
| $t_{PW0}$                      | 6.6ns (Min)          |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $T_A = 25^\circ\text{C}$ ,  $V_{EE} = DV_{EE} = -5.2\text{V}$ ,  $V_{RT} = 0\text{V}$ ,  $V_{RB} = -2\text{V}$  (Note 1)

| PARAMETER   | TEST CONDITIONS   | MIN | TYP       | MAX       | UNIT            |
|---|---|-----|-----------|-----------|-----------------|
| <b>SYSTEM PERFORMANCE</b>   |   |     |           |           |                 |
| Resolution  |   | -   | 8         | -         | Bits            |
| Integral Linearity Error, INL   | $f_C = 75\text{MHz}$  | -   | $\pm 0.3$ | $\pm 0.5$ | LSB             |
| Differential Linearity Error, DNL   | $f_C = 75\text{MHz}$  | -   | $\pm 0.3$ | $\pm 0.5$ | LSB             |
| <b>DYNAMIC CHARACTERISTICS</b>  |   |     |           |           |                 |
| Signal to Noise and Distortion Ratio, SINAD<br>= $\frac{\text{RMS Signal}}{\text{RMS Noise} + \text{Distortion}}$ | Input = 1MHz, Full Scale<br>$f_C = 75\text{MHz}$                      | -   | 46        | -         | dB              |
|   | Input = 18.75MHz, Full Scale<br>$f_C = 75\text{MHz}$                  | -   | 40        | -         | dB              |
| Error Rate  | Input = 18.749MHz, Full Scale<br>Error > 16 LSB, $f_C = 75\text{MHz}$ | -   | -         | $10^{-9}$ | TPS<br>(Note 2) |
| Differential Gain Error, DG   | NTSC 40 IRE Mod. Ramp,<br>$f_C = 75\text{MSPS}$                       | -   | 1.0       | -         | %               |
| Differential Phase Error, DP  |   | -   | 0.5       | -         | Degree          |
| Maximum Conversion Rate, $f_C$  | Error Rate of $10^{-9}$ TPS (Note 2)                                  | 75  | -         | -         | MSPS            |
| Aperture Jitter, $t_{AJ}$   |   | -   | 10        | -         | ps              |
| Sampling Delay, $t_{DS}$  |   | -   | 3.0       | -         | ns              |
| <b>ANALOG INPUT</b>   |   |     |           |           |                 |
| Input Bandwidth   | $V_{IN} = 2V_{P-P}$ (-3dB)  | 150 | -         | -         | MHz             |
| Analog Input Capacitance, $C_{IN}$  | $V_{IN} = 1\text{V} + 0.07V_{RMS}$                                    | -   | 17        | -         | pF              |
| Analog Input Resistance, $R_{IN}$   |   | -   | 390       | -         | k $\Omega$      |
| Input Bias Current, $I_{IN}$  | $V_{IN} = -1\text{V}$   | -   | -         | 200       | $\mu\text{A}$   |
| <b>REFERENCE INPUTS</b>   |   |     |           |           |                 |
| Reference Resistance, $R_{REF}$   |   | 75  | 110       | 155       | $\Omega$        |

**Electrical Specifications**  $T_A = 25^{\circ}\text{C}$ ,  $AV_{EE} = DV_{EE} = -5.2\text{V}$ ,  $V_{RT} = 0\text{V}$ ,  $V_{RB} = -2\text{V}$  (Note 1) (Continued)

| PARAMETER                           | TEST CONDITIONS                             | MIN   | TYP  | MAX   | UNIT          |
|-------------------------------------|---|-------|------|-------|---------------|
| Offset Voltage                      |   |       |      |       |               |
| $E_{OT}$                            | $V_{RT}$                                    | 8     | 18   | 32    | mV            |
| $E_{OB}$                            | $V_{RB}$                                    | 0     | 10   | 24    | mV            |
| <b>DIGITAL INPUTS</b>               |   |       |      |       |               |
| Logic H Level, $V_{IH}$             |   | -1.13 | -    | -     | V             |
| Logic L Level, $V_{IL}$             |   | -     | -    | -1.50 | V             |
| Logic H Current, $I_{IH}$           | -0.8V is Applied to Input                   | 0     | -    | 50    | $\mu\text{A}$ |
| Logic L Current, $I_{IL}$           | -1.6V is Applied to Input                   | -50   | -    | 50    | $\mu\text{A}$ |
| Input Capacitance                   |   | -     | 7    | -     | pF            |
| <b>DIGITAL OUTPUTS</b>              |   |       |      |       |               |
| Logic H Level, $V_{OH}$             | $R_L = 620\Omega$ to $DV_{EE}$              | -1.03 | -    | -     | V             |
| Logic L Level, $V_{OL}$             | $R_L = 620\Omega$ to $DV_{EE}$              | -     | -    | -1.62 | V             |
| <b>TIMING CHARACTERISTICS</b>       |   |       |      |       |               |
| H Pulse Width of Clock, $t_{PW1}$   |   | 6.6   | -    | -     | ns            |
| L Pulse Width of Clock, $t_{PW0}$   |   | 6.6   | -    | -     | ns            |
| Output Rise Time, $t_r$             | $R_L = 620\Omega$ to $DV_{EE}$ , 20% to 80% | -     | 0.9  | -     | ns            |
| Output Fall Time, $t_f$             | $R_L = 620\Omega$ to $DV_{EE}$ , 20% to 80% | -     | 2.1  | -     | ns            |
| Output Delay, $t_{OD}$              |   | 4.0   | 6.5  | 9.0   | ns            |
| <b>POWER SUPPLY CHARACTERISTICS</b> |   |       |      |       |               |
| Supply Current, $I_{EE}$            |   | -150  | -104 | -     | mA            |
| Power Consumption, $P_D$            | Note 3                                      | -     | 580  | -     | mW            |

NOTES:

- Electrical Specifications guaranteed within stated operating conditions.
- TPS: Times Per Sample.
- $$P_D = I_{EE} \cdot V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$$
- $T_A$  specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed.

**Timing Diagram**

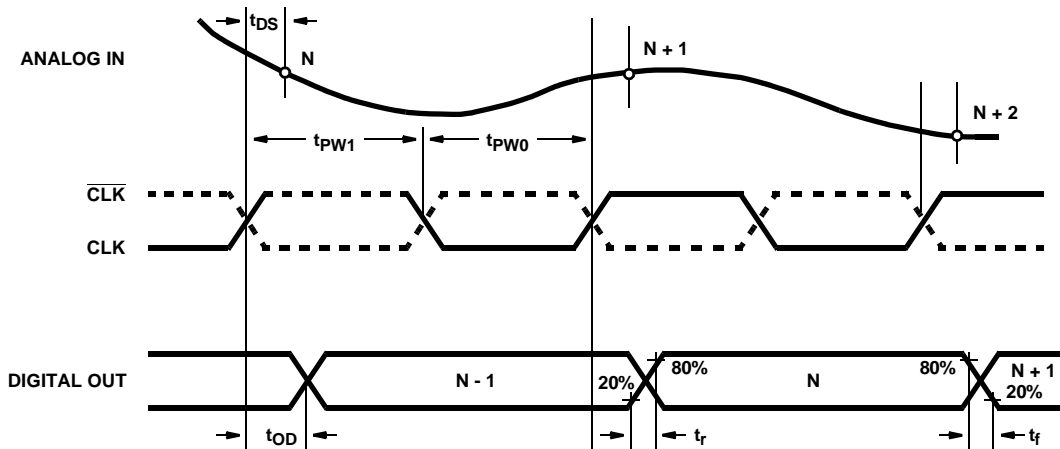


FIGURE 1.

# HI1386

A/D OUTPUT CODE TABLE

| V <sub>IN</sub><br>(NOTE 1) | STEP | MINV 1<br>LINV 1 |            | 0<br>1     |            | 1<br>0     |            | 0<br>0     |            |
|-----------------------------|------|------------------|------------|------------|------------|------------|------------|------------|------------|
|                             |      | D7               | D0         | D7         | D0         | D7         | D0         | D7         | D0         |
| 0V                          | 0    | 000.....00       | 100.....00 | 011.....11 | 111.....11 | 000.....00 | 100.....00 | 011.....11 | 111.....11 |
|                             |      | 000.....00       | 100.....00 | 011.....11 | 111.....11 | 000.....00 | 100.....00 | 011.....11 | 111.....11 |
|                             |      | 000.....01       | 100.....01 | 011.....10 | 111.....10 | 000.....00 | 100.....00 | 011.....11 | 111.....11 |
| -1V                         | 127  | .....            | .....      | .....      | .....      | .....      | .....      | .....      | .....      |
|                             |      | .....            | .....      | .....      | .....      | .....      | .....      | .....      | .....      |
|                             |      | .....            | .....      | .....      | .....      | .....      | .....      | .....      | .....      |
|                             | 128  | 011.....11       | 111.....11 | 000.....00 | 100.....00 | 011.....11 | 111.....11 | 000.....00 | 100.....00 |
|                             | 128  | 100.....00       | 000.....00 | 111.....11 | 011.....11 | 100.....00 | 000.....00 | 111.....11 | 011.....11 |
| -2V                         | 254  | .....            | .....      | .....      | .....      | .....      | .....      | .....      | .....      |
|                             |      | .....            | .....      | .....      | .....      | .....      | .....      | .....      | .....      |
|                             |      | .....            | .....      | .....      | .....      | .....      | .....      | .....      | .....      |
| -2V                         | 255  | 111.....10       | 011.....10 | 100.....01 | 000.....01 | 111.....11 | 011.....11 | 100.....00 | 000.....00 |
|                             |      | 111.....11       | 011.....11 | 100.....00 | 000.....00 | 111.....11 | 011.....11 | 100.....00 | 000.....00 |

NOTE:

5. V<sub>RT</sub> = 0V, V<sub>RB</sub> = -2V.

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