

# CA3304, CA3304A

Complete Data Sheet available via web, Harris' home page: http://www.semi.harris.com or via Harris AnswerFAX, see Section 17

4-Bit, 25 MSPS, Flash A/D Converters

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**Features** 

•	CMOS/SOS	Low Power	with Video	Speed (Typ	) 25mW

- Parallel Conversion Technique
- Single Power Supply Voltage . . . . . . . . . 3V to 7.5V
- 25MHz Sampling Rate (40ns Conversion Time) at 5V Supply
- 4-Bit Latched Three-State Output with Overflow and Data Change Outputs
- 1/8 LSB Maximum Nonlinearity (A Version)
- · Inherent Resistance to Latch-Up Due to SOS Process
- . Bipolar Input Range with Optional Second Supply
- Wide Input Bandwidth (Typ) . . . . . . . . . . . . . . . . 25MHz

## Applications

- · High Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- · High Energy Physics Research
- General-Purpose Hybrid ADCs
- · Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision
- RSSI Circuits

## Description

The Harris CA3304 is a CMOS parallel (FLASH) analog-todigital converter designed for applications demanding both low-power consumption and high speed digitization. Digitizing at 25MHz, for example, requires only about 35mW.

The CA3304 operates over a wide, full-scale signal input voltage range of 0.5V up to the supply voltage. Power consumption is as low as 10mW, depending upon the clock frequency selected.

The intrinsic high conversion rate makes the CA3304 types ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3304s in series to increase the resolution of the conversion system. A series connection of two CA3304s may be used to produce a 5-bit, 25MHz converter. Operation of two CA3304s in parallel doubles the conversion speed (i.e., increases the sampling rate from 25MHz to 50MHz). A data change pin indicates when the present output differs from the previous, thus allowing compaction of data storage.

Sixteen paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3304. Fifteen comparators are required to quantize all input voltage levels in this 4-bit converter, and the additional comparator is required for the overflow bit.

# Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3304E	±0.25 LSB	25MHz (40ns)	-40 to 85	16 Ld PDIP	E16.3
CA3304AE	±0.125 LSB	25MHz (40ns)	-40 to 85	16 Ld PDIP	E16.3
CA3304M	±0.25 LSB	25MHz (40ns)	-40 to 85	16 Ld SOIC (W)	M16.3
CA3304AM	±0.125 LSB	25MHZ (40ns)	-40 to 85	16 Ld SOIC (W)	M16.3
CA3304D	±0.25 LSB	25MHz (40ns)	-55 to 125	16 Ld SBDIP	D16.3
CA3304AD	±0.125 LSB	25MHz (40ns)	-55 to 125	16 Ld SBDIP	D16.3

#### **Pinout**

#### CA3304 (SBDIP, PDIP, SOIC) TOP VIEW

