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ADC1175

8-Bit, 20MHz, 60mW A/D Converter

General Description

The ADC1175 is a low power, 20 Msps analog-to-digital converter that digitizes signals to 8 bits while consuming just 60 mW of power (typ). The ADC1175 uses a unique architecture that achieves 7.5 Effective Bits. Output formatting is straight binary coding.

The excellent DC and AC characteristics of this device, together with its low power consumption and +5V single supply operation, make it ideally suited for many video, imaging and communications applications, including use in portable equipment. Furthermore, the ADC1175 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC1175's reference ladder is available for connections, enabling a wide range of input possibilities.

The ADC1175 is offered in a TSSOP. It is designed to operate over the commercial temperature range of -20°C to +75°C.

Features

- Internal Sample-and-Hold Function
- Single +5V Operation
- Internal Reference Bias Resistors
- Industry Standard Pinout
- TRI-STATE Outputs

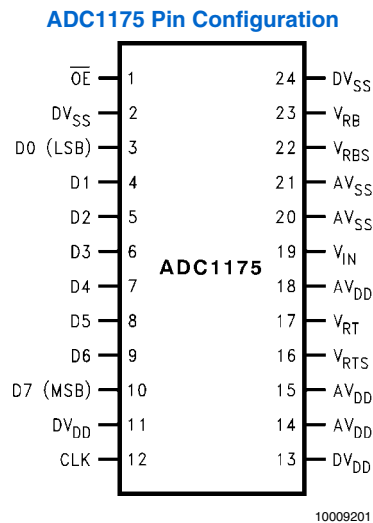
Key Specifications

■ Resolution	8 Bits
■ Maximum Sampling Frequency	20 Msps (min)
■ DNL	0.75 LSB (max)
■ ENOB	7.5 Bits (typ)
■ Guaranteed No Missing Codes	
■ Power Consumption (excluding I _{REF})	60mW (typ)

Applications

- Video Digitization
- Digital Still Cameras
- Personal Computer Video Cameras
- CCD Imaging
- Electro-Optics

Pin Configuration

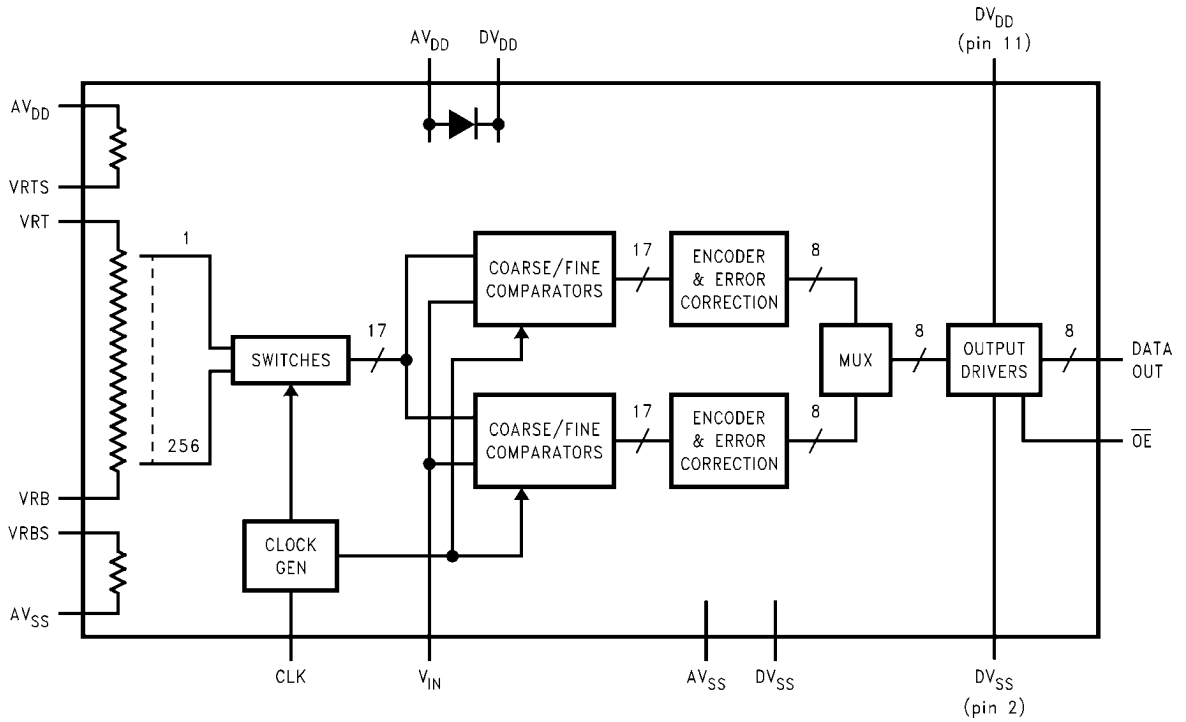


Ordering Information

Order Code	Temperature	Description
ADC1175CIJM *	-20°C to +75°C	SOIC (EIAJ)
ADC1175CIJMX *	-20°C to +75°C	SOIC (EIAJ) (tape & reel)
ADC1175CIMTC	-20°C to +75°C	TSSOP
ADC1175CIMTCX	-20°C to +75°C	TSSOP (tape & reel)
ADC1175EVAL *		Evaluation Board

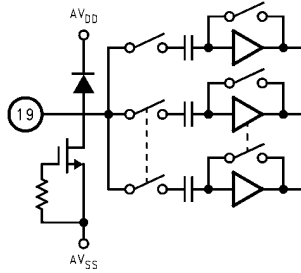
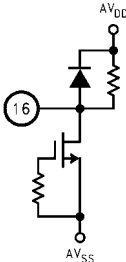
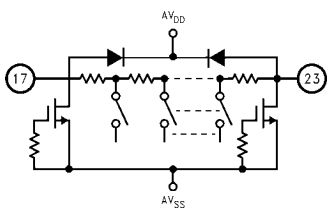
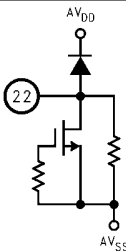
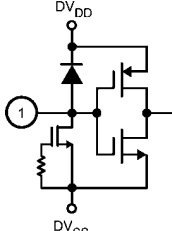
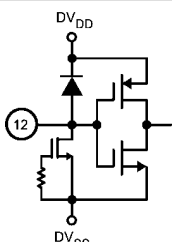
* Discontinued in the SOIC (EIAJ) package. The Evaluation Board is also discontinued. Shown for reference only.

Block Diagram



10009202

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
19	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT} .
16	V_{RTS}		Reference Top Bias with internal pull-up resistor. Short this pin to V_{RT} to self bias the reference ladder.
17	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to AV_{DD} . Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
23	V_{RB}		Analog Input that is the low (bottom) side of the reference ladder of the ADC. Nominal range is 0V to 4.0V. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
22	V_{RBS}		Reference Bottom Bias with internal pull down resistor. Short to V_{RB} to self bias the reference ladder.
1	\overline{OE}		CMOS/TTL compatible Digital input that, when low, enables the digital outputs of the ADC1175. When high, the outputs are in a high impedance state.
12	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.

Pin No.	Symbol	Equivalent Circuit	Description
3 thru 10	D0-D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are enabled by bringing the \overline{OE} pin low.
13	DV _{DD}		Positive digital supply pin. Connect to a clean voltage source of +5V. AV _{DD} and DV _{DD} should have a common source and be separately bypassed with a 10 μ F capacitor and a 0.1 μ F ceramic chip capacitor. See Section 3.0 for more information.
11	DV _{DD}		This digital supply pin supplies power for the digital output drivers. This pin should be connected to a supply source in the range of 2.5V to the Pin 13 potential.
2, 24	DV _{SS}		The ground return for the digital supply. AV _{SS} and DV _{SS} should be connected together close to the ADC1175.
14, 15, 18	AV _{DD}		Positive analog supply pin. Connected to a quiet voltage source of +5V. AV _{DD} and DV _{DD} should have a common source and be separately bypassed with a 10 μ F capacitor and a 0.1 μ F ceramic chip capacitor. See Section 3.0 for more information.
20, 21	AV _{SS}		The ground return for the analog supply. AV _{SS} and DV _{SS} should be connected together close to the ADC1175 package.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

AV_{DD}, DV_{DD}	6.5V
Voltage on Any Pin	-0.3V to 6.5V
V_{RT}, V_{RB}	AV_{SS} to AV_{DD}
CLK, OE Voltage	-0.5 to $(AV_{DD} + 0.5V)$
Digital Output Voltage	DV_{SS} to DV_{DD}
Input Current (Note 3)	$\pm 25mA$
Package Input Current (Note 3)	$\pm 50mA$
Package Dissipation at 25°C	(Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Machine Model	200V
Soldering Temp., Infrared, 10 sec. (Note 6)	300°C
Storage Temperature	-65°C to +150°C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	$-20^{\circ}C \leq T_A \leq +75^{\circ}C$
Supply voltage (AV_{DD}, DV_{DD})	+4.75V to +5.25V
$AV_{DD} - DV_{DD}$	<0.5V
$ AV_{SS} - DV_{SS} $	0V to 100 mV
Pin 13 - Pin 11 Voltage	<0.5V
V_{RT}	1.0V to V_{DD}
V_{RB}	0V to 4.0V
$V_{RT} - V_{RB}$	1V to 2.8V
V_{IN} Voltage Range	V_{RB} to V_{RT}

Package Thermal Resistance

Package	θ_{JA}
TSSOP-24	92°C / W

Converter Electrical Characteristics

The following specifications apply for $AV_{DD} = DV_{DD} = +5.0V_{DC}$, $\overline{OE} = 0V$, $V_{RT} = +2.6V$, $V_{RB} = 0.6V$, $C_L = 20$ pF, $f_{CLK} = 20$ MHz at 50% duty cycle. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^{\circ}C$ (Notes 7, 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units
DC Accuracy					
INL	Integral Non Linearity	$f_{CLK} = 20$ MHz	± 0.5	± 1.3	LSB (max)
INL	Integral Non Linearity	$f_{CLK} = 30$ MHz	± 1.0		LSB (max)
DNL	Differential Non Linearity	$f_{CLK} = 20$ MHz	± 0.35	± 0.75	LSB (max)
DNL	Differential Non Linearity	$f_{CLK} = 30$ MHz	± 1.0		LSB (max)
	Missing Codes			0	(max)
E_{OT}	Top Offset		-24		mV
E_{OB}	Bottom Offset		+37		mV
Video Accuracy					
DP	Differential Phase Error	$f_{in} = 4.43$ MHz sine wave, $f_{CLK} = 17.7$ MHz	0.5		Degree
DG	Differential Gain Error	$f_{in} = 4.43$ MHz sine wave, $f_{CLK} = 17.7$ MHz	0.4		%
Analog Input and Reference Characteristics					
V_{IN}	Input Range		2.0	V_{RB} V_{RT}	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance	$V_{IN} = 1.5V + 0.7V_{rms}$	(CLK LOW)	4	pF
			(CLK HIGH)	11	
R_{IN}	R_{IN} Input Resistance		>1		M Ω
BW	Analog Input Bandwidth		120		MHz
R_{RT}	Top Reference Resistor		360		Ω
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}		200	Ω (min)
				400	Ω (max)
R_{RB}	Bottom Reference Resistor		90		Ω
I_{REF}	Reference Ladder Current	$V_{RT} = V_{RTS}, V_{RB} = V_{RBS}$	7	4.8 9.3	mA (min) mA (max)
		$V_{RT} = V_{RTS}, V_{RB} = AV_{SS}$	8	5.4 10.5	mA (min) mA (max)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units
V_{RT}	Reference Top Self Bias Voltage	V_{RT} connected to V_{RTS} V_{RB} connected to V_{RBS}	2.6		V
V_{RB}	Reference Bottom Self Bias Voltage	V_{RT} connected to V_{RTS} V_{RB} connected to V_{RBS}	0.6	0.55 0.65	V (min) V (max)
$V_{RTS} - V_{RBS}$	Self Bias Voltage Delta	V_{RT} connected to V_{RTS} , V_{RB} connected to V_{RBS}	2	1.89 2.15	V (min) V (max)
		V_{RT} connected to V_{RTS} , V_{RB} connected to AV_{SS}	2.3		V
$V_{RT} - V_{RB}$	Reference Voltage Delta		2	1.0 2.8	V (min) V (max)
Power Supply Characteristics					
$I_{A_{DD}}$	Analog Supply Current	$DV_{DD} = AV_{DD} = 5.25V$	9.5		mA
$I_{D_{DD}}$	Digital Supply Current	$DV_{DD} = AV_{DD} = 5.25V$	2.5		mA
$I_{A_{DD}} + I_{D_{DD}}$	Total Operating Current	$DV_{DD} = AV_{DD} = 5.25V, f_{CLK} = 20 \text{ MHz}$	12	17	mA (max)
		$DV_{DD} = AV_{DD} = 5.25V, f_{CLK} = 30 \text{ MHz}$	13		
		$DV_{DD} = AV_{DD} = 5.25V, \text{CLK Low}$ (Note 10)	9.6		mA
	Power Consumption	$DV_{DD} = AV_{DD} = 5.25V, f_{CLK} = 20 \text{ MHz}$	60	85	mW (max)
		$DV_{DD} = AV_{DD} = 5.25V, f_{CLK} = 30 \text{ MHz}$	65		mW
CLK, \overline{OE} Digital Input Characteristics					
V_{IH}	Logical High Input Voltage	$DV_{DD} = AV_{DD} = +5.25V$		3.0	V (min)
V_{IL}	Logical Low Input Voltage	$DV_{DD} = AV_{DD} = +5.25V$		1.0	V (max)
I_{IH}	Logical High Input Current	$V_{IH} = DV_{DD} = AV_{DD} = +5.25V$	5		μA
I_{IL}	Logic Low Input Current	$V_{IL} = 0V, DV_{DD} = AV_{DD} = +5.25V$	-5		μA
C_{IN}	Logic Input Capacitance		5		pF
Digital Output Characteristics					
I_{OH}	High Level Output Current	$DV_{DD} = 4.75V, V_{OH} = 2.4V$		-1.1	mA (max)
I_{OL}	Low Level Output Current	$DV_{DD} = 4.75V, V_{OL} = 0.4V$		1.6	mA (min)
I_{OZH}, I_{OZL}	Tri-State® Leakage Current	$DV_{DD} = 5.25V$ $\overline{OE} = DV_{DD}, V_{OL} = 0V$ or $V_{OH} = DV_{DD}$	± 20		μA
AC Electrical Characteristics					
f_{C1}	Maximum Conversion Rate		30	20	MHz (min)
f_{C2}	Minimum Conversion Rate		1		MHz
t_{OD}	Output Delay	CLK rise to data rising	19.5		ns
		CLK rise to data falling	16		ns
	Pipeline Delay (Latency)		2.5		Clock Cycles
t_{DS}	Sampling (Aperture) Delay	CLK low to acquisition of data	3		ns
t_{AJ}	Aperture Jitter		30		ps rms
t_{OH}	Output Hold Time	CLK high to data invalid	10		ns
t_{EN}	\overline{OE} Low to Data Valid	Loaded as in <i>Figure 2</i>	11		ns
t_{DIS}	\overline{OE} High to High Z State	Loaded as in <i>Figure 2</i>	15		ns
ENOB	Effective Number of Bits	$f_{IN} = 1.31 \text{ MHz}, V_{IN} = \text{FS} - 2 \text{ LSB}$	7.5	7.0	Bits (min)
		$f_{IN} = 4.43 \text{ MHz}, V_{IN} = \text{FS} - 2 \text{ LSB}$	7.3		
		$f_{IN} = 9.9 \text{ MHz}, V_{IN} = \text{FS} - 2 \text{ LSB}$	7.2		
		$f_{IN} = 4.43 \text{ MHz}, f_{CLK} = 30 \text{ MHz}$	6.5		

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units
SINAD	Signal-to- Noise & Distortion	$f_{IN} = 1.31 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 4.43 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 9.9 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 4.43 \text{ MHz}, f_{CLK} = 30 \text{ MHz}$	46.9 45.7 45.1 40.9	43	dB (min)
SNR	Signal-to- Noise Ratio	$f_{IN} = 1.31 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 4.43 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 9.9 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 4.43 \text{ MHz}, f_{CLK} = 30 \text{ MHz}$	47.6 46 46.1 42.1	44	dB (min)
SFDR	Spurious Free Dynamic Range	$f_{IN} = 1.31 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 4.43 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 9.9 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 4.43 \text{ MHz}, f_{CLK} = 30 \text{ MHz}$	56 58 53 47		dB
THD	Total Harmonic Distortion	$f_{IN} = 1.31 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 4.43 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 9.9 \text{ MHz}, V_{IN} = FS - 2 \text{ LSB}$ $f_{IN} = 4.43 \text{ MHz}, f_{CLK} = 30 \text{ MHz}$	-55 -57 -52 -47		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to $GND = AV_{SS} = DV_{SS} = 0V$, unless otherwise specified.

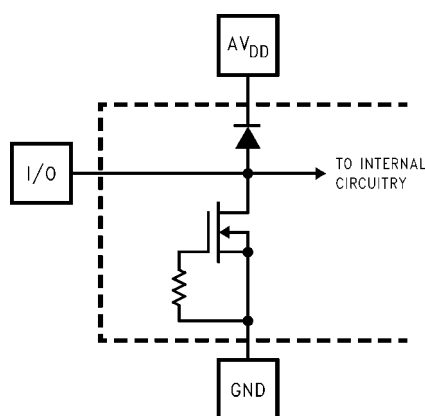
Note 3: When the input voltage at any pin exceeds the power supplies (that is, less than AV_{SS} or DV_{SS} , or greater than AV_{DD} or DV_{DD}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperatures (T_{jmax}) for this device is $150^{\circ}C$. The maximum allowable power dissipation is dictated by T_{jmax} , the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature, T_A , and can be calculated using the formula $P_{DMAX} = (T_{jmax} - T_A) / \theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC1175 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5k Ω resistor. Machine model is 220 pF discharged through ZERO Ω .

Note 6: See AN-450, "Surface Mounting Methods and Their Effect on Product Reliability", or the section entitled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The analog inputs are protected as shown below. Input voltage magnitudes up to 6.5V or 500 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_{DD} or below GND by more than 50 mV. As an example, if AV_{DD} is 4.75V $_{DC}$, the full-scale input voltage must be $\leq 4.80V_{DC}$ to ensure accurate conversions.



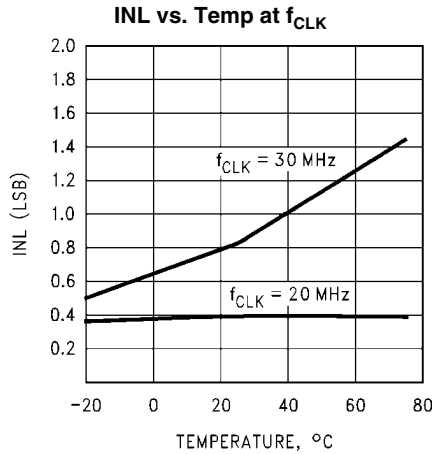
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Note 8: To guarantee accuracy, it is required that AV_{DD} and DV_{DD} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

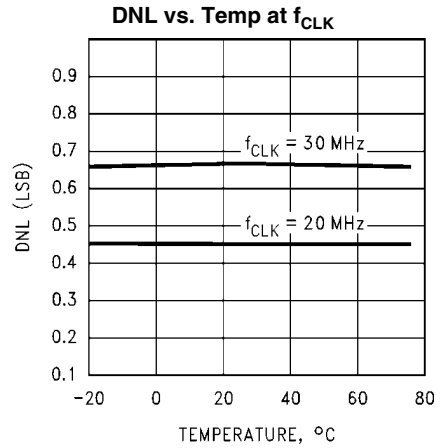
Note 9: Typical figures are at $T_J = 25^{\circ}C$, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: At least two clock cycles must be presented to the ADC1175 after power up. See Section 4.0 for details.

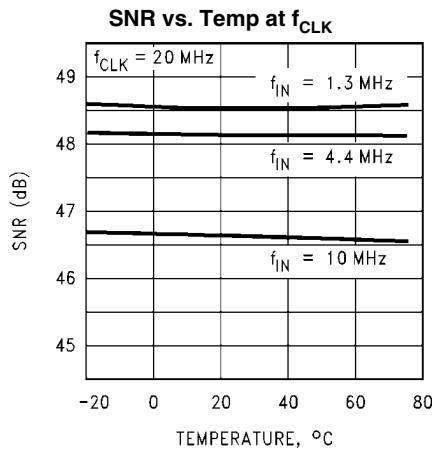
Typical Performance Characteristics



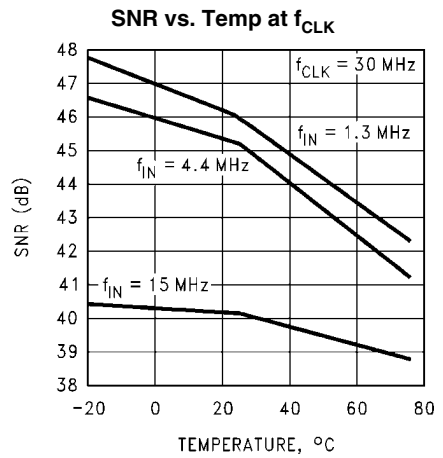
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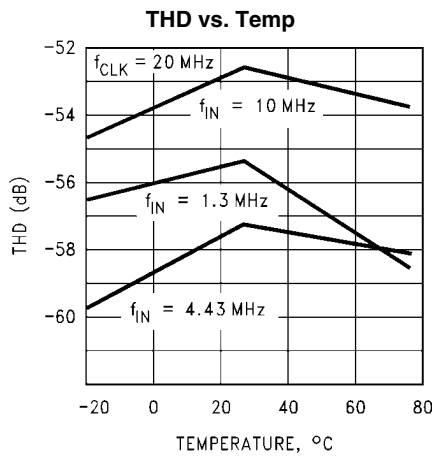
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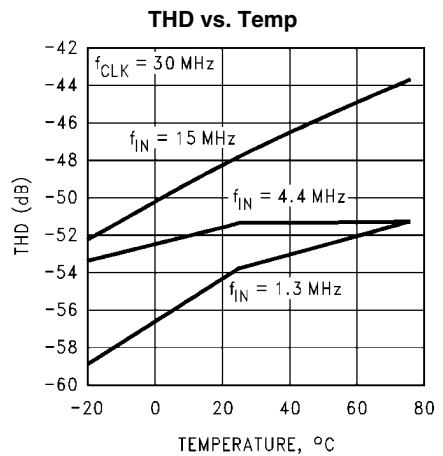
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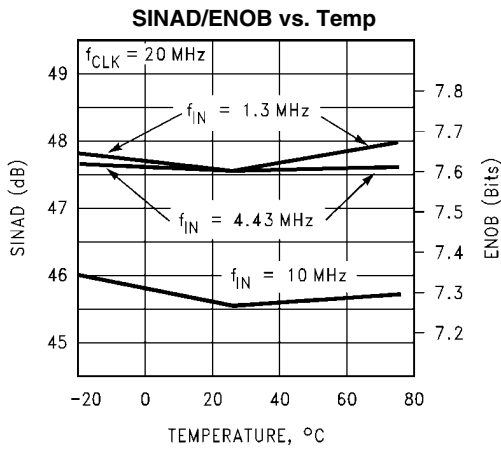
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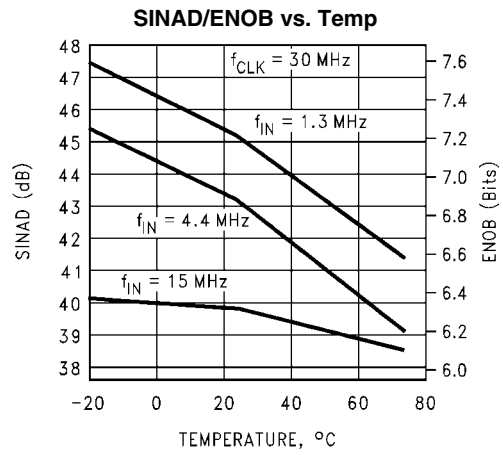
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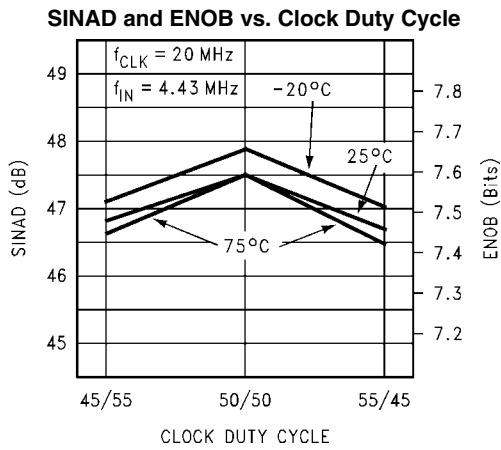
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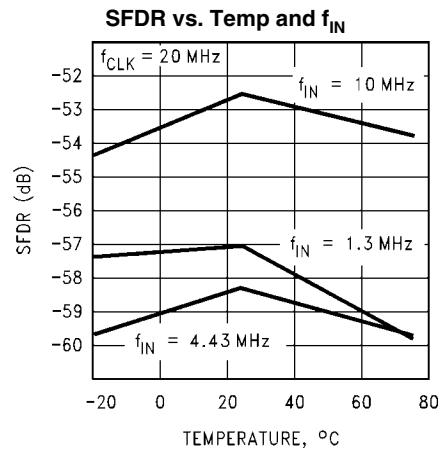
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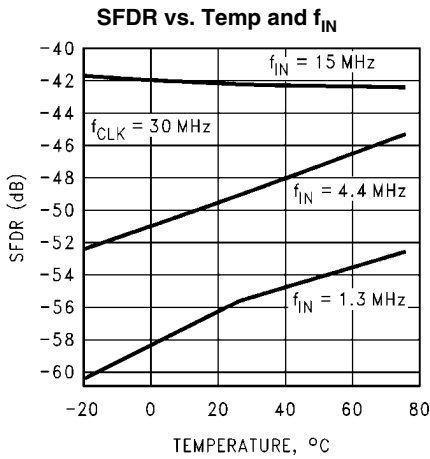
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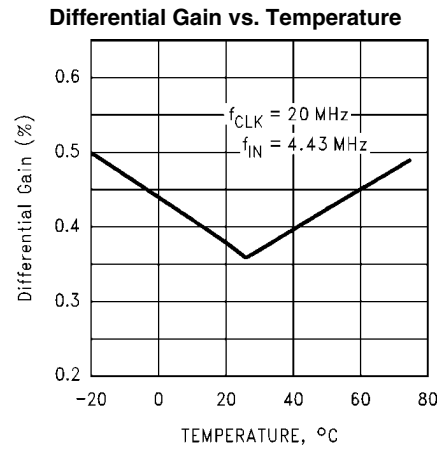
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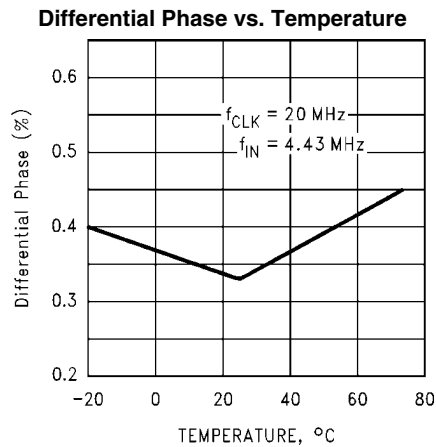
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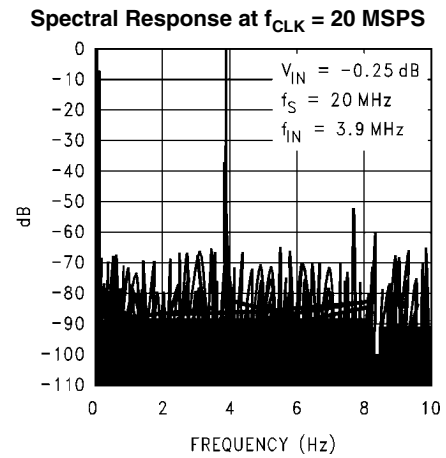
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Specification Definitions

ANALOG INPUT BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with f_{IN} equal to 100 kHz plus integer multiples of f_{CLK} . The input frequency at which the output is -3 dB relative to the low frequency input signal is the full power bandwidth.

APERTURE JITTER is the time uncertainty of the sampling point (t_{DS}), or the range of variation in the sampling delay.

BOTTOM OFFSET is the difference between the input voltage that just causes the output code to transition to the first code and the negative reference voltage. Bottom offset is defined as $E_{OB} = V_{ZT} - V_{RB}$, where V_{ZT} is the first code transition input voltage. Note that this is different from the normal Zero Scale Error.

DIFFERENTIAL GAIN ERROR is the percentage difference between the output amplitudes of a high frequency reconstructed sine wave at two different d.c. levels.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DIFFERENTIAL PHASE ERROR is the difference in the output phase of a reconstructed small signal sine wave at two different d.c. levels.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as $(SINAD - 1.76) / 6.02$ and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale ($1/2$ LSB below the first code transition) through positive full scale ($1/2$ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output stage. Data for any give sample is available the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

SAMPLING (APERTURE) DELAY is that time required after the fall of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode t_{DS} after the clock goes low.

SIGNAL TO NOISE RATIO (SNR) is the ratio of the rms value of the input signal to the rms value of the other spectral components below one-half the sampling frequency, not including harmonics or d.c.

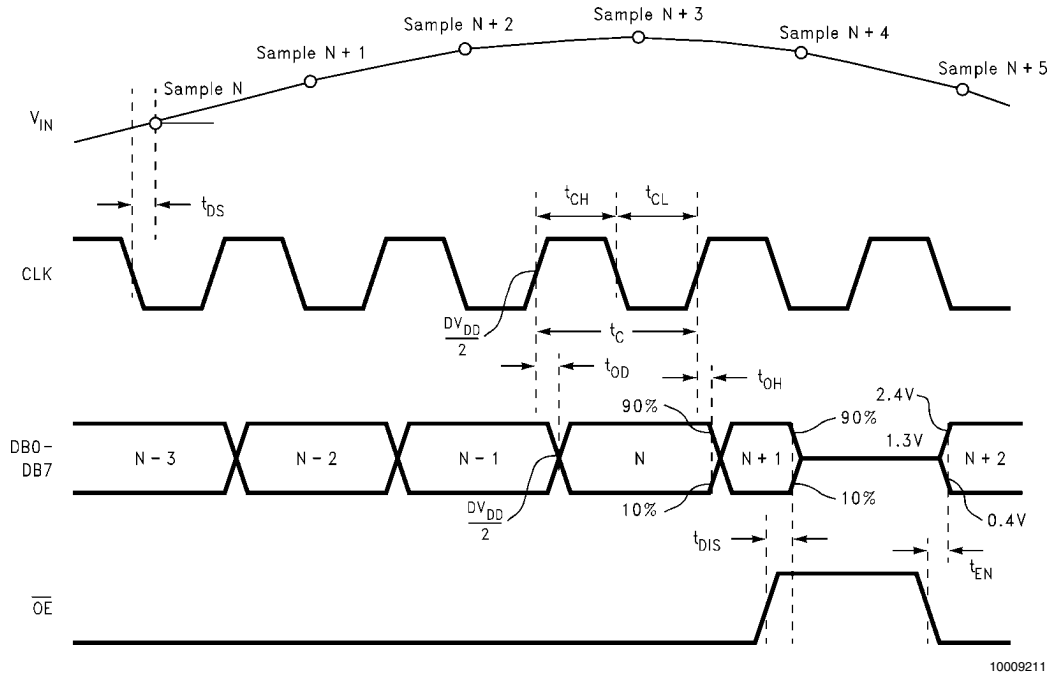
SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOP OFFSET is the difference between the positive reference voltage and the input voltage that just causes the output code to transition to full scale and is defined as $E_{OT} = V_{FT} - V_{RT}$. Where V_{FT} is the full scale transition input voltage. Note that this is different from the normal Full Scale Error.

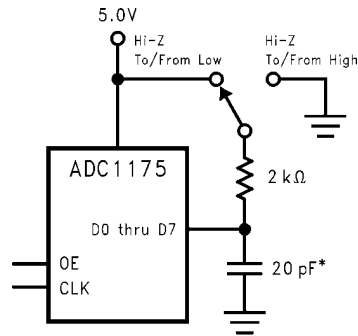
TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first six harmonic components, to the rms value of the input signal.

Timing Diagram



10009211

FIGURE 1. ADC1175 Timing Diagram



* Includes stray and distributed capacitance

10009212

FIGURE 2. t_{EN} , t_{DIS} Test Circuit

Functional Description

The ADC1175 uses a new, unique architecture to achieve 7.2 effective bits at and maintains superior dynamic performance up to $\frac{1}{2}$ the clock frequency.

The analog signal at V_{IN} that is within the voltage range set by V_{RT} and V_{RB} are digitized to eight bits at up to 30 MSPS. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RT} will cause the output word to consist of all ones. V_{RT} has a range of 1.0 Volt to the analog supply voltage, AV_{DD} , while V_{RB} has a range of 0 to 4.0 Volts. V_{RT} should always be between 1.0 Volt and 2.8 Volts more positive than V_{RB} .

If V_{RT} and V_{RTS} are connected together and V_{RB} and V_{RBS} are connected together, the nominal values of V_{RT} and V_{RB} are 2.6V and 0.6V, respectively. If V_{RT} and V_{RTS} are connected together and V_{RB} is grounded, the nominal value of V_{RT} is 2.3V.

Data is acquired at the falling edge of the clock and the digital equivalent of the data is available at the digital outputs 2.5 clock cycles plus t_{OD} later. The ADC1175 will convert as long as the clock signal is present at pin 12. The Output Enable pin \overline{OE} , when low, enables the output pins. The digital outputs are in the high impedance state when the \overline{OE} pin is high.

Applications Information

1.0 THE ANALOG INPUT

The analog input of the ADC1175 is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 4 pF when the clock is low, and 11 pF when the clock is high. Since a dynamic capacitance is more difficult to drive than a fixed capacitance, choose an amplifier that can drive this type of load. The LMH6702, LMH6609, LM6152, LM6154, LM6181 and LM6182 have been found to be excellent devices for driving the ADC1175. Do not drive the input beyond the supply rails. *Figure 3* shows an example of an input circuit using the LMH6702.

Driving the analog input with input signals up to 2.8 V_{P-P} will result in normal behavior where signals above V_{RT} will result in a code of FFh and input voltages below V_{RB} will result in an output code of zero. Input signals above 2.8 V_{P-P} may result in odd behavior where the output code is not FFh when the input exceeds V_{RT} .

2.0 REFERENCE INPUTS

The reference inputs V_{RT} (Reference Top) and V_{RB} (Reference Bottom) are the top and bottom of the reference ladder.

Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in the Operating Ratings table (1.0V to AV_{DD} for V_{RT} and 0V to $(AV_{DD} - 1.0V)$ for V_{RB}). Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin.

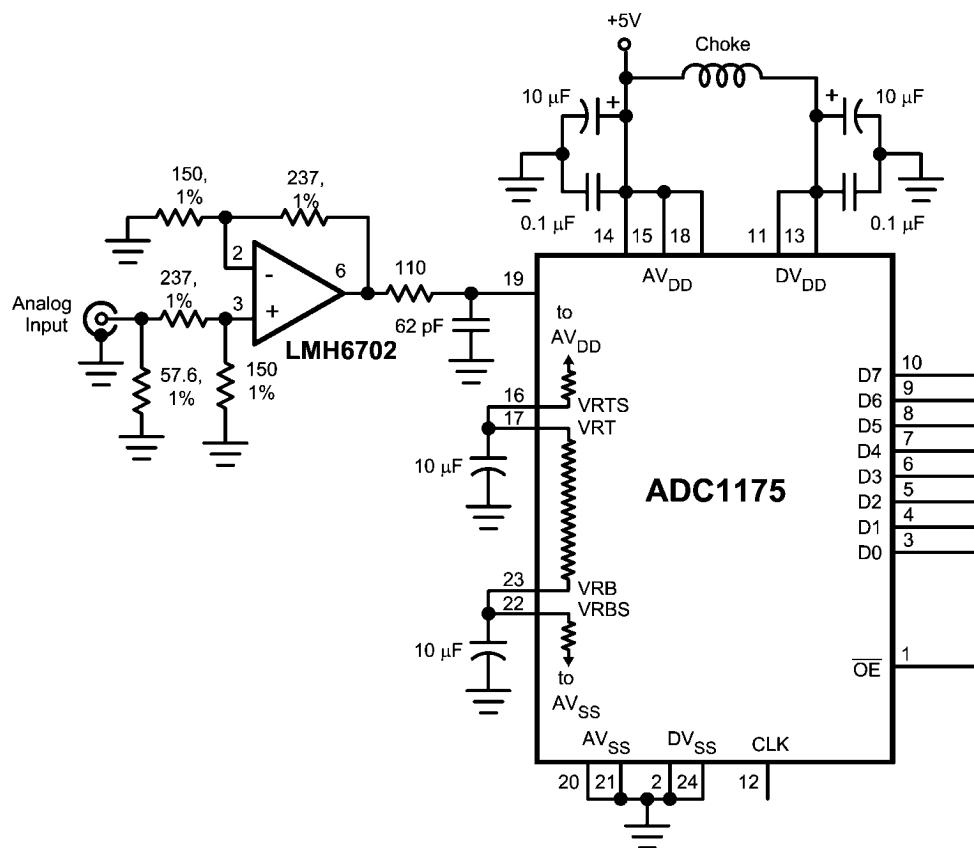
The reference ladder can be self-biased by connecting V_{RT} to V_{RTS} and connecting V_{RB} to V_{RBS} to provide top and bottom reference voltages of approximately 2.6V and 0.6V, respectively, with $V_{CC} = 5.0V$. This connection is shown in *Figure 3*. If V_{RT} and V_{RTS} are tied together, but V_{RB} is tied to analog ground, a top reference voltage of approximately 2.3V is generated. The top and bottom of the ladder should be bypassed with 10 μ F tantalum capacitors located close to the reference pins.

The reference self-bias circuit of *Figure 3* is very simple and performance is adequate for many applications. Superior performance can generally be achieved by driving the reference pins with a low impedance source.

By forcing a little current into or out of the top and bottom of the ladder, as shown in *Figure 4*, the top and bottom reference voltages can be trimmed and performance improved over the self-bias method of *Figure 3*. The resistive divider at the amplifier inputs can be replaced with potentiometers. The LMC662 amplifier shown was chosen for its low offset voltage and low cost. Note that a negative power supply is needed for these amplifiers if their outputs are required to go slightly negative to force the required reference voltages.

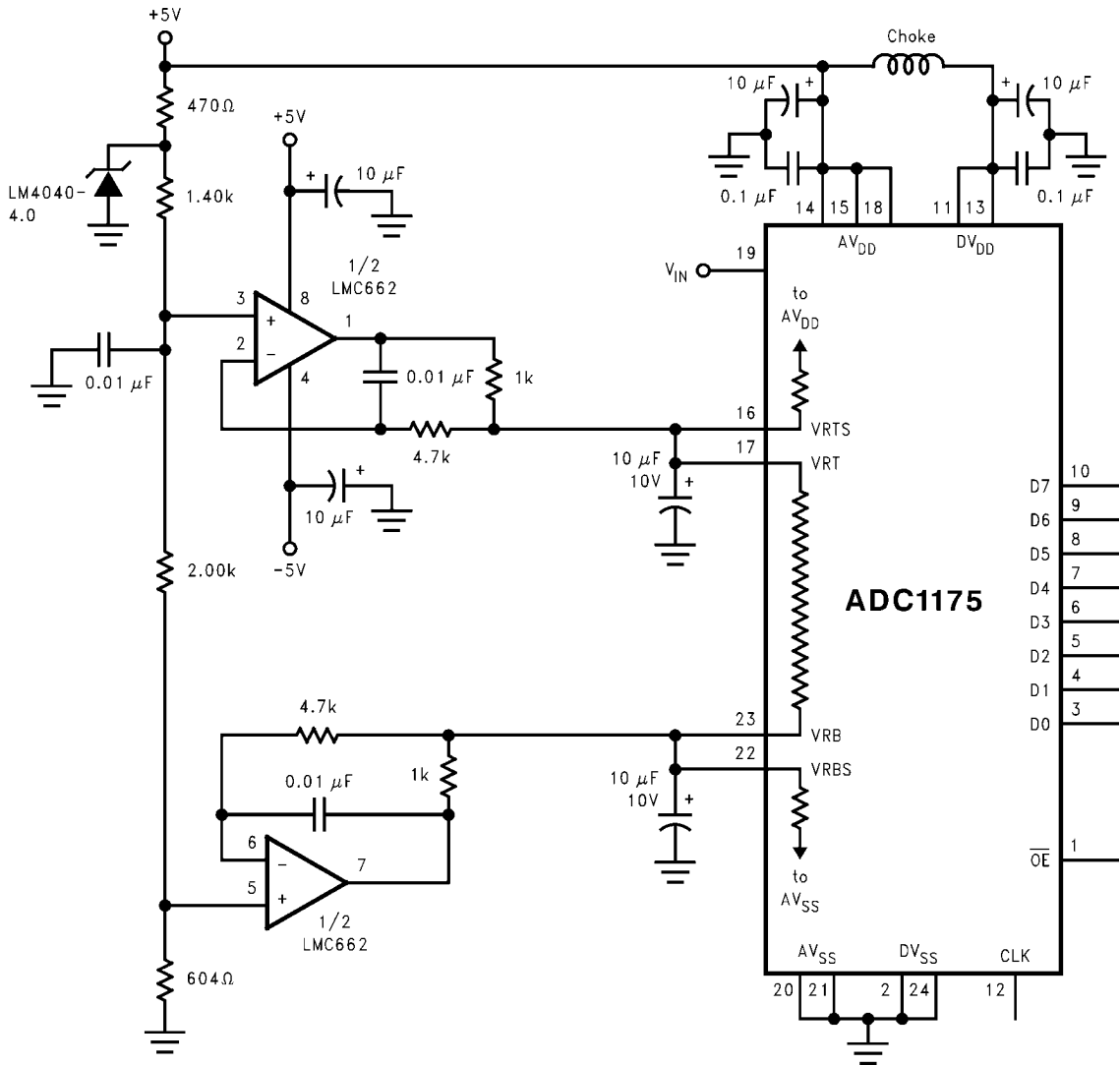
If reference voltages are desired that are more than a few tens of millivolts from the self-bias values, the circuit of *Figure 5* will allow forcing the reference voltages to whatever levels are desired. This circuit provides the best performance because of the low source impedance of the transistors. Note that the V_{RTS} and V_{RBS} pins are left floating.

V_{RT} can be anywhere between $V_{RB} + 1.0V$ and the analog supply voltage, and V_{RB} can be anywhere between ground and 1.0V below V_{RT} . To minimize noise effects and ensure accurate conversions, the total reference voltage range ($V_{RT} - V_{RB}$) should be a minimum of 1.0V and a maximum of about 2.8V. If V_{RB} is not required to be below about +700mV, the -5V points in *Figure 5* can be returned to ground and the negative supply eliminated.



10009213

FIGURE 3. Simple, Low Component Count, Self-Bias Reference application. Because of resistor tolerances, the reference voltages can vary by as much as 6%. Choose an amplifier that can drive a dynamic capacitance (see text).



10009214

FIGURE 4. Better defining the ADC Reference Voltage. Self-bias is still used, but the reference voltages are trimmed by providing a small trim current with the operational amplifiers.

4.0 THE ADC1175 CLOCK

Although the ADC1175 is tested and its performance is guaranteed with a 20MHz clock, it typically will function with clock frequencies from 1MHz to 30MHz.

If continuous conversions are not required, power consumption can be reduced somewhat by stopping the clock at a logic low when the ADC1175 is not being used. This reduces the current drain in the ADC1175's digital circuitry from a typical value of 2.5mA to about 100 μ A.

Note that powering up the ADC1175 without the clock running may not save power, as it will result in an increased current flow (by as much as 170%) in the reference ladder. In some cases, this may increase the ladder current above the specified limit. Toggling the clock twice at 1MHz or higher and returning it to the low state will eliminate the excess ladder current.

An alternative power-saving technique is to power up the ADC1175 with the clock active, then halt the clock in the low state after two or more clock cycles. Stopping the clock in the high state is not recommended as a power-saving technique.

5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals is essential to ensure accurate conversion. Separate analog and digital ground planes that are connected beneath the ADC1175 may be used, but best EMI practices require a single ground plane. However, it is important to keep analog signal lines away from digital signal lines and away from power supply currents. This latter requirement requires the careful separation and placement of power planes. The use of power traces rather than one or more power planes is not recommended as higher frequencies are not well filtered with lumped capacitances. To filter higher frequency noise components it is necessary to have sufficient capacitance between the power and ground planes.

If separate analog and digital ground planes are used, the analog and digital grounds may be in the same layer, but should be separated from each other. If separate analog and digital ground layers are used, they should *never overlap* each other.

Capacitive coupling between a typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families. In general, slower logic families will produce less high frequency noise than do high speed logic families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

An effective way to control ground noise is by using a single, solid ground plane, splitting the power plane into analog and digital areas and having power and ground planes in adjacent board layers. There should be no traces within either the

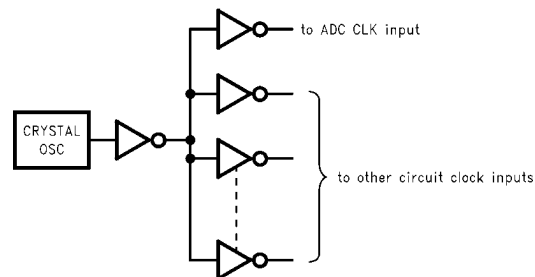
power or the ground layers of the board. The analog and digital power planes should reside in the same board layer so that they can not overlap each other. The analog and digital power planes define the analog and digital areas of the board. Generally, analog and digital lines should cross each other at 90 degrees to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog and digital. Even the generally accepted 90 degree crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies and at high resolution is obtained with a straight signal path.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should not be placed side by side, not even with just a small part of their bodies being beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground return.

6.0 DYNAMIC PERFORMANCE

The ADC1175 is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications, the clock source driving the CLK input must be free of jitter. For best a.c. performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See Figure 6.



10009217

FIGURE 6. Isolating the ADC clock from Digital Circuitry.

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal.

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 50mV below the ground pins or 50mV above the supply pins. Exceeding these limits on even a transient basis can cause faulty or erratic operation. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground due to improper line termination. A resistor of 50 Ω to 100 Ω in series with the offending digital input, located close to the signal source, will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC1175. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for

each conversion, the more instantaneous digital current is required from DV_{DD} and DGND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with an 74AC541, for example) may be necessary if the data bus to be driven is heavily loaded. Dynamic performance can also be improved by adding 47Ω to 100Ω series resistors at each digital output, reducing the energy coupled back into the converter output pins.

Using an inadequate amplifier to drive the analog input.

As explained in Section 1.0, the capacitance seen at the input alternates between 4 pF and 11 pF with the clock. This dynamic capacitance is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving device. The LMH6702, LMH6609, LM6152, LM6154, LM6181 and LM6182 have been found to be excellent devices for driving the ADC1175 analog input.

Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in section 2.0, care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices that can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. Simple gates with RC timing is generally inadequate as a clock source.

Input test signal contains harmonic distortion that interferes with the measurement of dynamic signal to noise ratio. Harmonic and other interfering signals can be removed by inserting a filter at the signal input. Suitable filters are shown in *Figure 7* and *Figure 8*. The circuit of *Figure 7* has cutoff of about 5.5 MHz and is suitable for input frequencies of 1 MHz to 5 MHz. The circuit of *Figure 8* has a cutoff of about 11 MHz and is suitable for input frequencies of 5 MHz to 10 MHz. These filters should be driven by a generator of 75 Ohm source impedance and terminated with a 75 Ohm resistor.

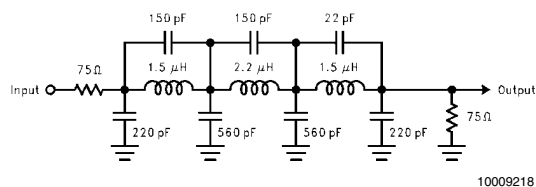


FIGURE 7. 5.5 MHz Low Pass Filter to Eliminate Harmonics at the Signal Input.

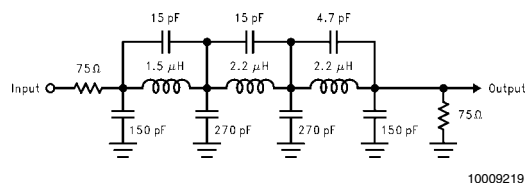
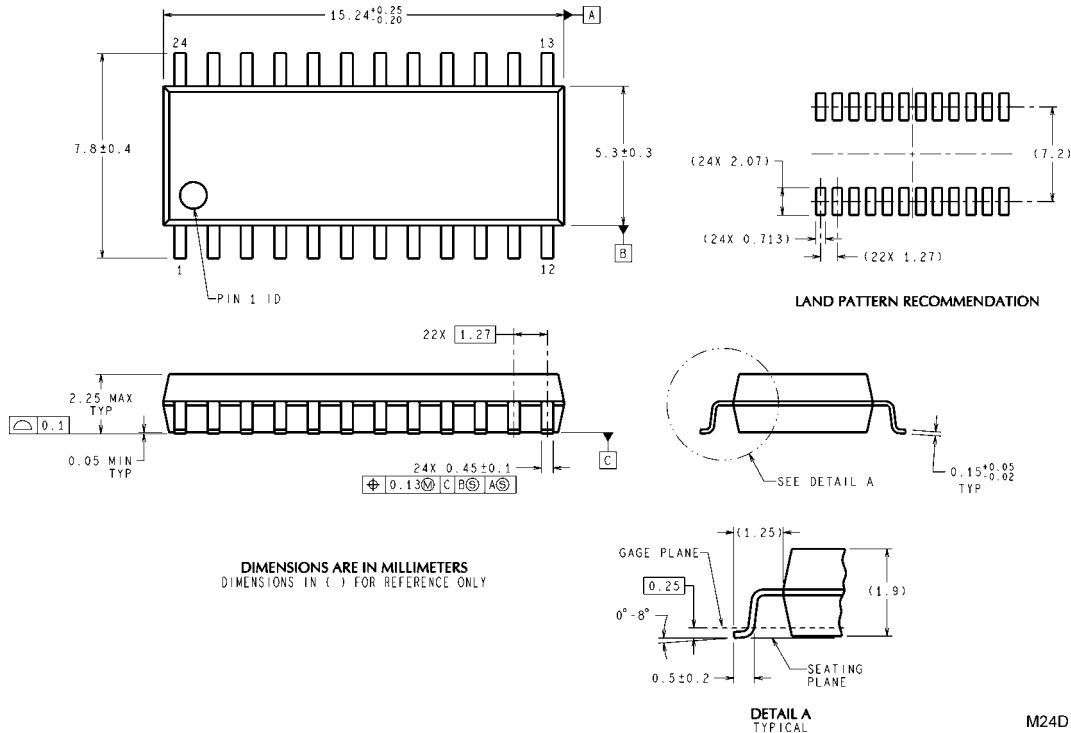


FIGURE 8. 11 MHz Low Pass filter to eliminate harmonics at the signal input. Use at input frequencies of 5 MHz to 10 MHz

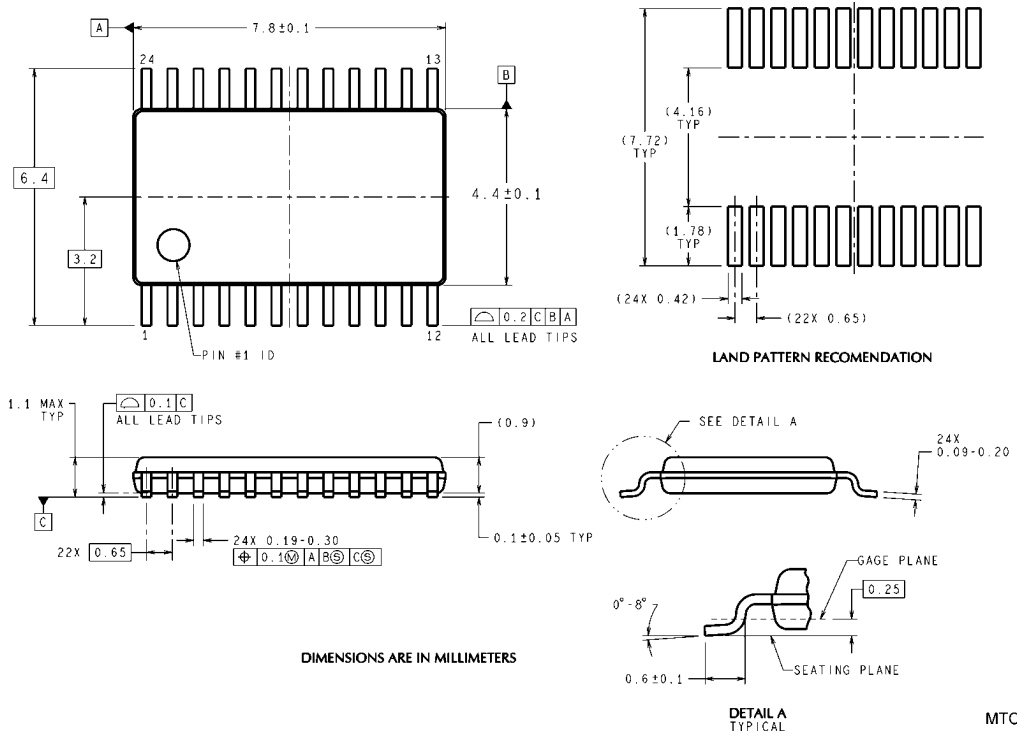
Not considering the effect on a driven CMOS digital circuit(s) when the ADC1175 is in the power down mode. Because the ADC1175 output goes into a high impedance state when in the power down mode, any CMOS device connected to these outputs will have their inputs floating when the ADC is in power down. Should the inputs of the circuit being driven by the ADC digital outputs float to a level near 2.5V, a CMOS device could exhibit relative large supply currents as the input stage toggles rapidly. The solution is to use pull-down resistors at the ADC outputs. The value of these resistors is not critical, as long as they do not cause excessive currents in the outputs of the ADC1175. Low pull-down resistor values could result in degraded SNR and SINAD performance of the ADC1175. Values between 5 k Ω and 100 k Ω should work well.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Package JM
Ordering Number ADC1175CIJM
NS Package Number M24D

M24D (Rev B)



24-Lead Package TC
Ordering Number ADC1175CIMTC
NS Package Number MTC24

MTC24 (Rev E)

Notes

Notes

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Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
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