February 1995

10-Bit, 20 MSPS A/D Converter

Features

- Resolution 10-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency 20 MSPS
- Low Power Consumption 140mW (Reference Current Excluded)
- Standby Mode Power 5mW
- No Sample and Hold Required
- TTL/CMOS Compatible I/O
- Three-State Outputs
- Single +5V Analog Power Supply
- Single +3.3V or +5V Digital Power Supply
- Evaluation Board Available: HI5710EVAL

Applications

- Video Digitizing - Multimedia
- Data Communications
- Image Scanners
- Medical Imaging
- Video Recording Equipment
- Camcorders
- QAM Demodulation

Description

The HI5710 is a low power, 10-bit, CMOS analog-to-digital converter. The use of a 2-step architecture realizes low power consumption, 140mW, and a maximum conversion speed of 20MHz with only a 3 clock cycle data latency. The HI5710 can be powered down, disabling the chip and the digital outputs, reducing power to less than 5mW. A built-in, user controlled, calibration circuit is used to provide low linearity error, 1 LSB. The low power, high speed and small package outline make the HI5710 an ideal choice for CCD, battery, and high channel count applications.

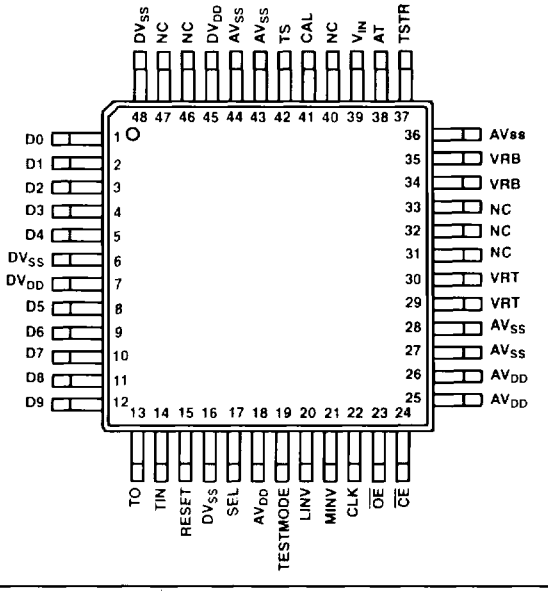
The HI5710 does not require an external sample and hold but requires an external reference and includes force and sense reference pins for increased accuracy. The digital outputs can be inverted, with the MSB controlled separately, allowing for various digital output formats. The HI5710 includes a test mode where the digital outputs can be set to a fixed state to ease in-circuit testing.

Ordering Information

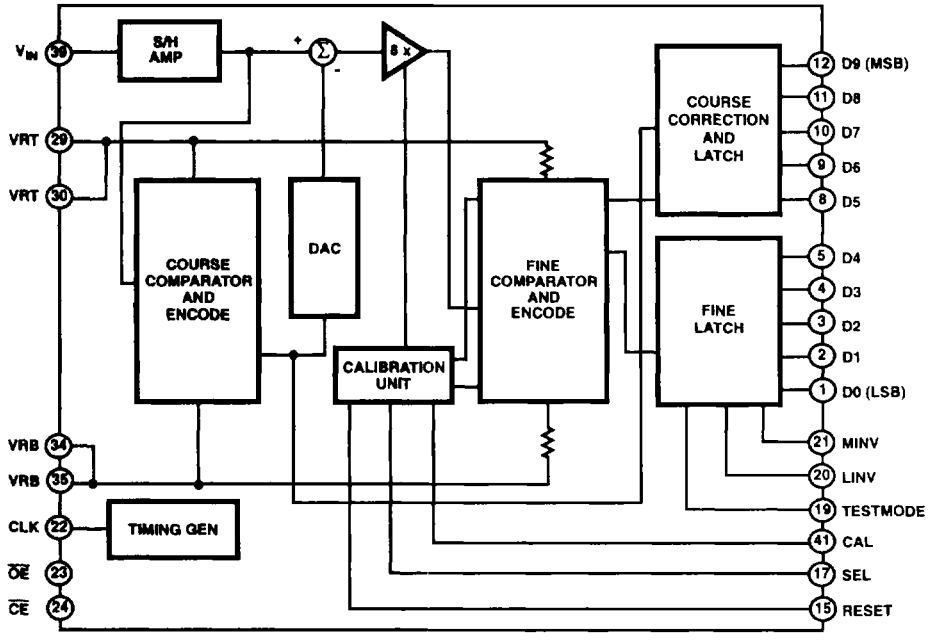
PART NUMBER	TEMP. RANGE	PACKAGE
HI5710JCQ	0°C to +75°C	48 Lead Plastic Metric Quad Flatpack

Pinout

HI5710 (MQFP)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Analog Input Voltage, V_{IN} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Input Voltage, V_{IH}, V_{IL} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Output Voltage, V_{OH}, V_{OL} . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Storage Temperature, T_{STG} . . . . . -55°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
(Lead Tips Only)

Thermal Information

Thermal Resistance θ_{JA}
HI5710JCQ . . . . . 111°C/W
Operating Temperature, T_A . . . . . 0°C to +75°C
Maximum Junction Temperature . . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions (Note 1)

Supply Voltage
AV_{DD}, AV_{SS} . . . . . +5V ± 0.25V
DV_{DD}, DV_{SS} . . . . . +3.3V ± 0.25V
IDGND-AGNDI . . . . . 0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . 1.8V to 2.8V
V_{RT} . . . . . 3.6V to 4.6V
Analog Input Range, V_{IN} . . . . . (V_{RT} - V_{RB}) (1.8V_{P-P} to 2.8V_{P-P})
Clock Pulse Width
T_{PW1} . . . . . 25ns (Min)
T_{PW0} . . . . . 25ns (Min)

Electrical Specifications

F_C = 20 MSPS, AV_{DD} = +5V, DV_{DD} = +3.3V, V_{RB} = 2.0V, V_{RT} = 4.0V, T_A = +25°C (Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
Offset Voltage	E_{OT}		47	67	87	mV
	E_{OB}		-68	-48	-28	mV
Integral Non-Linearity, INL		V_{IN} = 2.0V to 4.0V	-	±1.3	±2.0	LSB
Differential Non-Linearity, DNL			-	±0.5	±1.0	LSB
DYNAMIC CHARACTERISTICS						
Maximum Conversion Speed, F_C		F_{IN} = 1kHz Ramp	20	-	-	MSPS
Minimum Conversion Speed, F_C			-	-	0.5	MSPS
Effective Number of Bits, ENOB		F_{IN} = 3MHz	-	8.7	-	Bits
Signal to Noise and Distortion, SINAD		F_{IN} = 100kHz	-	53	-	dB
		F_{IN} = 500kHz	-	52	-	dB
		F_{IN} = 1MHz	-	53	-	dB
		F_{IN} = 3MHz	-	54	-	dB
		F_{IN} = 7MHz	-	47	-	dB
		F_{IN} = 10MHz	-	45	-	dB
Spurious Free Dynamic Range, SFDR		F_{IN} = 100kHz	-	60	-	dB
		F_{IN} = 500kHz	-	59	-	dB
		F_{IN} = 1MHz	-	60	-	dB
		F_{IN} = 3MHz	-	65	-	dB
		F_{IN} = 7MHz	-	50	-	dB
		F_{IN} = 10MHz	-	49	-	dB
Differential Gain Error, DG		NTSC 40 IRE Mod Ramp, F_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP			-	0.3	-	Degree

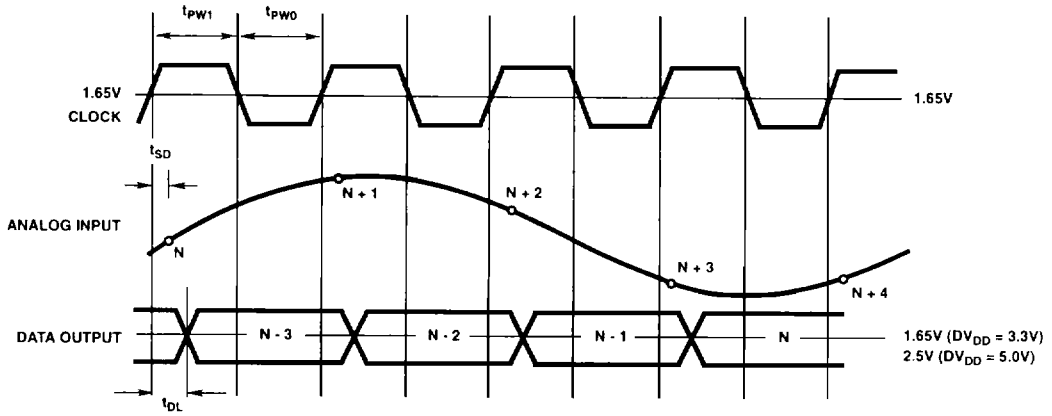
Electrical Specifications F_C = 20 MSPS, AV_{DD} = +5V, DV_{DD} = +3.3V, V_{RB} = 2.0V, V_{RT} = 4.0V, T_A = +25°C (Note 1) **(Continued)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
Analog Input Bandwidth (-3dB), BW				-	100	-	MHz
Analog Input Current		V_{IN} = 4V		-	-	50	µA
		V_{IN} = 2V		-50	-	-	µA
Analog Input Capacitance, C_{IN}		V_{IN} = 2.5V + 0.07V_{RMS}		-	9	-	pF
REFERENCE INPUT							
Reference Pin Current, I_{RT}		RESET = Low		7.2	8.2	9.2	mA
Reference Pin Current, I_{RB}		RESET = Low		4.2	5.2	6.2	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}				210	300	390	Ω
DIGITAL INPUTS							
Digital Input Voltage	V_{IH1}	AV_{DD} = 4.75V to 5.25V, $\overline{OE}$ Excluded		2.3	-	-	V
	V_{IL1}			-	-	0.80	V
Digital Input Voltage	V_{IH2}	$\overline{OE}$ Only		0.7 x DV_{DD}	-	-	V
	V_{IL2}			-	-	0.3 x DV_{DD}	V
Digital Input Current	I_{IH}	DV_{DD} = Max	V_{IH} = DV_{DD}	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS							
Digital Output Current	I_{OH}	$\overline{OE}$ = DV_{SS}, DV_{DD} = Min	V_{OH} = DV_{DD} -0.5V	4.0	-	-	mA
	I_{OL}		V_{OL} = 0.4V	3.5	-	-	mA
Digital Output Leakage Current	I_{OZH}	$\overline{OE}$ = DV_{DD}, DV_{DD} = Max	V_{OH} = DV_{DD}	-	-	1	µA
	I_{OZL}		V_{OL} = 0V	-	-	1	µA
TIMING CHARACTERISTICS							
Output Data Delay, T_{DL}		Load is One TTL Gate		8	13	18	ns
Output Enable/Disable Delay	t_{PZL}			10	15	20	ns
	t_{PLZ}			20	25	30	ns
	t_{PZH}			10	15	20	ns
	t_{PHZ}			20	25	30	ns
Sampling Delay, t_{SD}				-	4	6	ns
POWER SUPPLY CHARACTERISTIC							
Analog Supply Current, IA_{DD}		F_{IN} = 1kHz Ramp Wave Input		23	26	29	mA
Digital Supply Current, ID_{DD}				1.6	1.7	1.8	mA
Analog Standby Current		$\overline{CE}$ = High		-	-	1.0	mA
Digital Standby Current				-	-	1.0	µA

NOTE:

1. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams



o = INDICATES POINT AT WHICH ANALOG DATA IS SAMPLED

FIGURE 1.

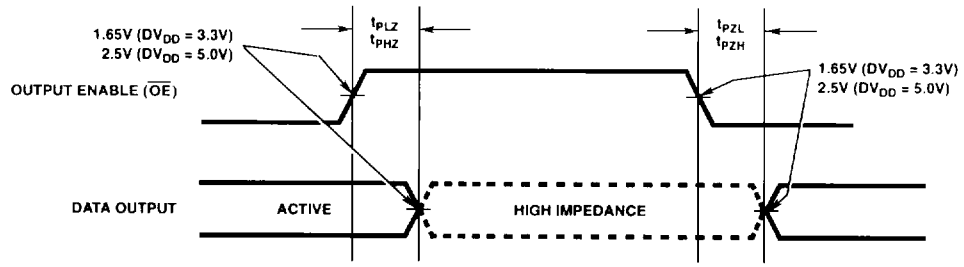


FIGURE 2.

Calibration Timing Diagrams

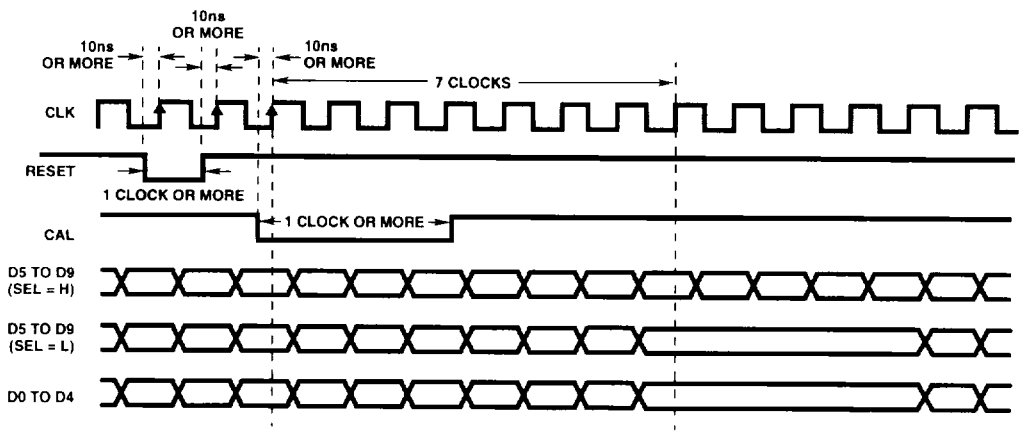


FIGURE 3.

Calibration Timing Diagrams (Continued)

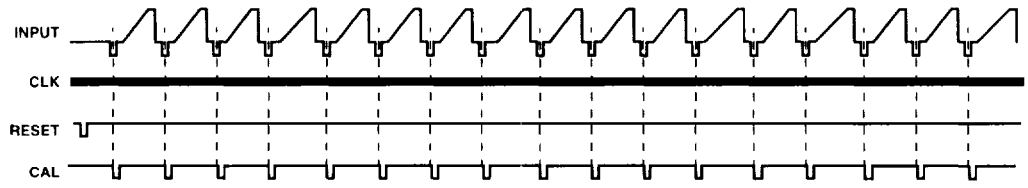


FIGURE 4A. CALIBRATION DURING H SYNC

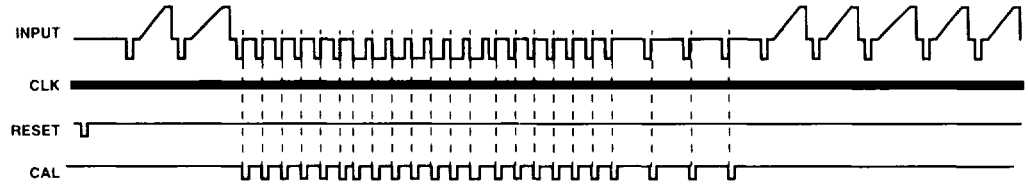


FIGURE 4B. CALIBRATION DURING V SYNC

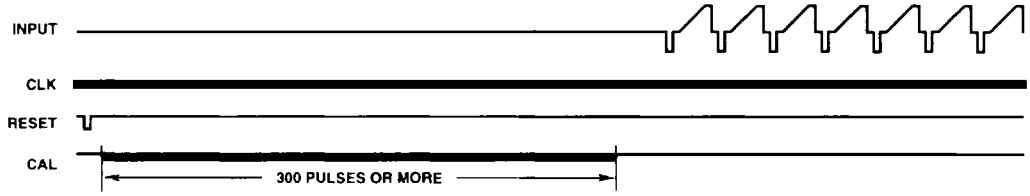


FIGURE 4C. CALIBRATION UPON POWER ON

FIGURE 4. VARIOUS CALIBRATION TIMINGS

Typical Performance Curves

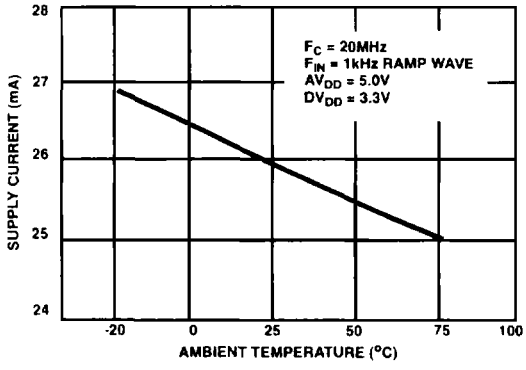


FIGURE 5. SUPPLY CURRENT vs AMBIENT TEMPERATURE

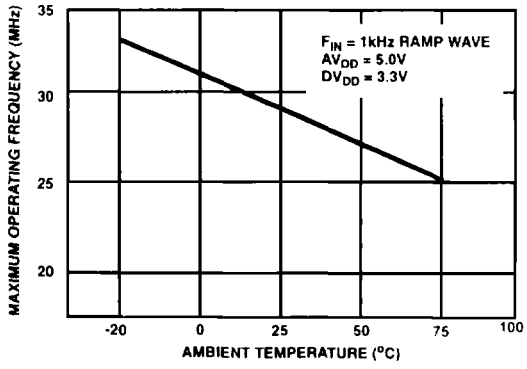


FIGURE 6. MAXIMUM OPERATING FREQUENCY vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

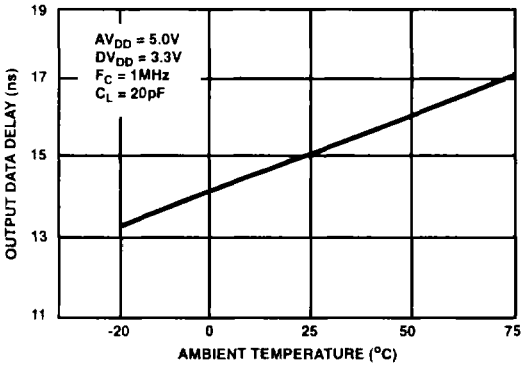


FIGURE 7. OUTPUT DATA DELAY vs AMBIENT TEMPERATURE

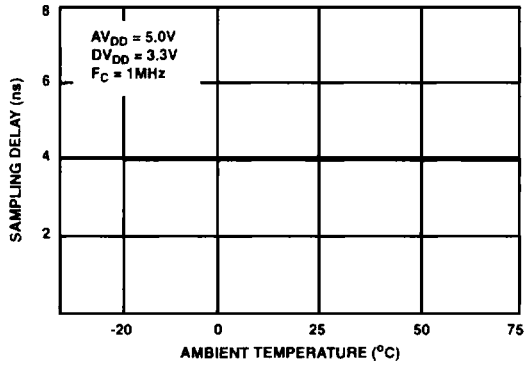


FIGURE 8. SAMPLING DELAY vs AMBIENT TEMPERATURE

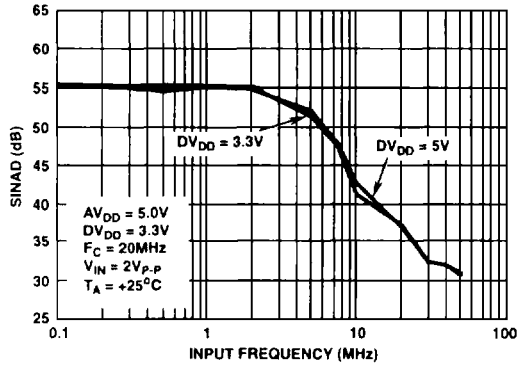


FIGURE 9. SINAD vs INPUT FREQUENCY

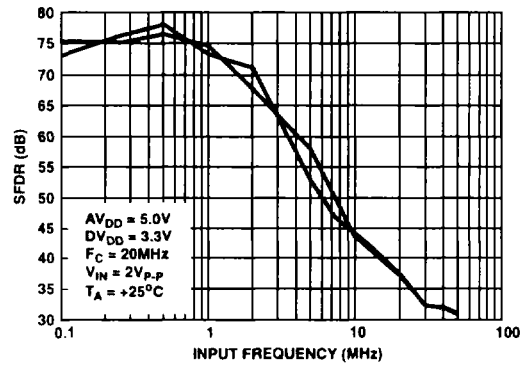


FIGURE 10. SFDR vs INPUT FREQUENCY

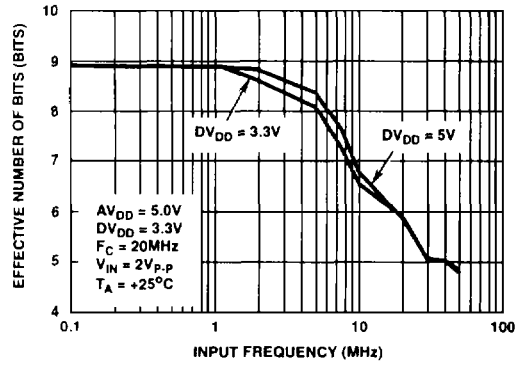


FIGURE 11. EFFECTIVE BITS vs INPUT FREQUENCY

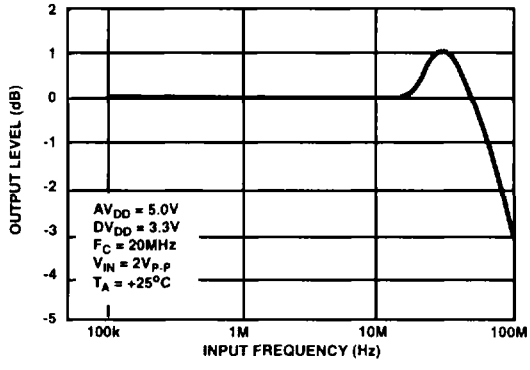


FIGURE 12. INPUT BANDWIDTH

Typical Performance Curves (Continued)

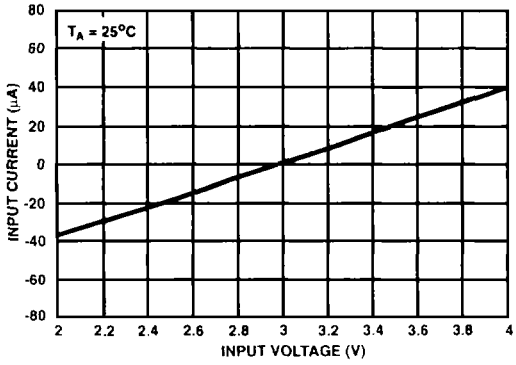


FIGURE 13. ANALOG INPUT CURRENT vs INPUT VOLTAGE

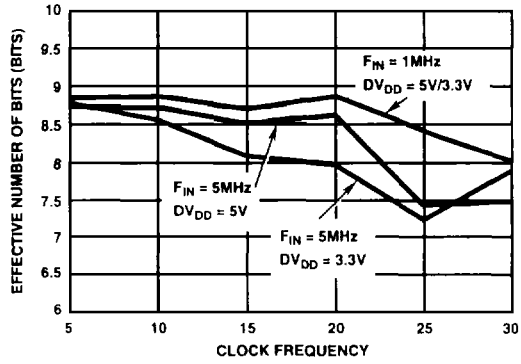


FIGURE 14. ENOB vs CLOCK FREQUENCY

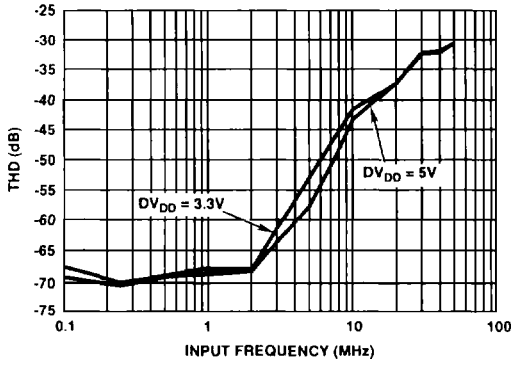


FIGURE 15. THD vs INPUT FREQUENCY

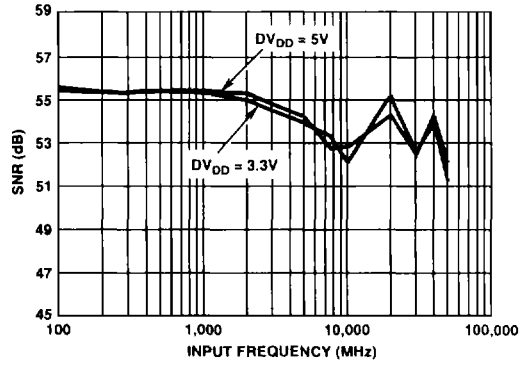
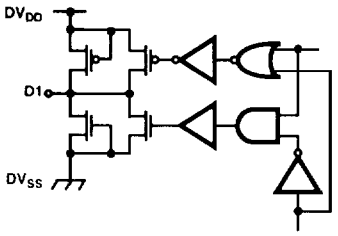
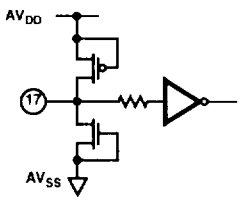
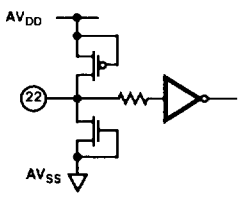
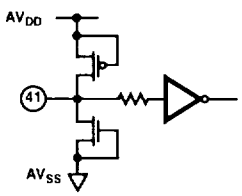
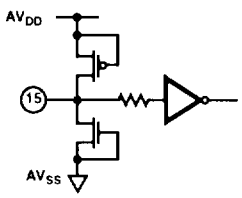
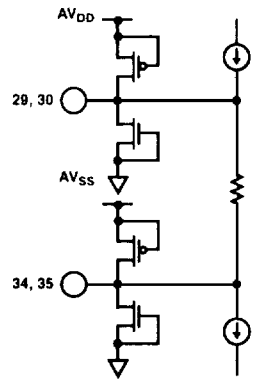
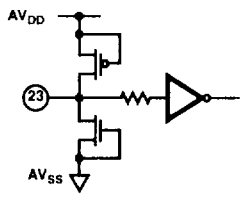
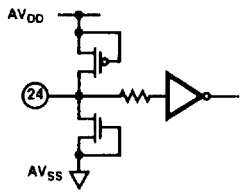
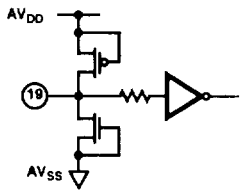


FIGURE 16. SNR vs INPUT FREQUENCY

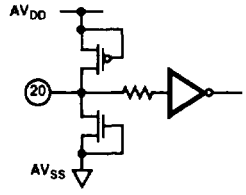
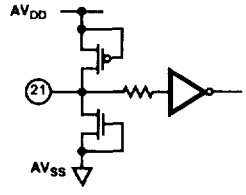
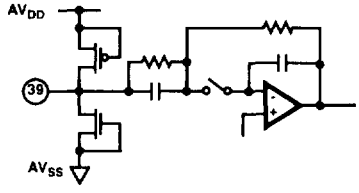
Pin Description and I/O Pin Equivalent Circuit

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 5, 8 to 12	D0 to D9		Digital Outputs: D0 (LSB) to D9 (MSB)
13	TO		Test Pin, Leave Pin Open
7, 45	DV_{DD}		Digital V_{DD}
6, 16, 48	DV_{SS}		Digital V_{SS}
27, 28, 36, 43, 44	AV_{SS}		Analog V_{SS}
17	SEL		D5 to D9 Output Data Select for Calibration (4 CLK) High: Through Output Low: Data Fixed as With D0 to D4
22	CLK		Clock Pin
41	CAL		Calibration Pulse Input, Calibration Starts On a Falling Edge, Normally High
15	RESET		Calibration Circuit Reset, Resets With a Negative Pulse, Normally High

Pin Description and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
14	TIN		Factory Test Signal Input, Normally Tied to AV_{SS} or AV_{DD}
29, 30	VRT		Reference Top, Normally 4.0V
34, 35	VRB		Reference Bottom, Normally 2.0V
38	AT		Factory Test Signal Output, Leave Pin Open
42	TS		Factory Test Signal Input, Tie to AV_{DD}
37	TSTR		Factory Test Signal Input, Tie to AV_{SS} or AV_{DD}
23	$\overline{OE}$		D0 to D9 Output Enable Low: Output's Enabled High: High Impedance State
24	$\overline{CE}$		Chip Enable Low: Active State High: Standby State
19	TESTMODE		Test Mode High: Normal Output State Low: Output fixed

Pin Description and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
20	LINV		Output Inversion High: D0 to D8 are Inverted Low: D0 to D8 are Normal
21	MINV		Output Inversion High: D9 is Inverted Low: D9 is Normal
18, 25, 26	AV_{DD}		Analog V_{DD}
39	V_{IN}		Analog Input

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE										
		MSB										LSB
V_{RT}	1023	1	1	1	1	1	1	1	1	1	1	1
	•					•						
	•					•						
	•					•						
	•											
	512	1	0	0	0	0	0	0	0	0	0	0
	511	0	1	1	1	1	1	1	1	1	1	1
	•					•						
	•					•						
	•					•						
	•											
V_{RB}	0	0	0	0	0	0	0	0	0	0	0	0

NOTE:

1. This table shows the correlation between the analog input voltage and the digital output code. (TESTMODE = 1, MINV and LINV= 0)

OUTPUT DATA FORMAT TABLE

TESTMODE	LINV	MINV	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
1	0	0	N	N	N	N	N	N	N	N	N	N
1	1	0	I	I	I	I	I	I	I	I	I	N
1	0	1	N	N	N	N	N	N	N	N	N	I
1	1	1	I	I	I	I	I	I	I	I	I	I
0	1	1	1	0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1	0	1	0	0
0	1	0	1	0	1	0	1	0	1	0	1	1
0	0	0	0	1	0	1	0	1	0	1	0	1

NOTE:

1. This table shows the output state for the combination of TESTMODE, LINV, and MINV states.
2. N: Non-Inverted Output.
3. I: Inverted Output.

Detailed Description

The HI5710 is a two step A/D converter featuring a 5-bit upper comparator group and a 5-bit lower comparator group. An internal calibration mode is used to improve linearity which is user controlled.

The reference voltage must be supplied externally, with V_{RB} and V_{RT} typically set to 2.0V and 4.0V respectively.

Both chip enable and output enable pins are provided for flexibility and to reduce power consumption. The digital outputs can be inverted by inputs LINV and MINV, where LINV controls outputs D0 through D8 and MINV controls output D9 (MSB). This allows for outputs of various digital formats, such as straight binary, inverted binary, offset two's complement or inverted offset two's complement.

Analog Input

The analog input typically requires a $2V_{P-P}$ full scale input signal. The full scale input can range from 1.8V to 2.8V depending on the reference voltages.

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. Op amps such as the HA5020 should make an excellent input amplifier depending on the applications requirements. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input. Be sure to consider the amplifiers settling time in CCD applications or where step inputs are expected.

Reference Input

The input range of the A/D is set by the voltage difference of V_{RT} and V_{RB}. The HI5710 is designed to use an external reference from 2.0V to 4.0V on V_{RB} and V_{RT}, respectively. The analog input range of the A/D will now be from 2.0V to 4.0V. The V_{RB} range is 1.8V to 2.8V, the V_{RT} range is 3.6V to 4.6V, and (V_{RT} - V_{RB}) range is 1.8V to 2.8V.

V_{RT} and V_{RB} must be decoupled to analog ground to minimize noise on the reference. A 0.1µF capacitor is usually adequate.

Clock Input

The HI5710 samples the input signal on the rising edge of the clock with the digital data latched at the output after 3 clock cycles. The HI5710 is designed to use a 50% duty cycle square wave, but a 10% variation should not affect performance.

The clock input can be driven from +3.3V or +5V TTL or CMOS logic. Be sure not to use +5V logic if the HI5710 digital supply is +3.3V, unless you are sure the input will not exceed the supply voltage. When using a +3.3V digital supply, HC or AC CMOS logic will work well.

Digital Inputs

The digital inputs can be driven from +3.3V or +5V TTL or CMOS logic, except for the $\overline{OE}$ input. The $\overline{OE}$ input should be driven by CMOS logic when using a +5V digital supply though TTL logic may work if not heavily loaded. Be sure not to use 5V logic if the HI5710 digital supply is +3.3V, unless you are sure the input will not exceed the supply voltage. When using a +3.3V digital supply, HC or AC CMOS logic will work well.

Digital Outputs

The digital outputs are CMOS outputs. The LINV input will invert outputs D0 through D8 and MINV will invert output D9 (MSB). This allows the user to set the output for a number of different digital formats. The outputs can also be three-stated by pulling the $\overline{OE}$ input high.

The digital supply can run from +3.3V to +5V. The digital outputs will generate less radiated noise using +3.3V, but the outputs will have less drive capability. The digital outputs will only swing to DV_{DD}, therefore exercise care if interfacing to +5V logic when using a +3.3V supply.

The outputs can also be set to a fixed, defined state, see Output Data Format table. By setting the TESTMODE pin low, the outputs go to a defined digital pattern. This pattern is varied by the MINV and LINV inputs. This feature can be used for in-circuit testing of the digital bus.

Calibration Function

The HI5710 has a built-in calibration circuit to minimize linearity error. The RESET and CAL inputs should be timed as

shown in Figure 4. A setup time of 10ns or longer is required for both the RESET and CAL inputs and they must stay low for at least one clock period.

A negative pulse on the RESET input should occur before the CAL input sees a falling edge. This sets up the initial calibration value. The calibration starts on the rising edge of the clock after the falling edge of the CAL pulse and requires 300 pulses to complete the calibration. The RESET input serves to minimize the calibration time, but it is not mandatory that it be used. The RESET input must remain at a high state when not in use. The calibration, when executed without the RESET pulse, requires 600 calibration pulses.

One calibration cycle is completed in 11 clock cycles. Seven clock cycles after the calibration pulse, the calibration circuit takes exclusive possession of the lower comparators, D0 through D4, for four clock cycles. During this time, the outputs are latched with the previous data (cycle seven data).

The upper 5 bits, D5 through D9, will operate as usual during the calibration if the SEL input is held high, making the HI5710 a 5 bit A/D converter during the last four clock cycles of the calibration. If the SEL input is low, the upper 5 bits are latched with the previous data (cycle seven data) during the last four cycles of the calibration as are the lower 5 bits.

The calibration must be done when the part is first powered up, when the supplies vary more that 100mV or when (V_{RT} - V_{RB}) changes more than 200mV. When first powered up, a minimum of 300 calibration pulses are required after the reset pulse. If no reset pulse is given, then a minimum of 600 calibration pulses are needed. Figure 4 shows several possible calibration timing schemes. It is not necessary to calibrate as often as these figures show, these are only design ideas. The HI5710 application note AN9511 shows a simple circuit for controlling the calibration function.

Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds. Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin. A larger capacitor (1µF to 10µF) should be placed somewhere on the PC board for low frequency decoupling of both analog and digital supplies.

The analog supply should be present before the digital supply to reduce the risk of latch-up. The digital supply can run from +3.3V to +5V. +3.3V generates less radiated noise at the digital outputs, but they have less drive capability. The specifications do not change with digital supply levels. Remember, the digital outs will only swing to DV_{DD}.

Typical Application Circuit

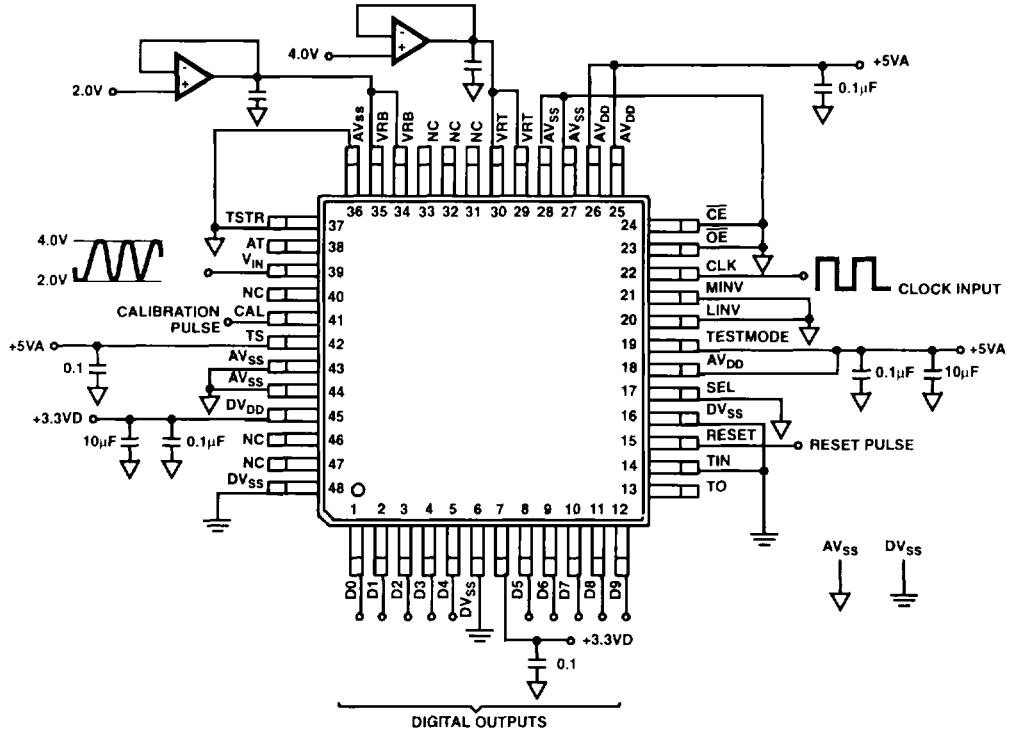


FIGURE 13.

Test Circuits

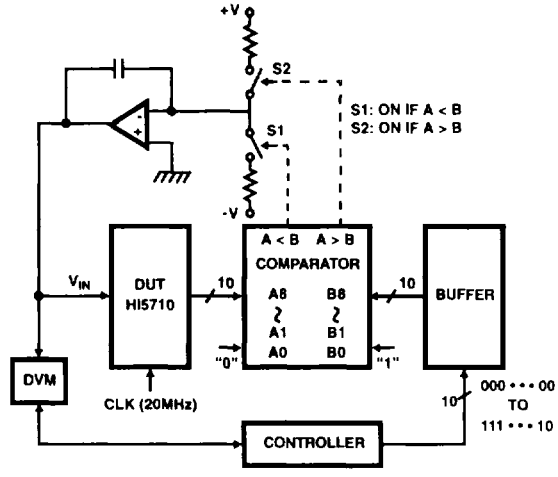


FIGURE 14. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

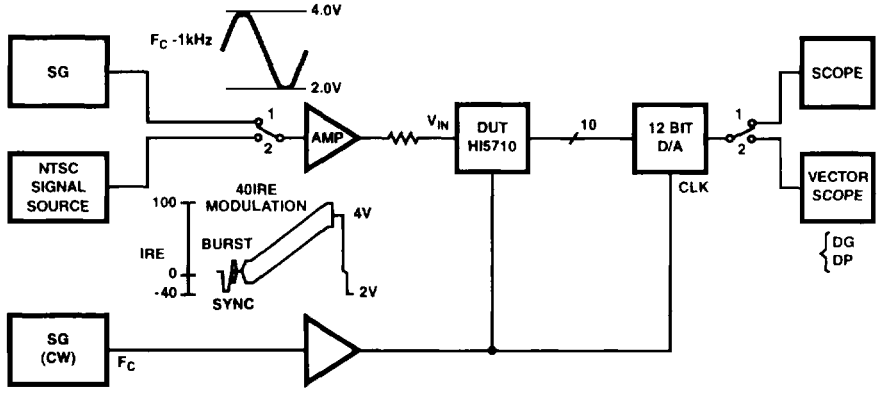


FIGURE 15. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

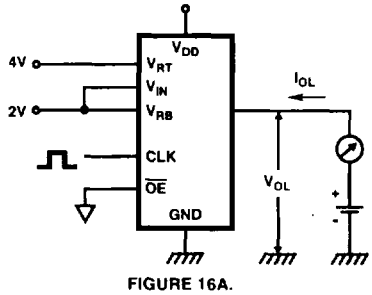


FIGURE 16A.

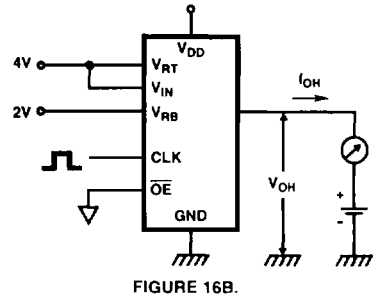


FIGURE 16B.

FIGURE 16. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Timing Definitions

Aperture Delay - Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter - This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Latency - After the analog sample is taken, the data on the bus is output at 3rd cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 3 cycles.

Power-up initialization - This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize some dynamic circuits within the converter.

Static Performance Definitions

Offset, full-scale, and gain all use a measured value of the external voltage reference to determine the ideal plus and minus full-scale values. The results are all displayed in LSBs.

Offset Error (V_{OS}) - The first code transition should occur at a level 1/2 LSB above the negative full-scale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full-Scale Error (FSE) - The last code transition should occur for a analog input that is 1 and 1/2 LSBs below positive full-scale. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL) - DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed for no missing codes over all temperature ranges.

Integral Linearity Error (INL) - INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection (PSRR) - Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error is noted. The number reported is the percent change in these parameters versus full-scale divided by the percent change in the supply.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5710. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 2048 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full-scale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR) - SNR is the measured rms signal to rms noise at a specified input and sampling frequency. The noise is the rms sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD) - SINAD is the measured rms signal to rms sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB) - The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5dB$

2nd and 3rd Harmonic Distortion - This is the ratio of the rms value of the 2nd and 3rd harmonic component respectively to the rms value of the measured input signal.

Transient Response - Transient response is measured by inputting a step to the input to the part and measuring the number of cycles it takes for the output code to settle within a defined accuracy.

Overvoltage Recovery - Overvoltage Recovery is measured by inputting a step, which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within a defined accuracy.

Full Power Input Bandwidth - Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

HFA1135	HI5710	HSP9501	HI1171	HA5020
HFA1245	HI5702	HSP48410	CA3338	HA2842
HA5020		HSP48908	HI3050	HFA1115
		HSP48212		
		HSP43891		
		HSP43168		
		HSP43216		

HFA1135: 350MHz Op Amp with Output Limiting
HFA1245: Dual 350MHz Op Amp with Disable/Enable
HA5020: 100MHz Video Op Amp
HI5710: 10-Bit 20 MSPS A/D Converter
HI5702: 10-Bit 40 MSPS A/D Converter
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI1171: 8-Bit 40MHz Video D/A Converter
CA3338: 8-Bit 50MHz Video D/A Converter
HI3050: Triple 10-Bit 50MHz Video DAC
HA2842: High Output Current, Video Op Amp
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 16. 10-BIT VIDEO IMAGING COMPONENTS

HFA3600	HI5710	HSP43168	HI5721	HFA1115
HFA3102	HI5702	HSP43216	HI20201	
HFA3101		HSP43891	HI20203	
HFA1100		HSP50016		
		HSP50110		
		HSP50210		

HFA3600: Low Noise Amplifier/Mixer
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3101: Gilbert Cell Transistor Array
HFA1100: 850MHz Op Amp
HI5710: 10-Bit 20 MSPS A/D Converter
HI5702: 10-Bit 40 MSPS A/D Converter
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit 100MHz Communications D/A Converter
HI20201: 10-Bit 160MHz High Speed D/A Converter
HI20203: 8-Bit 160MHz High Speed D/A Converter
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 17. 10-BIT COMMUNICATIONS COMPONENTS