

PI3WVR12612

HDMI 2.0, DisplayPort 1.2 Video Switch

Features

- 4-lane, 1:2 mux/demux that will support RBR, HBR1, or HBR2
- Data rate: 3.4 Gbps to 6.0 Gbps for high data channels
- 1-channel 1:2 mux/demux for HPD signal
- Differential switch matrix for DP AUX and HDMI DDC
- Supports 720 Mbps high-speed DP AUX
- -2.0 dB Insertion Loss for Dx channels @ 3 GHz
- -3 dB Bandwidth for Dx channels: 4.1 GHz
- Return loss for Dx channels @ 3 GHz: -12 dB
- Low Crosstalk for high speed channels: -25 dB@ 6 Gbps
- Low Off Isolation for high speed channels: -24 dB@ 6 Gbps
- Low channel-to-channel skew, 35ps max
- Low Bit-to-Bit Skew, 5ps typ (between '+' and '-' bits)
- V_{DD} Operating Range: 3.3 V +/-10%
- ESD Tolerance: 2kV HBM
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
 - 52-pin TQFN (ZL)

Description

Diodes' PI3WVR12612 is a multi-standard video switch with wide voltage range capability. It supports DisplayPort 1.2, HDMI 2.0, and emerging and proprietary standards.

PI3WVR12612 can pass high-speed signals up to 1.2 V peak-to-peak differential with a common-mode voltage from 0 to 3.4 V. The wide voltage range allows DC-coupled multi-standard operation. Eliminating AC coupling capacitors saves board space and improves signal integrity for dense PCB designs.

The high speed channels can also pass 0 V to 3.3 V CMOS signals up to 1 MHz.

In addition to four high-speed lanes, PI3WVR12612 also switches AUX, DDC, and HPD signals.

Application

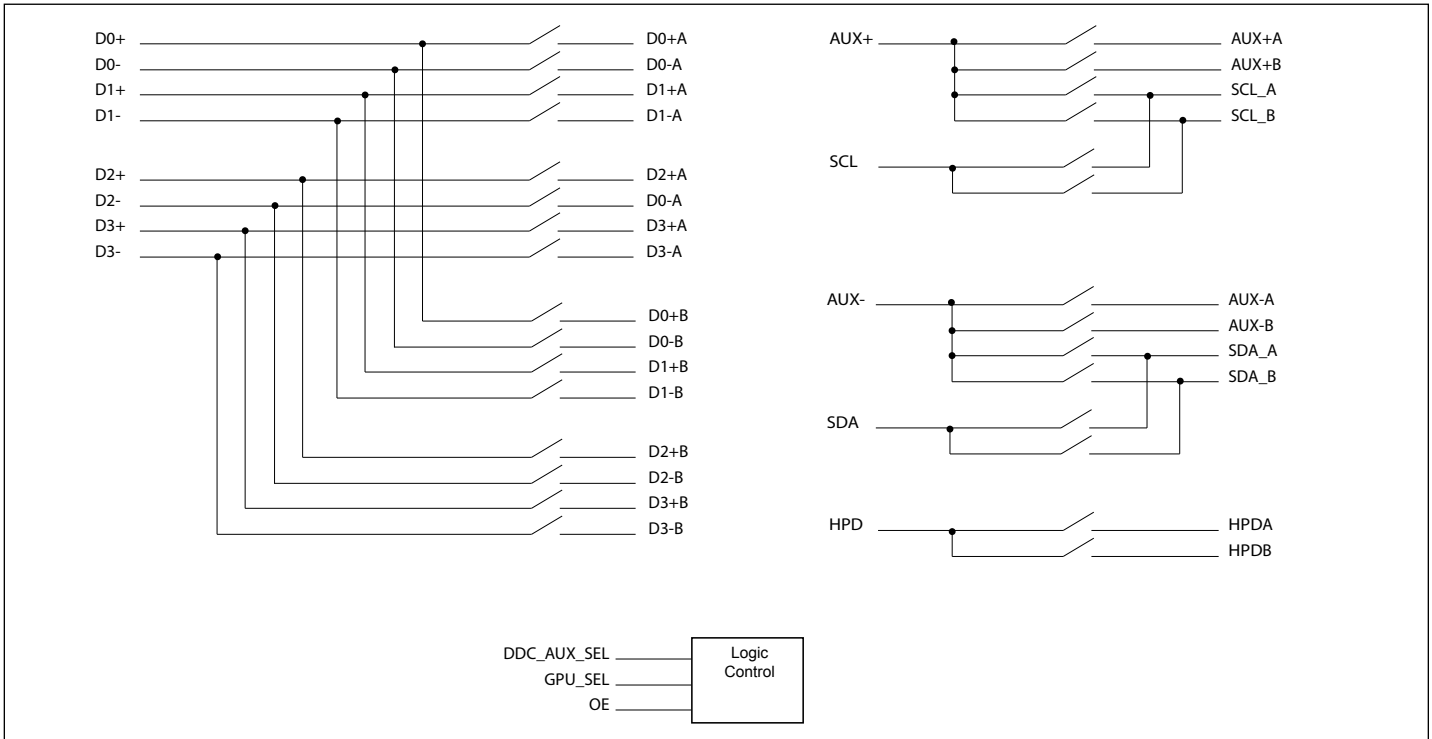
- Routing of DisplayPort and HDMI signals with low signal attenuation between source and sink.

Notes:

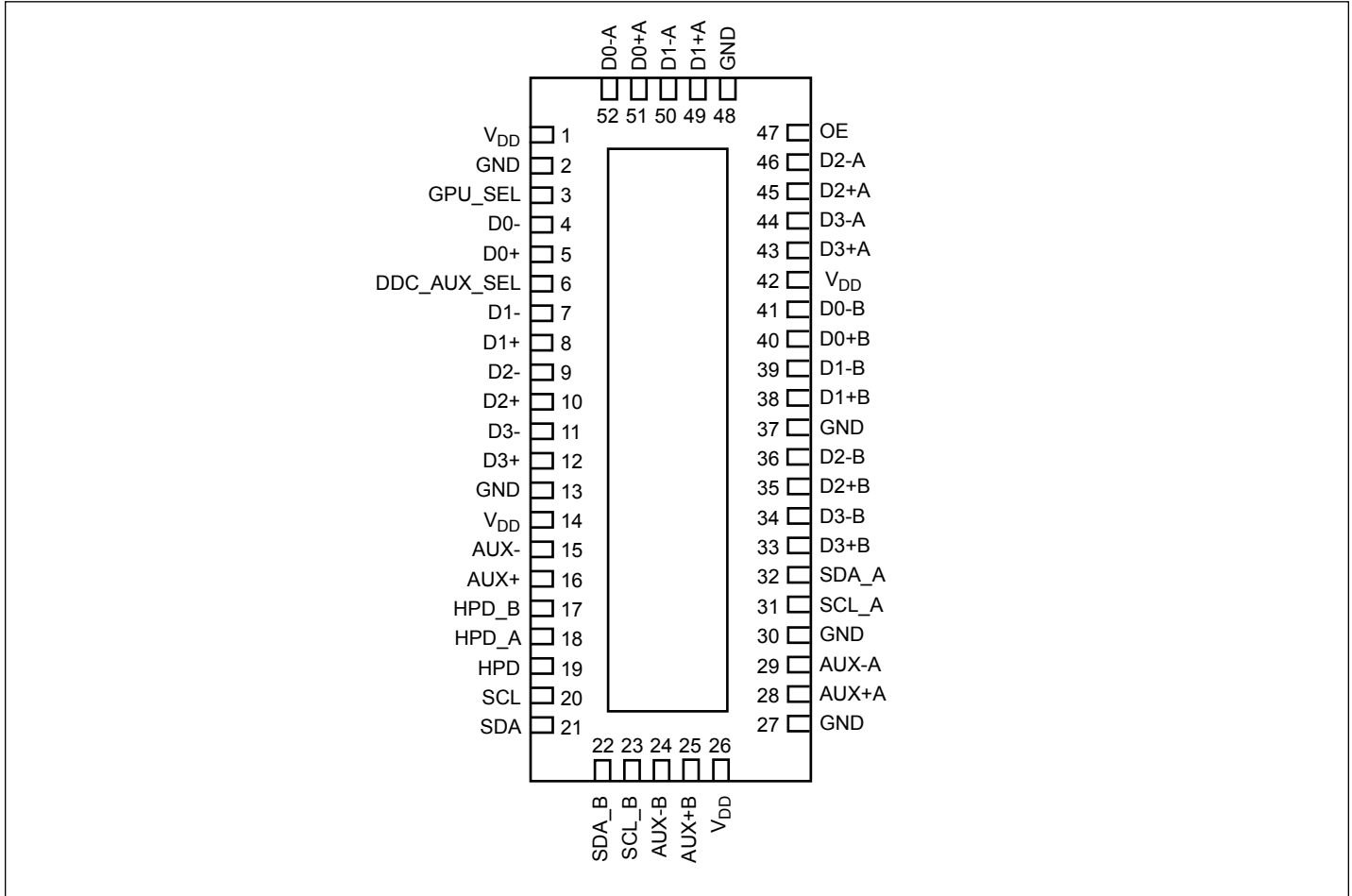
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

PI3WVR12612

Block Diagram



Pin Configuration



Truth Table

Control			Switch Function			
OE	GPU_SEL	DDC_AUX_SEL	D0-D3	AUX	HPD	DDC
High	Low	Low	A	AUX A	HPD A	Hi-Z
High	High	Low	B	AUX B	HPD B	Hi-Z
High	Low	High	A	DDC A	HPD A	Hi-Z
High	High	High	B	DDC B	HPD B	Hi-Z
High	Low	Medium	A	AUX A	HPD A	DDC A
High	High	Medium	B	AUX B	HPD B	DDC B
Low	x	x	Hi-Z	Hi-Z	Hi-Z	Hi-Z

- Medium level = 1/2 V_{DD} = 1.65V. To set this level, need to have external pull up/pull down resistors.

Pin Description

Pin#	Pin Name	Signal Type	Description
3	GPU_SEL	I	Switch logic control
4	D0-	I/O	Negative differential signal 0 for COM port
5	D0+	I/O	Positive differential signal 0 for COM port
7	D1-	I/O	Negative differential signal 1 for COM port
8	D1+	I/O	Positive differential signal 1 for COM port
9	D2-	I/O	Negative differential signal 2 for COM port
10	D2+	I/O	Positive differential signal 2 for COM port
11	D3-	I/O	Negative differential signal 3 for COM port
12	D3+	I/O	Positive differential signal 3 for COM port
15	AUX-	I/O	Negative differential signal for AUX COM port
16	AUX+	I/O	Positive differential signal for AUX COM port
19	HPD	I/O	HPD for COM port
18	HPD_A	I/O	HPD for port A
17	HPD_B	I/O	HPD for port B
25	AUX+B	I/O	Positive differential signal for AUX, port B
24	AUX-B	I/O	Negative differential signal for AUX, port B
28	AUX+A	I/O	Positive differential signal for AUX, port A
29	AUX-A	I/O	Negative differential signal for AUX, port A
33	D3+B	I/O	Positive differential signal 3 for port B
34	D3-B	I/O	Negative differential signal 3 for port B
35	D2+B	I/O	Positive differential signal 2 for port B
36	D2-B	I/O	Negative differential signal 2 for port B
38	D1+B	I/O	Positive differential signal 1 for port B
39	D1-B	I/O	Negative differential signal 1 for port B
40	D0+B	I/O	Positive differential signal 0 for port B
41	D0-B	I/O	Negative differential signal 0 for port B
43	D3+A	I/O	Positive differential signal 3 for port A
44	D3-A	I/O	Negative differential signal 3 for port A
45	D2+A	I/O	Positive differential signal 2 for port A
46	D2-A	I/O	Negative differential signal 2 for port A
49	D1+A	I/O	Positive differential signal 1 for port A
50	D1-A	I/O	Negative differential signal 1 for port A
51	D0+A	I/O	Positive differential signal 0 for port A
52	D0-A	I/O	Negative differential signal 0 for port A
6	DDC_AUX_SEL	I	Switch logic control
23	SCL_B	I/O	DDC_clock channel for port B

Pin Description Cont.

Pin#	Pin Name	Signal Type	Description
31	SCL_A	I/O	DDC_clock channel for port A
22	SDA_B	I/O	DDC_data channel for port B
32	SDA_A	I/O	DDC_data channel for port A
20	SCL	I/O	DDC_clock channel for COM port
21	SDA	I/O	DDC_data channel for COM port
47	OE	I	Output enable. If OE is high, IC is enabled. If OE is low, then IC is power down and all I/Os are hi-z
1, 14, 26, 42	VDD	Power	3.3V +/-10% power supply
2, 13, 27, 30, 37, 48	GND	Ground	Ground

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Junction Temperature (Tj)	125°C
Supply Voltage to Ground Potential	-0.5V to +4.2V
DC Input Voltage	-0.5V to V _{DD}
High Speed Data Channel.....	-0.5V to 3.8V
HPD_x, SDA_x, SCL_x	-0.5V to 5.5V
DC Output Current	120mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for Switching over Operating Range

(T_A = -40°C to +105°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units
V _{IH}	Input HIGH Voltage (OE, GPU_SEL)	Guaranteed HIGH level	1.5			V
V _{IL}	Input LOW Voltage (OE, GPU_SEL)	Guaranteed LOW level			0.75	
V _{IH}	Input HIGH Voltage (DDC_AUX_SEL)	Guaranteed HIGH level	2.65		V _{DD}	
V _{IM}	Input Mid-Level Voltage (DDC_AUX_SEL)	Guaranteed MID level	V _{DD} /2-300mV	V _{DD} /2	V _{DD} /2+300mV	
V _{IL}	Input LOW Voltage (DDC_AUX_SEL)	Guaranteed LOW level	-0.5		0.6	
V _{IK}	Clamp Diode Voltage (HS Channel)	V _{DD} = Max., I _{IN} = -18mA		-1.6V	-1.8	μA
V _{IK}	Clamp Diode Voltage (Aux, Cntrl)	V _{DD} = Max., I _{IN} = -18mA		-0.7	-1.5	
I _{IH}	Input HIGH Current (All Control Pins)	V _{DD} = Max., V _{IN} = V _{DD}			±5	
I _{IL}	Input LOW Current (All Control Pins)	V _{DD} = Max., V _{IN} = GND			±5	μA
I _{OFF_SB}	I/O leakage when part is off for sideband signals only (DDC, AUX, HPD)	V _{DD} = 0V, V _{INPUT} = 0V to 3.6V			20	
R _{ON_HS}	On resistance between input to output for high speed signals	V _{INPUT,cm} = 0V to 3.4V, V _{INPUT,diff} < 1.2V _{p-p,diff} , V _{DD} = 3.0V, I _{INPUT} = 20mA		11		Ω
R _{ON_AUX}	On resistance between input to output for side-band signals (AUX)	V _{DD} = 3.0V, V _{INPUT} = 0 to 3.3V, I _{INPUT} = 20mA		7		Ω
R _{ON_DDC}	On resistance between input to output for DDC channel	V _{DD} = 3.0V, V _{INPUT} = 0V, I _{INPUT} = 20mA		12		Ω
R _{ON_HPD}	On resistance between input to output for HPD channel	V _{DD} = 3.0V, V _{INPUT} = 0 to 3.0V, I _{INPUT} = 20mA		7		Ω
V _{AUX_SS}	Signal Swing Tolerance in Aux path	V _{DD} = 3.0V	-0.5		5.5	V
V _{HPD_I}	Input voltage on HPD path				5.5	V
V _{HPD_O}	Output voltage tolerance on HPD path	HPD input from 3.3V to 5.25V		3.3	3.6	V
V _{SDA_X}	Input Voltage on SDA path			5		V
V _{PASS} (SDA_X)	Switch output voltage tolerance input	V _{in} = 5.25V, I _i = 100μA, V _{DD} = 3.3V	1.8	2.2	2.5	V

DC Electrical Characteristics for Switching over Operating Range Cont.

Parameter	Description	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units
V _{SCL_X}	Input Voltage on SCL path			5		V
V _{PASS} (SCL_X)	Switch output voltage tolerance input	V _{IN} = 5.25V, I _i = 100uA, V _{DD} = 3.3V	1.8	2.2	2.5	V

Power Supply Characteristics (T_A = -40°C to +105°C)

Parameter	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
I _{DD}	Power Supply Current	V _{DD} = 3.3V, V _{IN} = GND or V _{DD}		1	3	mA
I _{DD,Off}	Power Supply Current, Disabled	V _{DD} = 3.3V, V _{IN} = GND or V _{DD} , V _{OE} < V _{IL}		1	50	μA

Note:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics over Operating Range (T_A = -40° to +105°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
X _{TALK}	Crosstalk on High Speed Channels	See Fig. 1 for Measurement Setup	f = 3.0 GHz	-25	-22	dB
			f = 2.7 GHz	-28	-25	
			f = 1.35 GHz	-32	-28	
O _{IRR}	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup	f = 3.0 GHz	-24	-20	dB
			f = 2.7 GHz	-25	-22	
			f = 1.35 GHz	-30	-27	
I _{LOSS}	Differential Insertion Loss on High Speed Channels	@6.0Gbps (see figure 4)	-2.3	-2.0	dB	
		@5.4Gbps (see figure 3)	-2.0	-1.8		
R _{loss}	Differential Return Loss on high speed channels	@3.0GHz (6.0Gbps)		-12	-11	dB
		@2.7GHz (5.4Gbps)		-14	-12.5	
BW _{Dx±}	Bandwidth -3dB for Main high speed path (Dx±)	See figure 3	3.7	4.1		GHz
BW _{AUX/HPD}	-3dB BW for AUX, DDC, and HPD signals	See figure 3	1.35	1.5		GHz

Note:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

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Switching Characteristics ($T_A = -40^\circ$ to $+105^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 10\%$)

Parameter	Description	Min.	Typ.	Max.	Units
T_{pd}	Propagation delay (input pin to output pin) on $Dx\pm$ channels		80		ps
tb-b	Bit-to-bit skew within the same differential pair of $Dx\pm$ channels		5	7	ps
tch-ch	Channel-to-channel skew of $Dx\pm$ channels			35	ps
Tsw a-b	Time it takes to switch from port A to port B			0.1	us
Tsw b-a	Time it takes to switch from port B to port A			0.1	us
Tstartup	Vdd valid to channel enable			10	us
Twakeup	Enabling output by changing OE from low to High			10	us

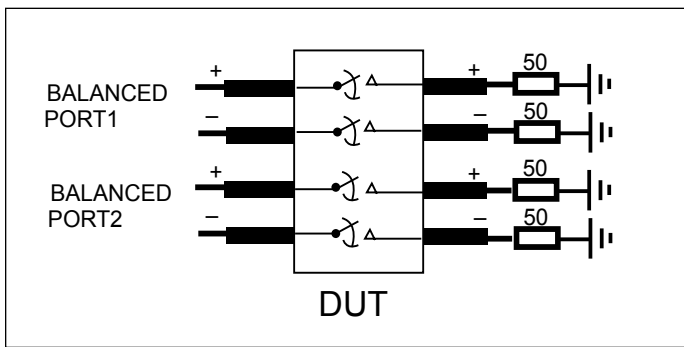


Figure 1. Crosstalk Setup

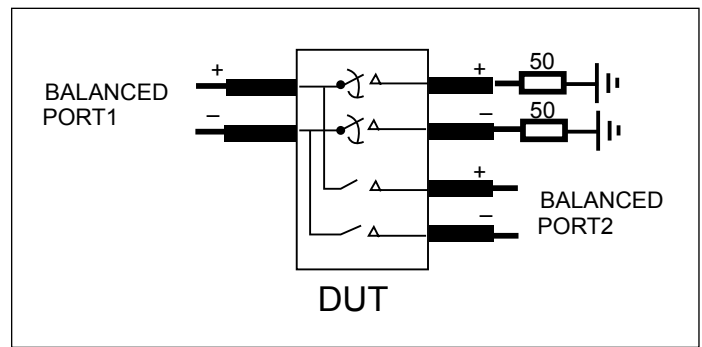


Figure 2. Off-isolation setup

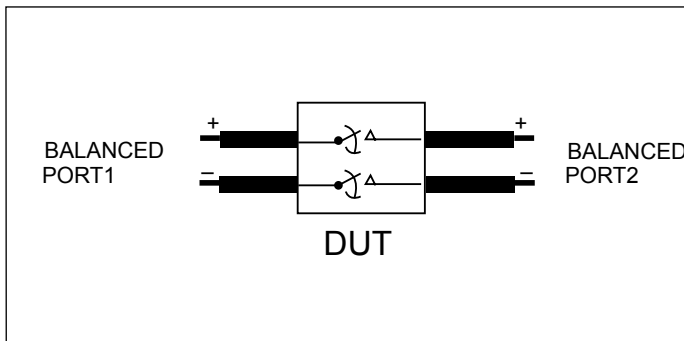
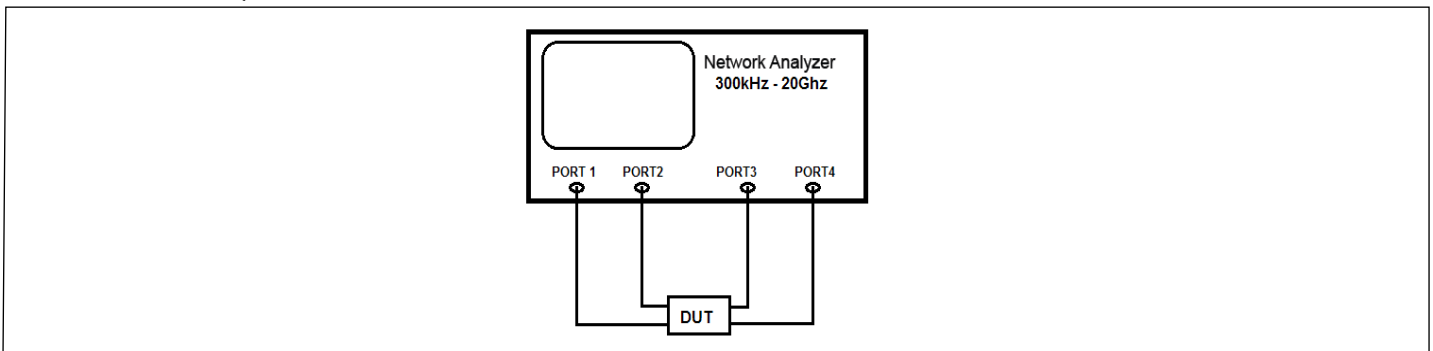


Figure 3. Differential Insertion Loss

Test Circuit for Dynamic Electrical Characteristics



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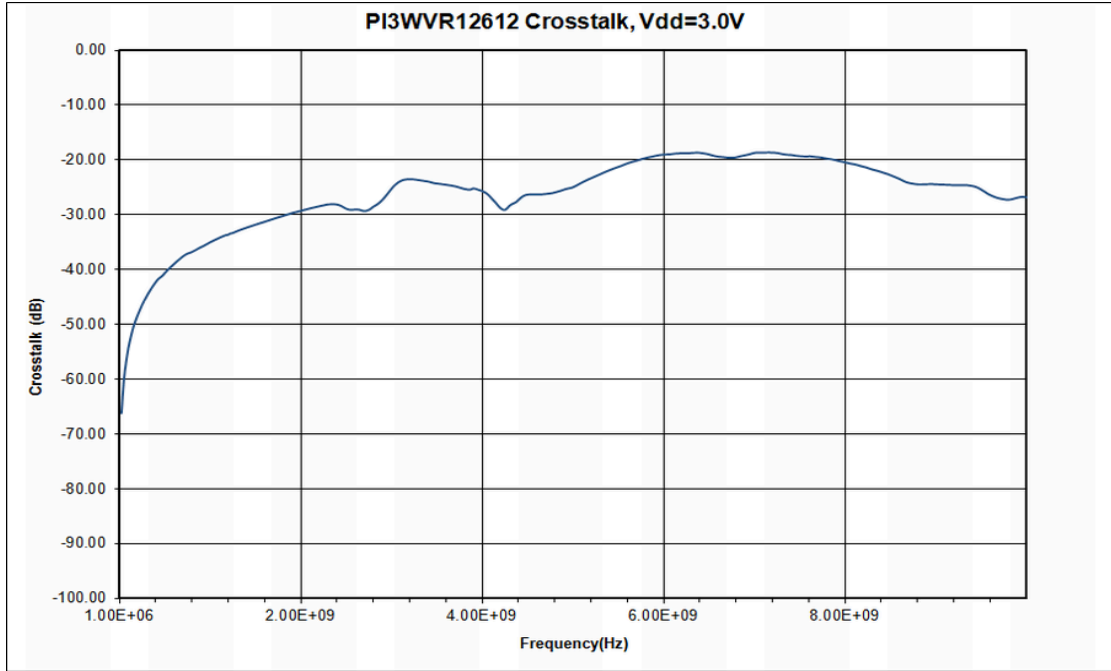


Figure 4. Crosstalk

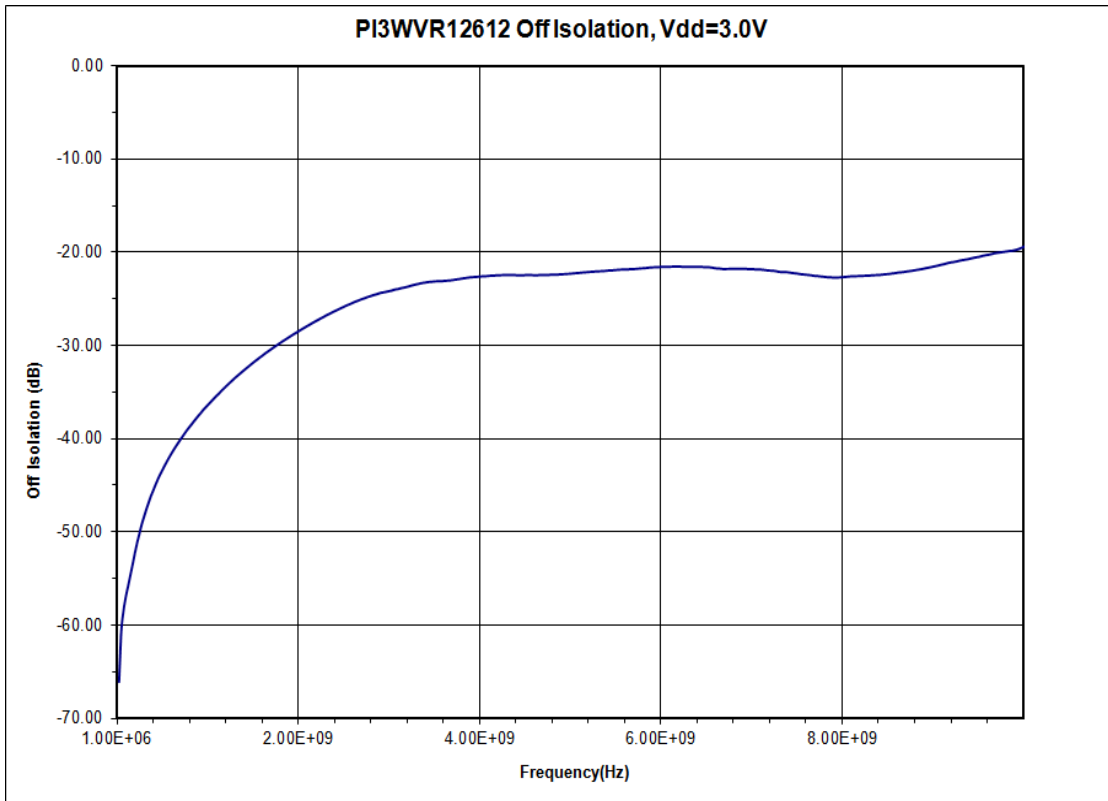


Figure 5. Off Isolation

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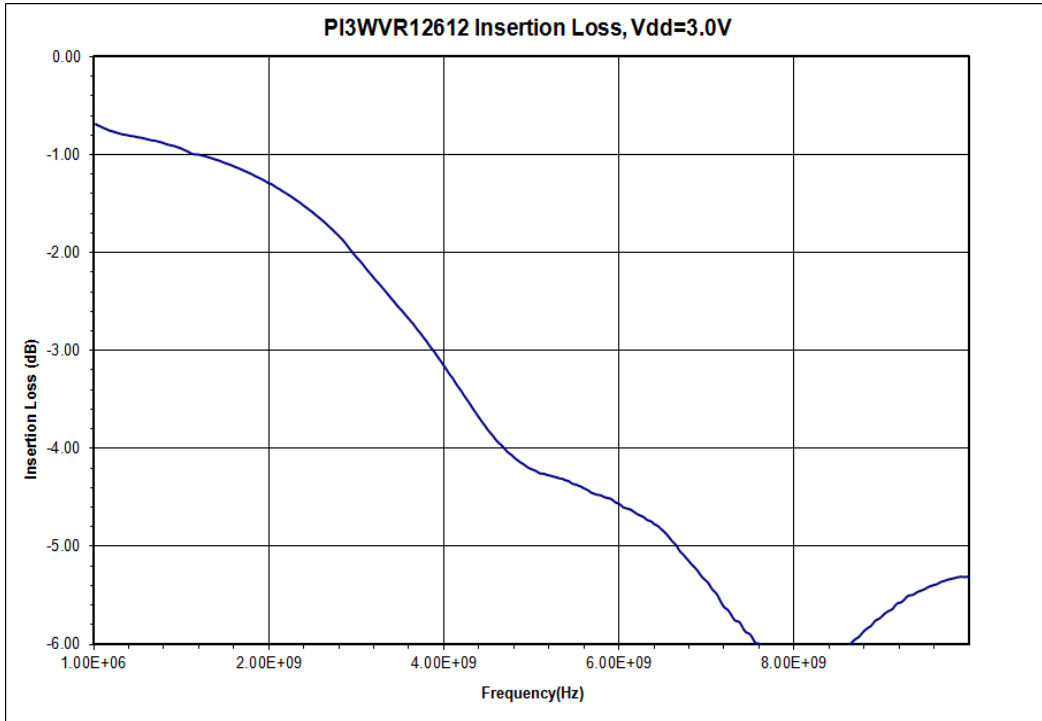


Figure 6. Insertion Loss

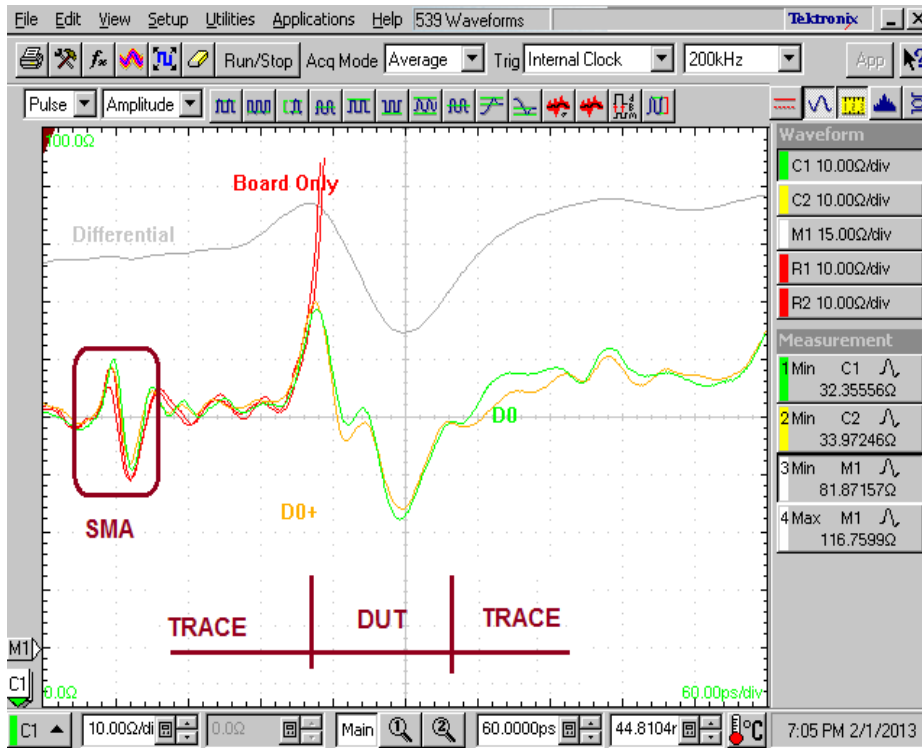


Figure 7. TDR Channel D0, VDD= 3.0V, 25°C

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Data Rate=2.7Gbps

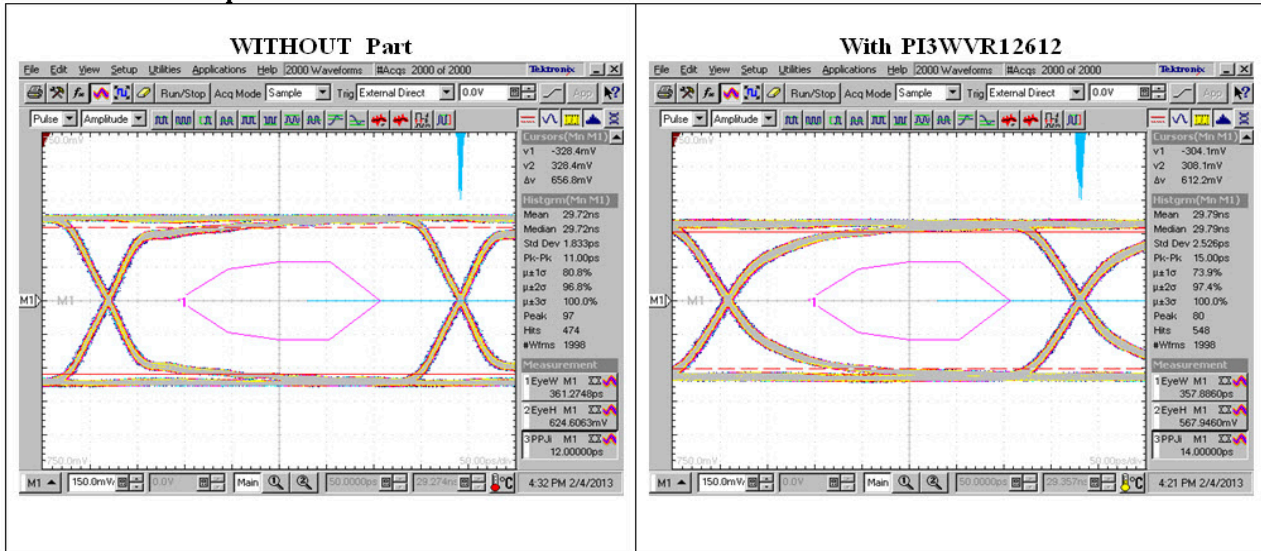


Figure 8. Differential output Eye at Input signal is a 2^7-1 PRBS, Vdd=3.0V, 25°C, Input swing is 800mV differential

Data Rate=5.4Gbps

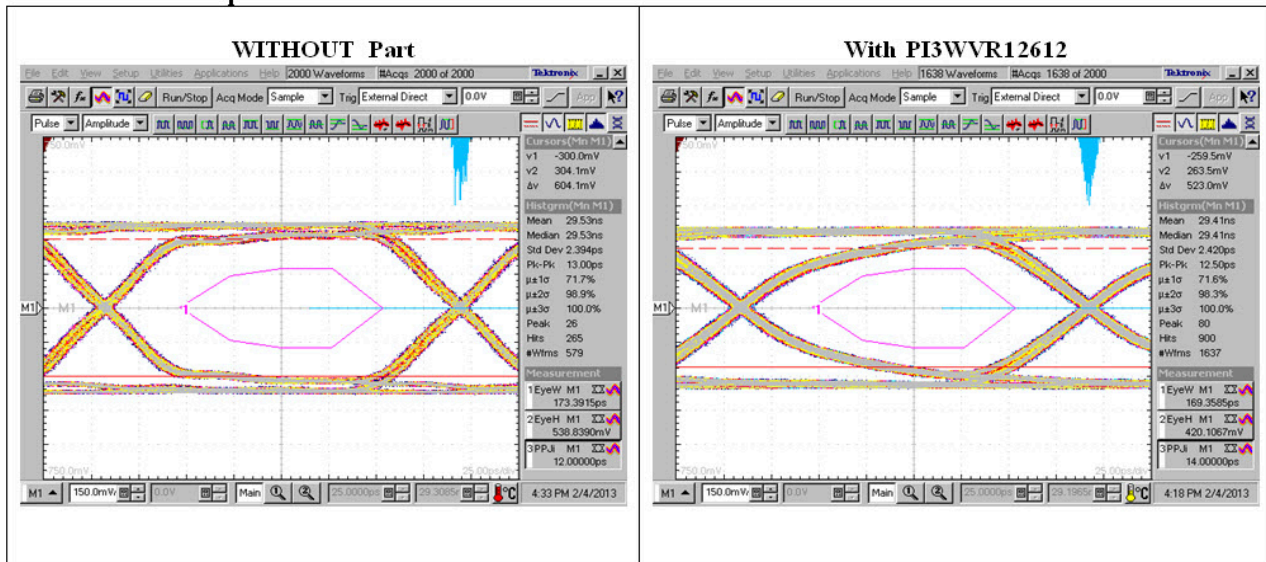
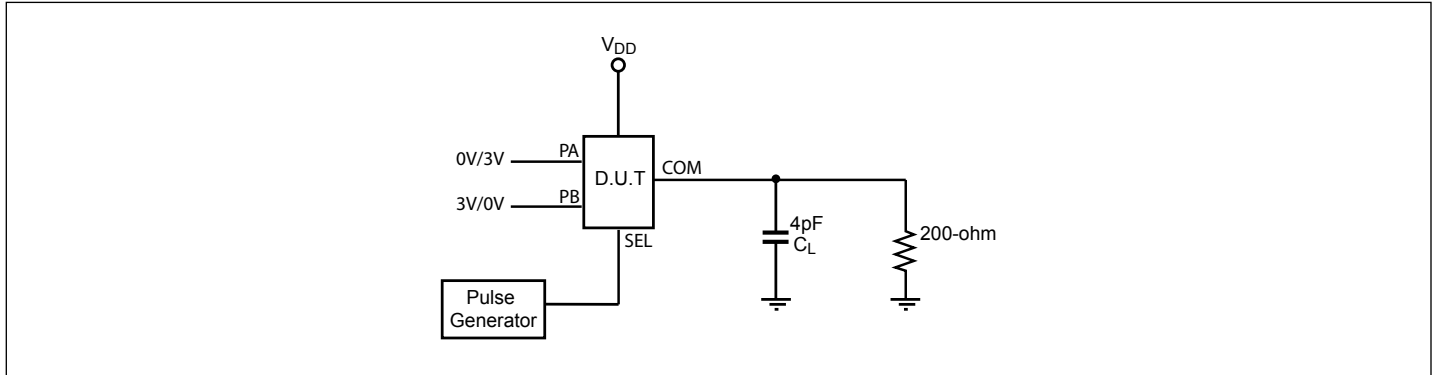


Figure 9. Differential output Eye at Input signal is a 2^7-1 PRBS, Vdd=3.0V, 25°C, Input swing is 800mV differential

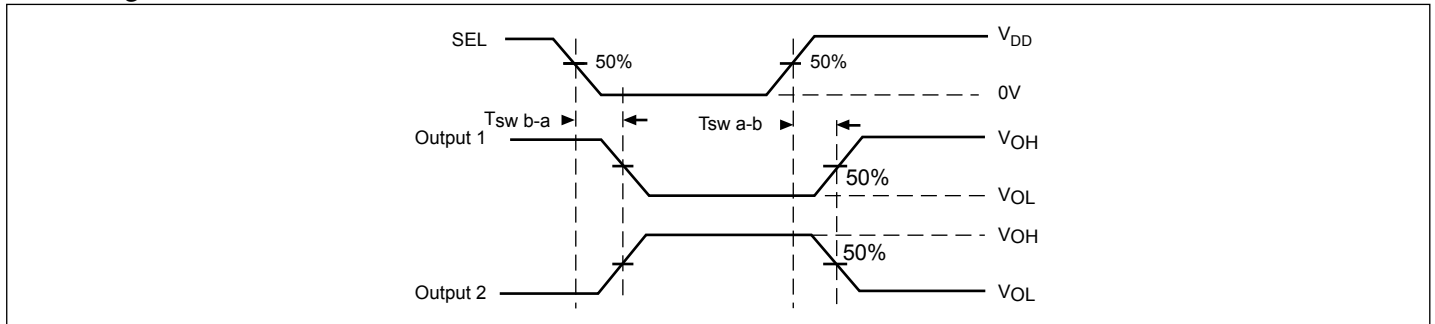
Test Circuit for Electrical Characteristics



Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. All input impulses are supplied by generators having the following characteristics: $PRR \leq \text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.5\text{ns}$, $t_F \leq 2.5\text{ns}$.
4. The outputs are measured one at a time with one transition per measurement.

Switching Waveforms



Voltage Waveforms Enable and Disable Times

Test Condition

Output 1 Test Condition	Output 2 Test Condition
PA = Low	PA = High
PB = High	PB = Low

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Part Marking

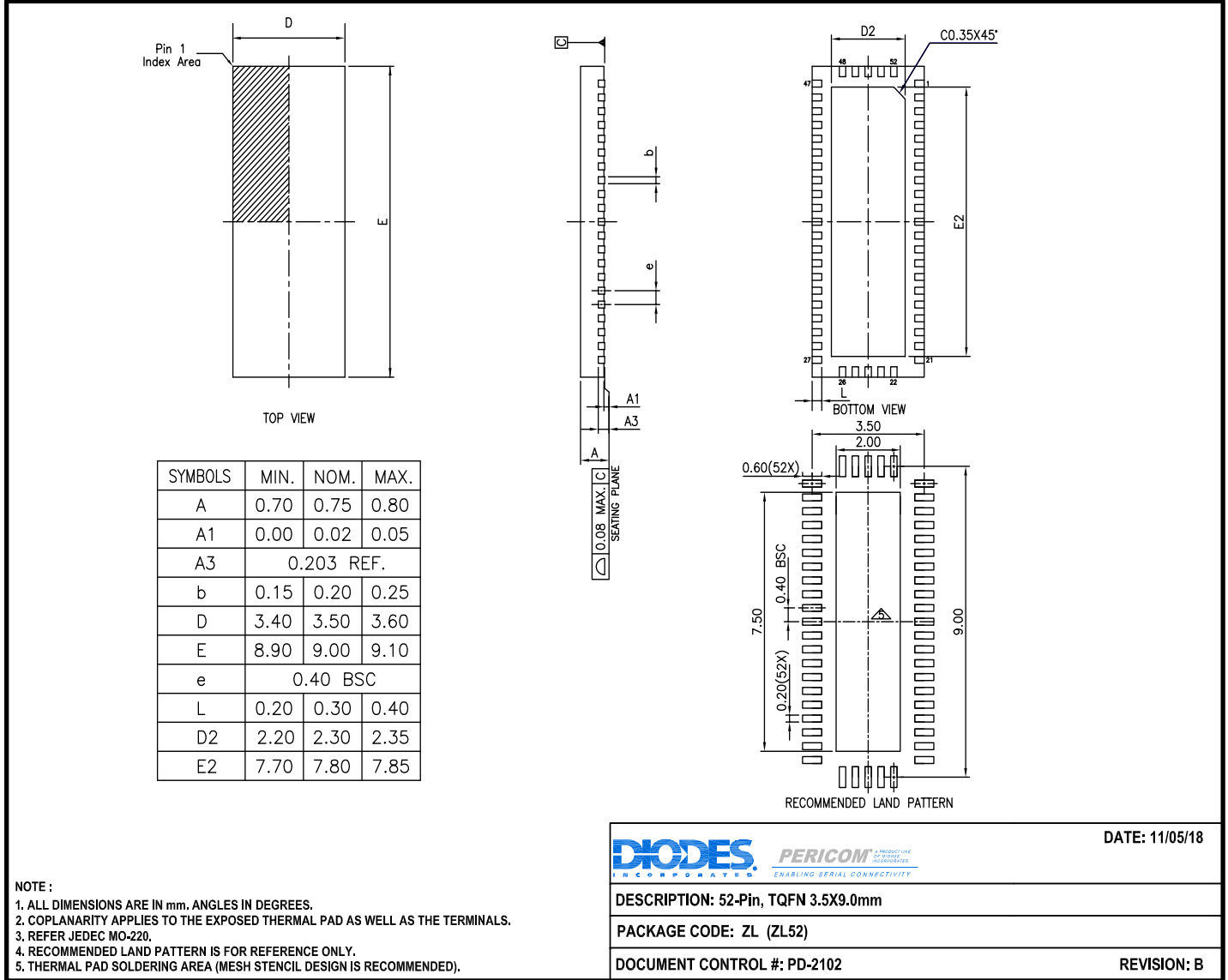


PI3WVR
12612ZLE
ZYYWWXX

Z: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Site Code
2nd X: Fab Code

Packaging Mechanical

52-TQFN (ZL)



For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Description
PI3WVR12612ZLEX	ZL	52-Pin, 3.5 x 9.0 mm (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
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4. E = Pb-free and Green
5. X suffix = Tape/Reel

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