PI3VDP612-A

4-Lane DisplayPort™ Rev 1.1a Compliant Switch with Triple Control Logic for Fast Switching

Features

- 4-lane, 1:2 mux/demux that will support 2.7Gbps or 1.62Gbps DP rev 1.1a signals
- 1-channel 1:2 mux/demux for DP_HPD signal
- 1-differential channel 1:2 mux/demux for DP_Aux signal
- Insertion Loss for high speed channels @ 2.7 Gbps: -1.5dB
- -3dB Bandwidth for high speed channels of 3.25 Ghz
- Low Bit-to-Bit Skew , 7ps max (between '+' and '-' bits)
- Low Crosstalk for high speed channels: -33dB@2.7 Gbps
- Low Off Isolation for high speed channels: -26dB@2.7 Gbps
- V_{DD} Operating Range: 3.3V ±10%
- ESD Tolerance: +/-8kV contact on Ports A and B per IEC61000-4-2 Specification
- Low channel-to-channel skew, 35ps max
- Packaging (Pb-free & Green):
  - -56 TQFN (ZFE)
  - -42 TQFN (ZHE)

Description

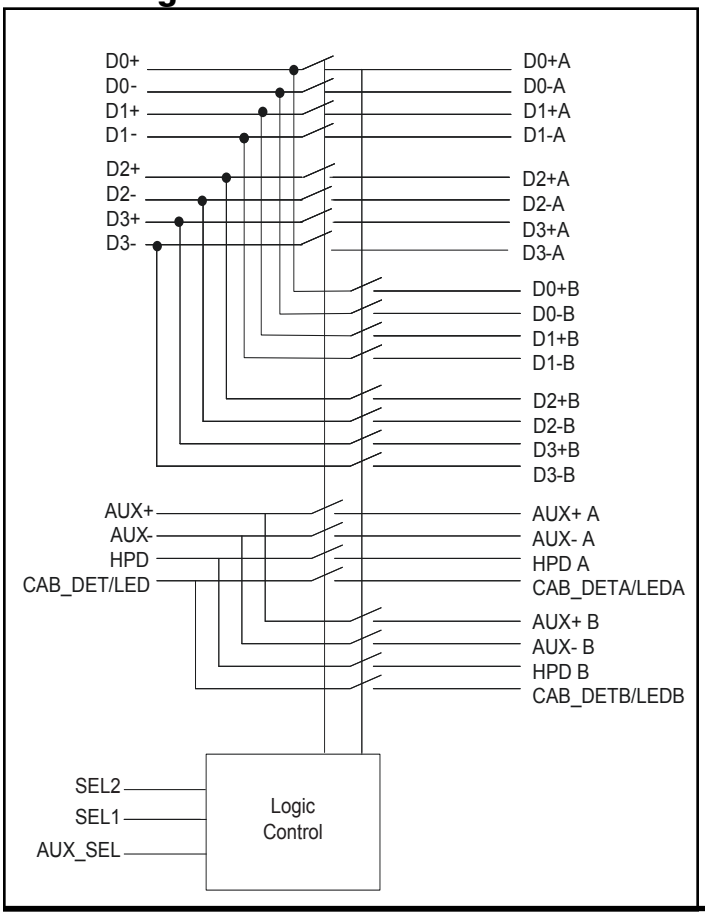
Pericom Semiconductor's PI3VDP612-A mux/demux is targeted for next generation digital video signals. This device can be used to connect a DisplayPort™ Source to two Independent DisplayPort Sinks or to connect two DisplayPort sources to a single DP display.

The newly released DisplayPort spec requires a data rate of 2.7 Gbps with AC coupled I/Os. Pericom's solution has been specifically designed around this standard and will support such signals.

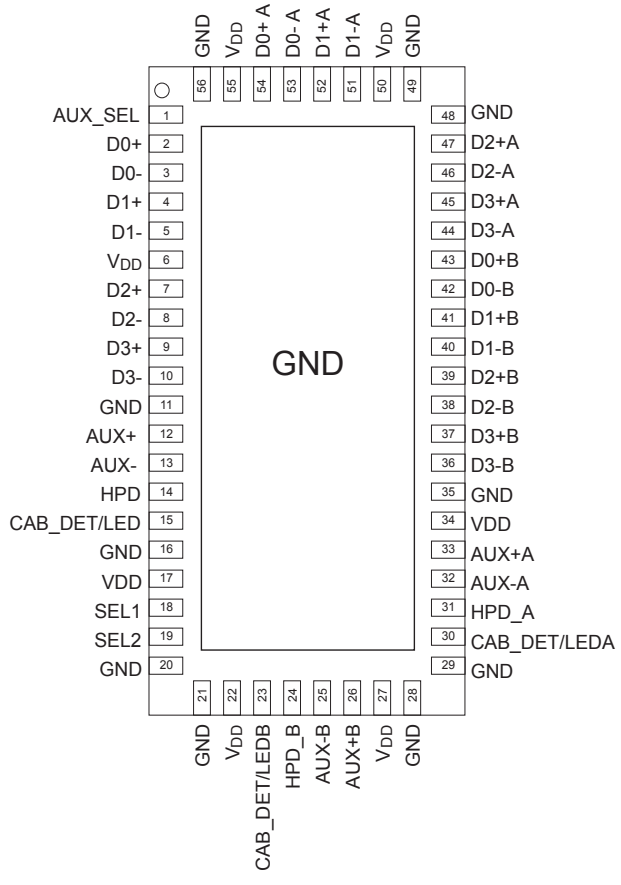
Application

Routing of DisplayPort signals with low signal attenuation between source and sink.

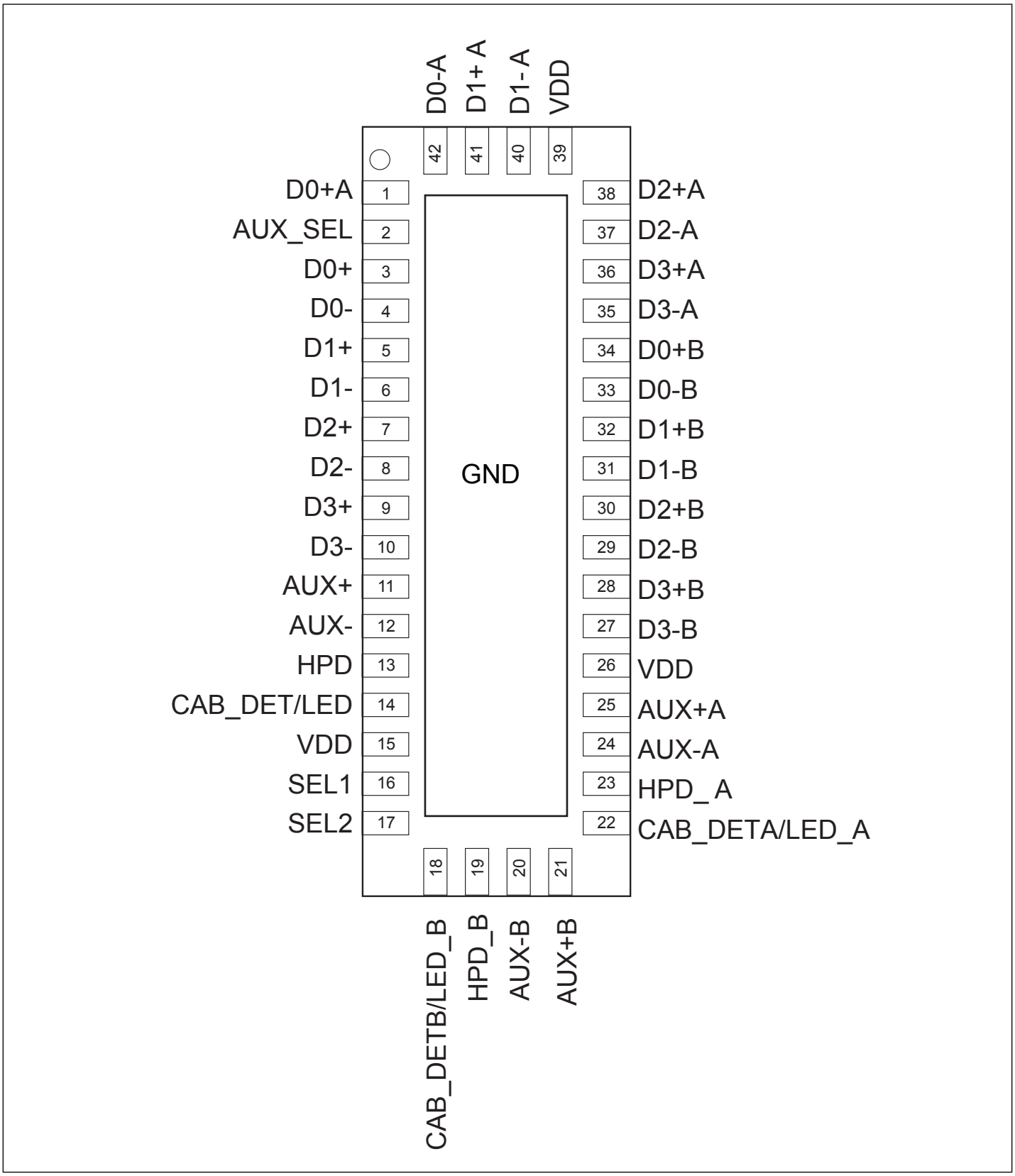
Block Diagram



Pin Description - 56-Pin



Pin Description - 42-Pin



Pin Description

42-Package Pin #	56-Package Pin #	Pin Name	Signal Type	Description	ESD
2	1	AUX_SEL	Input	Logic control for AUX signals: if LOW then AUX from COM port will connect to AUX from port A. If HIGH, then AUX from COM port will connect to AUX from port B.	
3	2	D0+	I/O	Positive Lane0 signal for common port	+/-7kV
4	3	D0-	I/O	Negative Lane0 signal for common port	+/-7kV
5	4	D1+	I/O	Positive Lane1 signal for common port	+/-7kV
6	5	D1-	I/O	Negative Lane1 signal for common port	+/-7kV
15, 26, 39	6, 17, 22, 27, 34, 50, 55	V_{DD}	Power	3.3V Power Supply	
7	7	D2+	I/O	Positive Lane2 signal for common port	+/-7kV
8	8	D2-	I/O	Negative Lane2 signal for common port	+/-7kV
9	9	D3+	I/O	Positive Lane3 signal for common port	+/-7kV
10	10	D3-	I/O	Negative Lane3 signal for common port	+/-7kV
*GND plate	11, 16, 20, 21, 28, 29, 35, 48, 49, 56	GND	Ground	Ground	
11	12	AUX+	I/O	Positive AUX signal for common port	+/-8kV
12	13	AUX-	I/O	Negative AUX signal for common port	+/-8kV
13	14	HPD	I/O	HPD for common port	+/-8kV
14	15	CAB_DET/LED	I/O	Common port pin for cable detect signal or LED common port	+/-8kV
16	18	SEL1	Input	Port Selection Control. If LOW, then port A is active. If HIGH, then port B is active	
17	19	SEL2	Input	Port Selection Control for HPD path and CAB_DET/LED path only: If LOW, then port A is active. If HIGH, then port B is active.	
	20	GND	Power	Ground	
	21	GND	Power	Ground	
	22	V_{DD}	Power	3.3V Power Supply	
18	23	CAB_DETB/ LEDB	I/O	Port B pin13 from dual mode DP connector or LED from port B	+/-8kV
19	24	HPD_B	I/O	HPD for port B	+/-8kV
20	25	AUX-B	I/O	Negative AUX signal for Port B	+/-8kV
21	26	AUX+B	I/O	Positive AUX signal for Port B	+/-8kV

(Continued)

Pin Description

42-Package Pin #	56-Package Pin #	Pin Name	Signal Type	Description	ESD
22	30	CAB_DETA/ LEDA	I/O	Port A cable detect from dual mode DP connector or LED from port A	+/-8kV
23	31	HPD_A	I/O	HPD for port A	+/-8kV
24	32	AUX-A	I/O	Negative AUX signal for Port A	+/-8kV
25	33	AUX+A	I/O	Positive AUX signal for Port A	+/-8kV
27	36	D3-B	I/O	Negative Lane3 signal for Port B	+/-8kV
28	37	D3+B	I/O	Positive Lane3 signal for Port B	+/-8kV
29	38	D2-B	I/O	Negative Lane2 signal for Port B	+/-8kV
30	39	D2+B	I/O	Positive Lane2 signal for Port B	+/-8kV
31	40	D1-B	I/O	Negative Lane1 signal for Port B	+/-8kV
32	41	D1+B	I/O	Positive Lane1 signal for Port B	+/-8kV
33	42	D0-B	I/O	Negative Lane0 signal for Port B	+/-8kV
34	43	D0+B	I/O	Positive Lane0 signal for Port B	+/-8kV
35	44	D3-A	I/O	Negative Lane3 signal for Port A	+/-8kV
36	45	D3+A	I/O	Positive Lane3 signal for Port A	+/-8kV
37	46	D2-A	I/O	Negative Lane2 signal for Port A	+/-8kV
38	47	D2+A	I/O	Positive Lane2 signal for Port A	+/-8kV
40	51	D1-A	I/O	Negative Lane1 signal for Port A	+/-8kV
41	52	D1+A	I/O	Positive Lane1 signal for Port A	+/-8kV
42	53	D0-A	I/O	Negative Lane0 signal for Port A	+/-8kV
1	54	D0+A	I/O	Positive Lane0 signal for Port A	+/-8kV

Truth Table (SEL control)

Function	SEL 1/SEL2/AUX_SEL
Port A is active	L
Port B is active	H

Notes:

SEL1 is only for DP lanes

SEL2 is only for HPD/CAB_DET signals

AUX_SEL is only for AUX path

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +3.6V
DC Input Voltage	–0.7V to 3.6V
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for Switching over Operating Range (T_A = –40°C to +85°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions(1)	Min	Typ(1)	Max	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level	1.6			V
V_{IL}	Input LOW Voltage	Guaranteed LOW level			0.75	
V_{IK}	Clamp Diode Voltage	V_{DD} = Max., I_{IN} = –18mA		–0.7	–1.2	
I_{IH}	Input HIGH Current	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{IL}	Input LOW Current	V_{DD} = Max., V_{IN} = GND			±5	
I_{OFF}	I/O leakage when part is off	V_{DD} = 0V, V_{INPUT} = 0V to 3.6V			50	
R_{ON}	On resistance between input to output	V_{DD} = 3.0V, -0.6V<V_{INPUT}<0.6V V_{DD} = 3.0V, 1.0V<V_{INPUT}<1.5V			7 10	Ohm Ohm

Power Supply Characteristics (T_A = 0°C to +70°C)

Parameter	Description	Test Conditions(1)	Min	Typ(1)	Max	Units
I_{CC}	Quiescent Power Supply Current	V_{DD} = Max., V_{IN} = GND or V_{DD}			70	µA

Dynamic Electrical Characteristics over Operating Range (T_A = -40° to +85°C, V_{DD} = 3.3V ±10%, GND=0V)

Parameter	Description	Test Conditions		Typ.(2)	Units
X_{TALK}	Crosstalk on High Speed Channels	See Fig. 1 for Measurement Setup	f= 1.35 GHz	-33dB	dB
			f = 100 MHz	-48dB	
O_{IRR}	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup,	f= 1.35 GHz	-33dB	
			f = 100 MHz	-56dB	
I_{LOSS}	Differential Insertion Loss on High Speed Channels	@2.7Gbps (see figure 3)		-1.5	dB
BW_Dx±	Bandwidth -3dB for Main high speed path (Dx±)	See figure 3		3.25	GHz
BW_AUX/HPD	-3dB BW for AUX and HPD signals	See figure 3		1.5	GHz

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

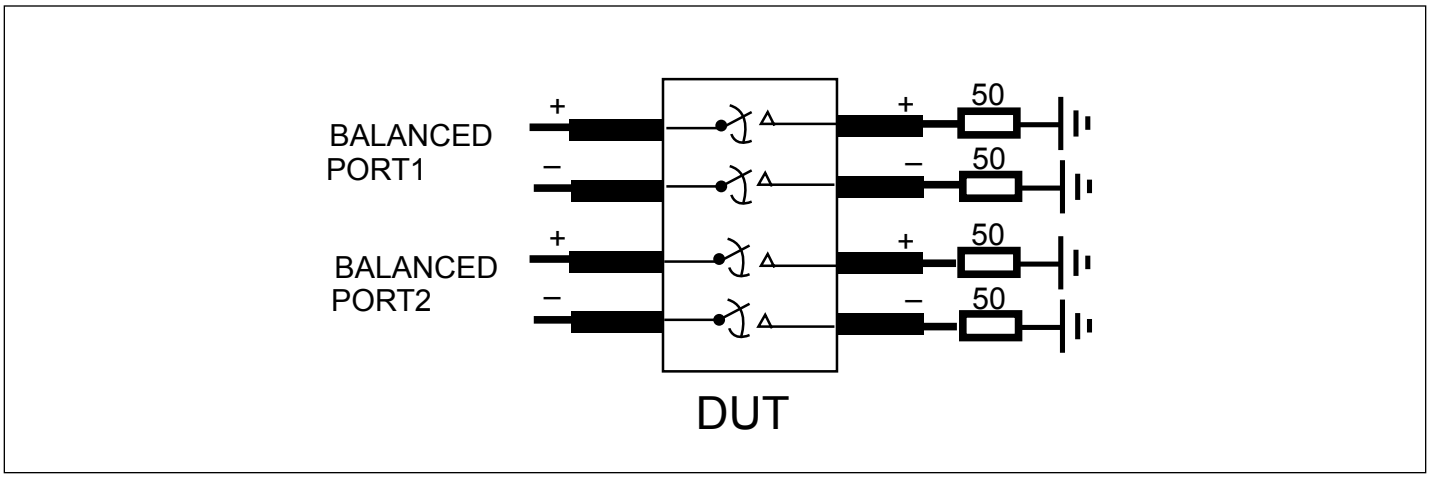


Fig 1. Crosstalk Setup

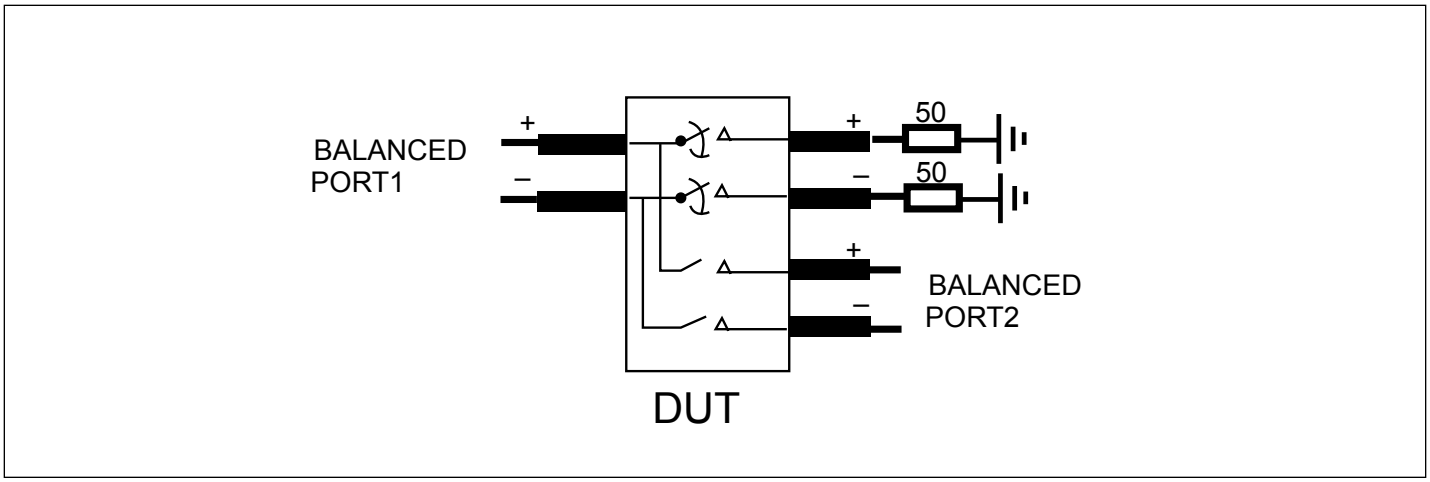


Fig 2. Off-isolation setup

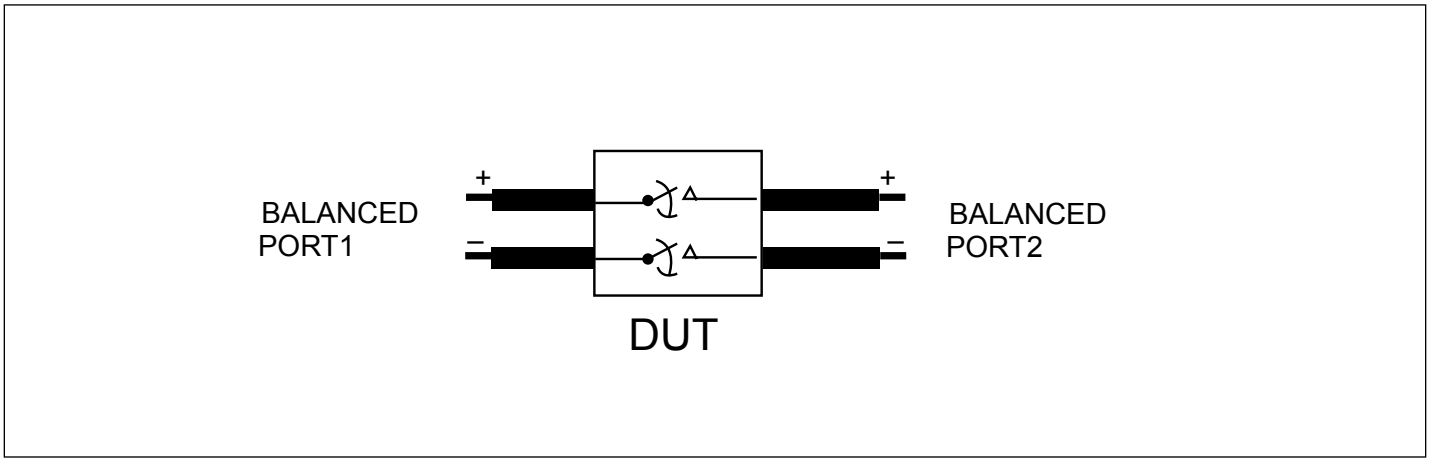


Fig 3. Differential Insertion Loss

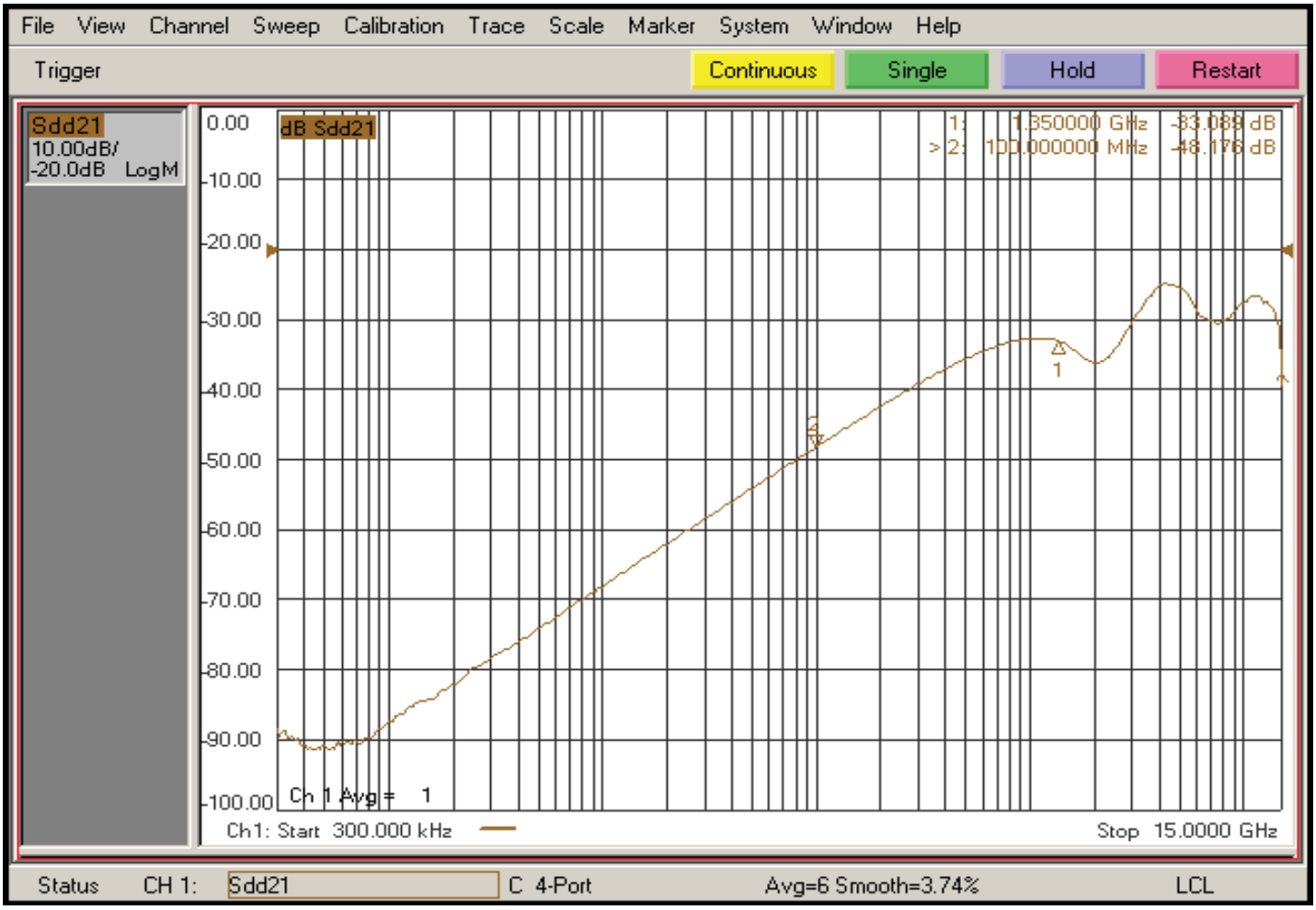

File View Channel Sweep Calibration Trace Scale Marker System Window Help
Trigger
Continuous
Single
Hold
Restart
Sdd21
10.00dB/
-20.0dB LogM
dB Sdd21
1: 1.350000 GHz -33.089 dB
> 2: 100.000000 MHz -48.176 dB
0.00
-10.00
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
-100.00
Ch 1 Avg = 1
Ch1: Start 300.000 kHz
Stop 15.0000 GHz
Status
CH 1:
Sdd21
C 4-Port
Avg=6 Smooth=3.74%
LCL

Fig 4. Xtalk

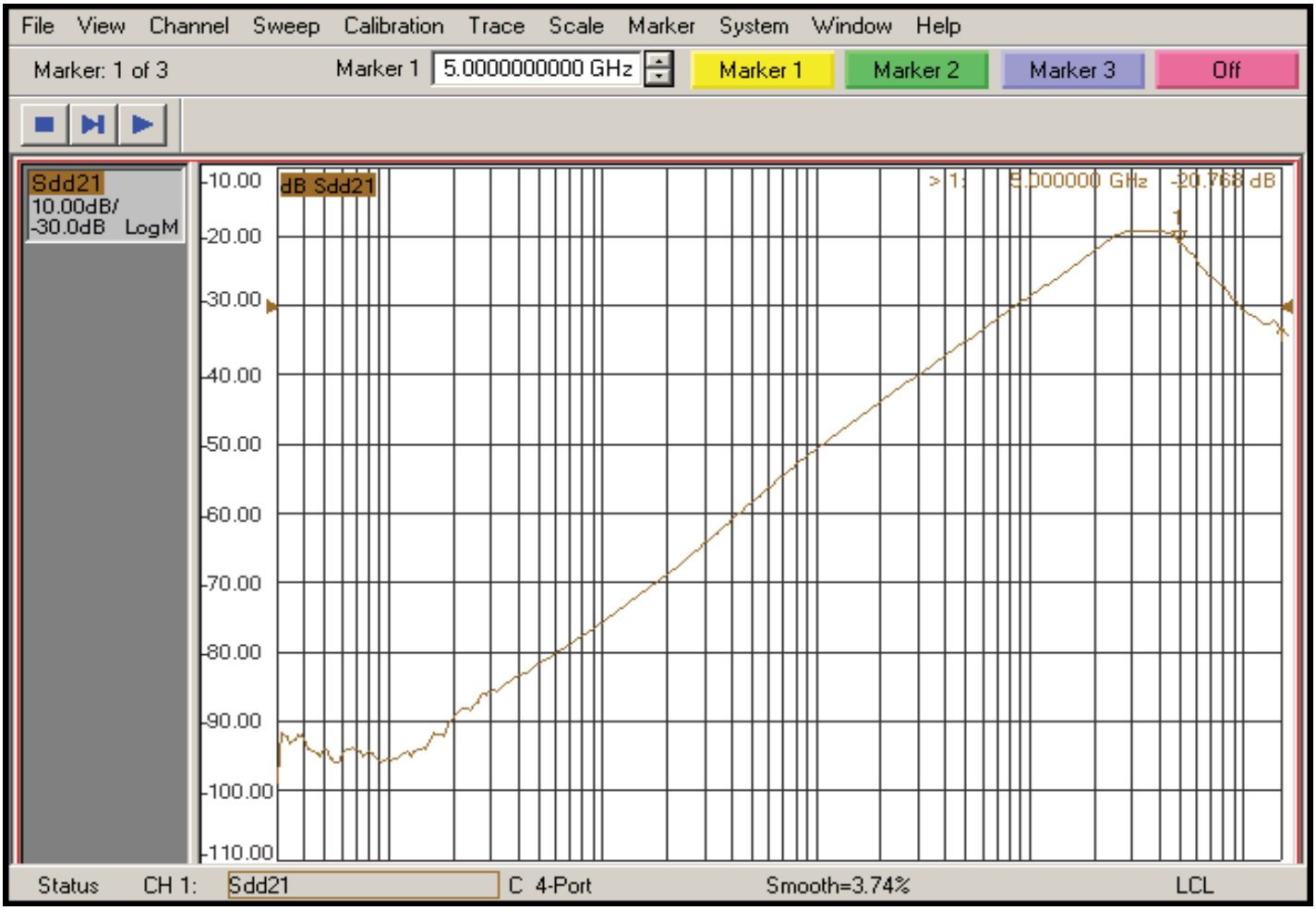


Fig 5. Off Isolation

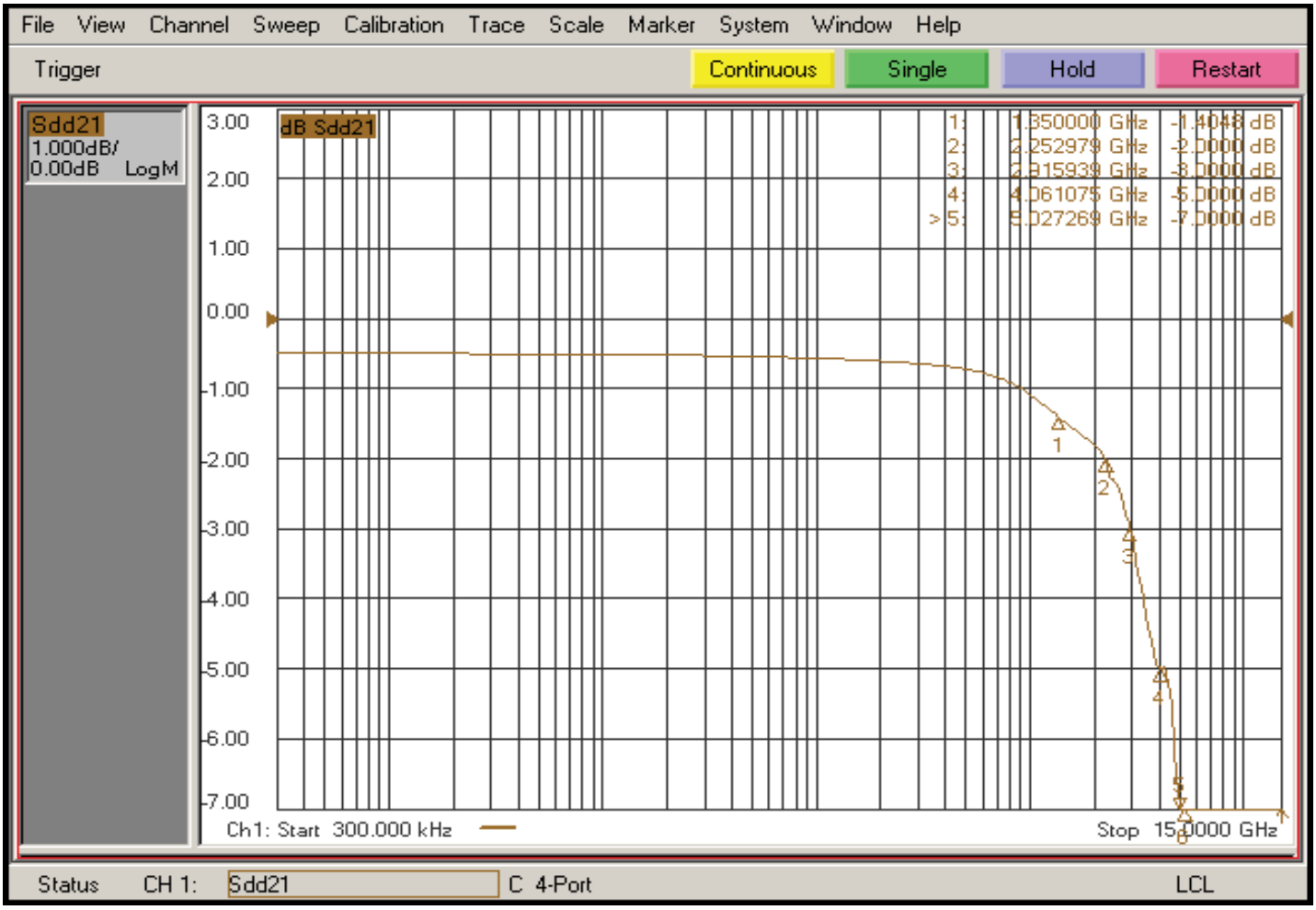


Fig 6. Insertion Loss

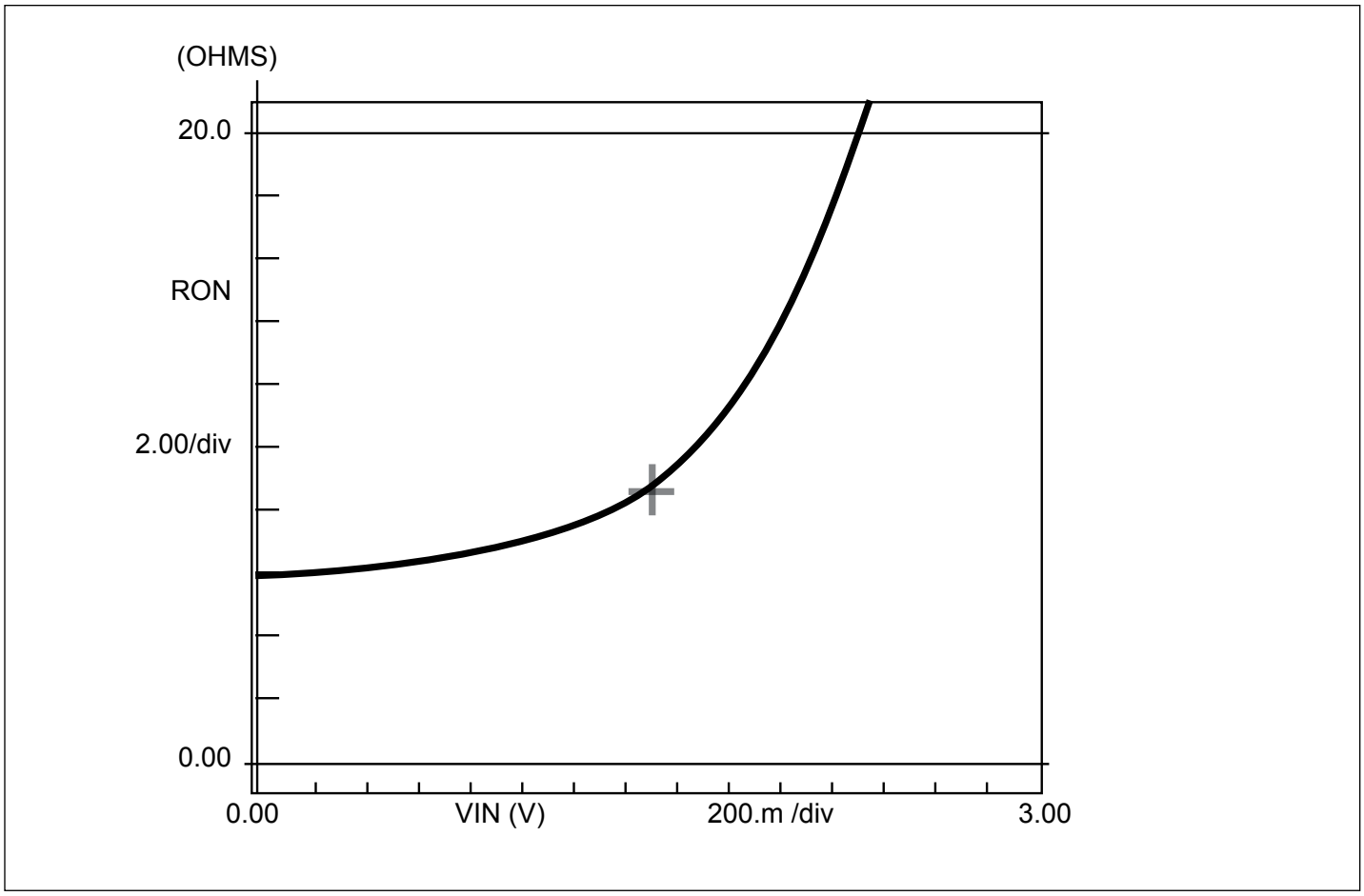
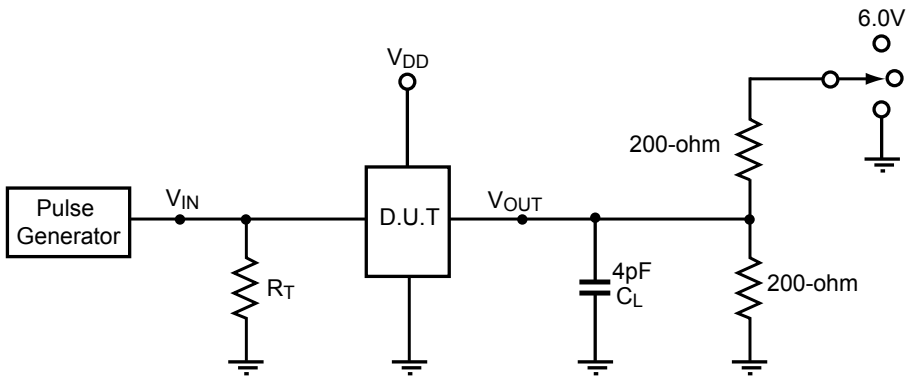


Fig 7. Ron Curve for High Speed Signal Path Only (Dx±)

Switching Characteristics (T_A= -40° to +85°C, V_{DD} = 3.3V±10%)

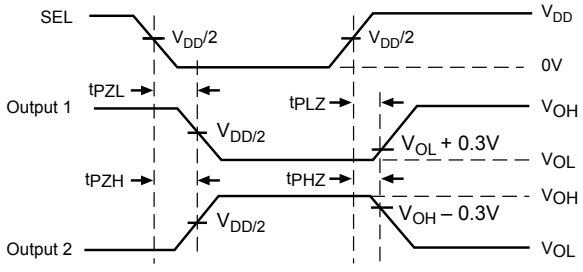
Parameter	Description	Min.	Max.	Units
t_{PZH}, t_{PZL}	Line Enable Time	0.5	15.0	ns
t_{PHZ}, t_{PLZ}	Line Disable Time	0.5	15.0	
T_{pd}	Propagation delay (input pin to output pin)		200	ps
t_{b-b}	Bit-to-bit skew within the same differential pair		7	ps
t_{ch-ch}	Channel-to-channel skew		50	ps

Test Circuit for Electrical Characteristics(1-5)



Notes:
1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.
5. The outputs are measured one at a time with one transition per measurement.

Switching Waveforms

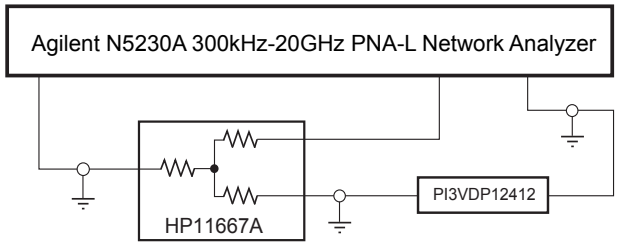


Voltage Waveforms Enable and Disable Times

Switch Positions

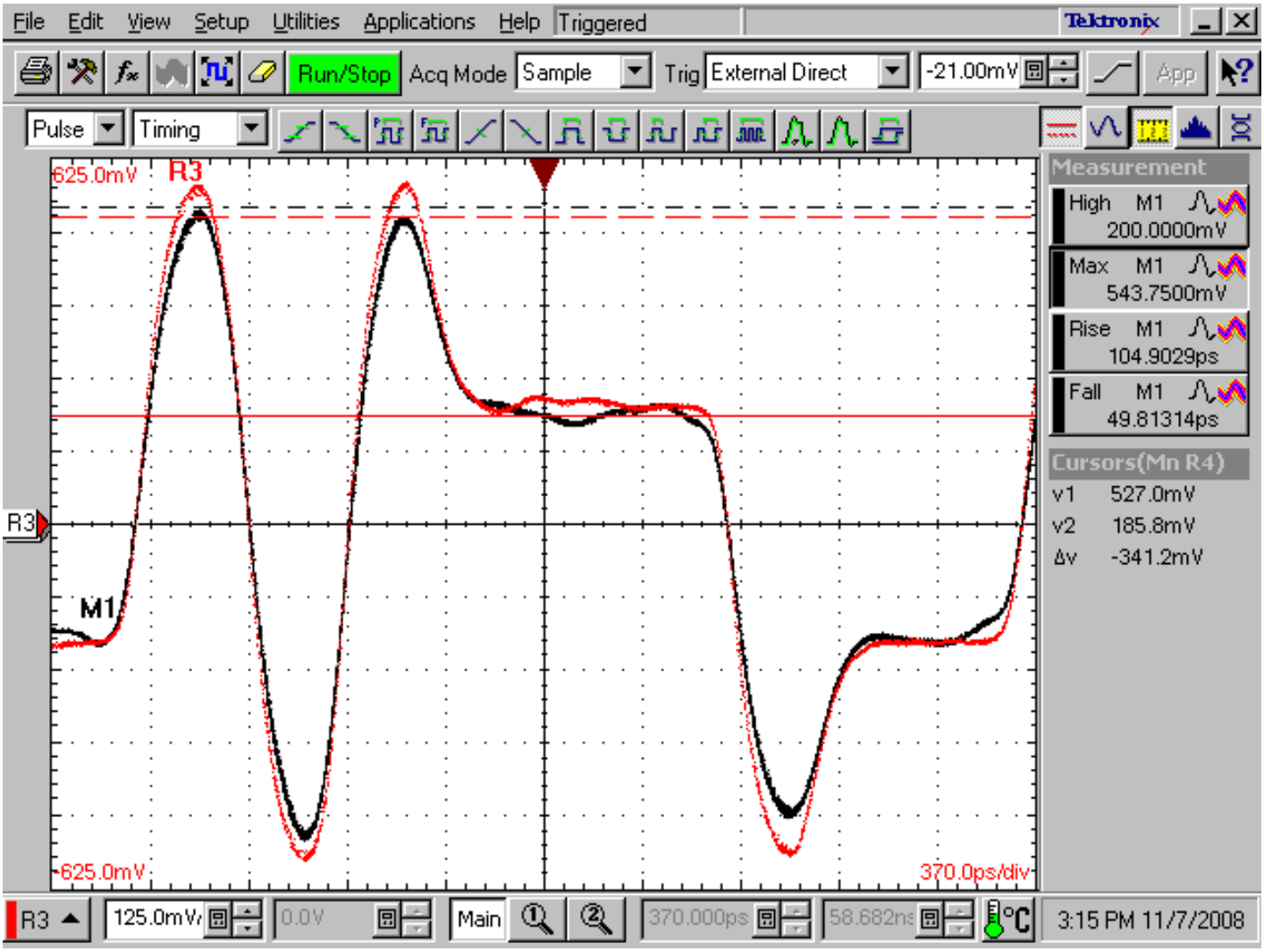
Test	Switch
t_{PLZ}, t_{PZL} (output on B-side)	6.0V
t_{PHZ}, t_{PZH} (output on B-side)	GND
Prop Delay	Open

Test Circuit for Dynamic Electrical Characteristics

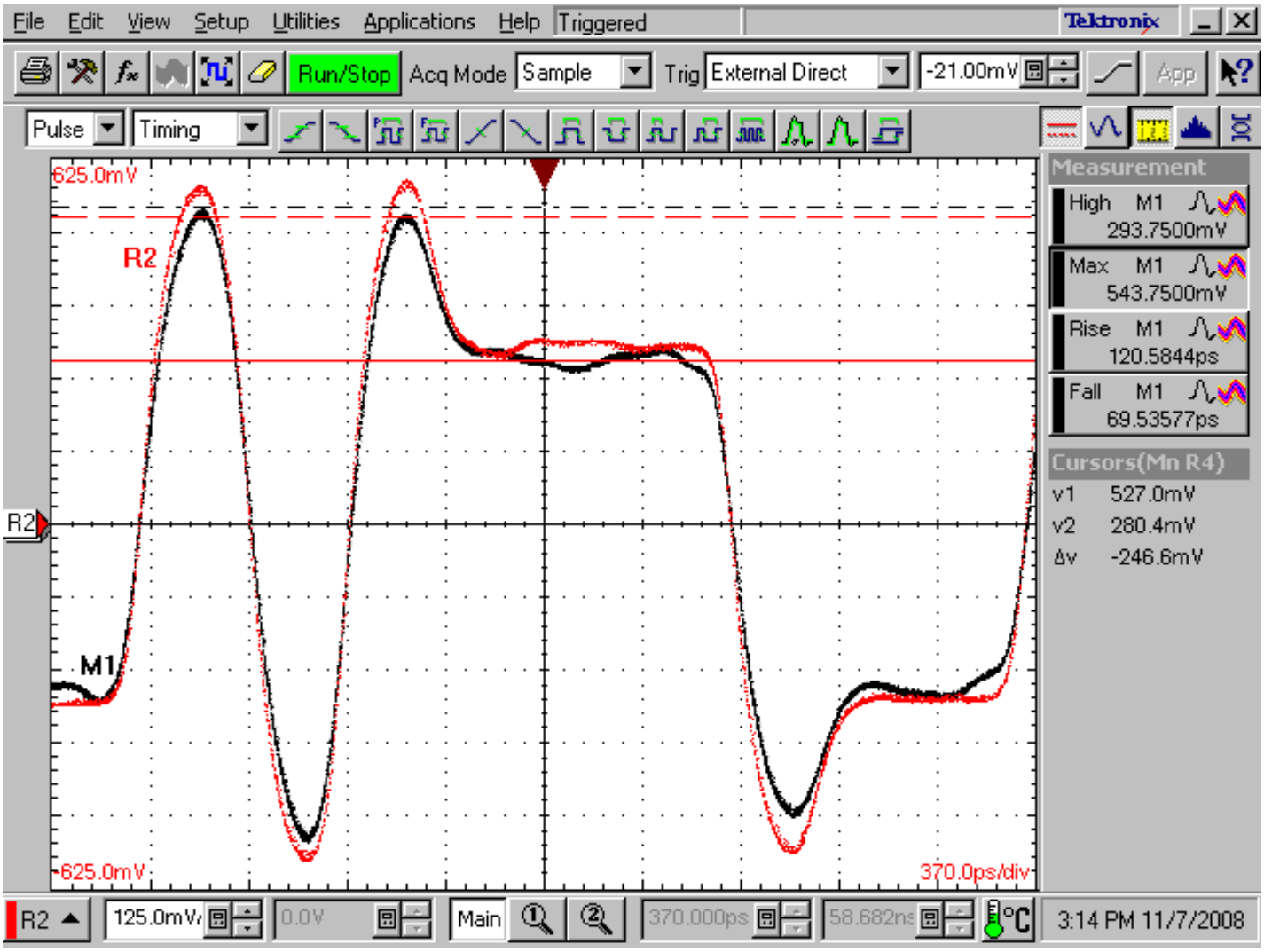


Application Section - Pre-Emphasis Waveforms

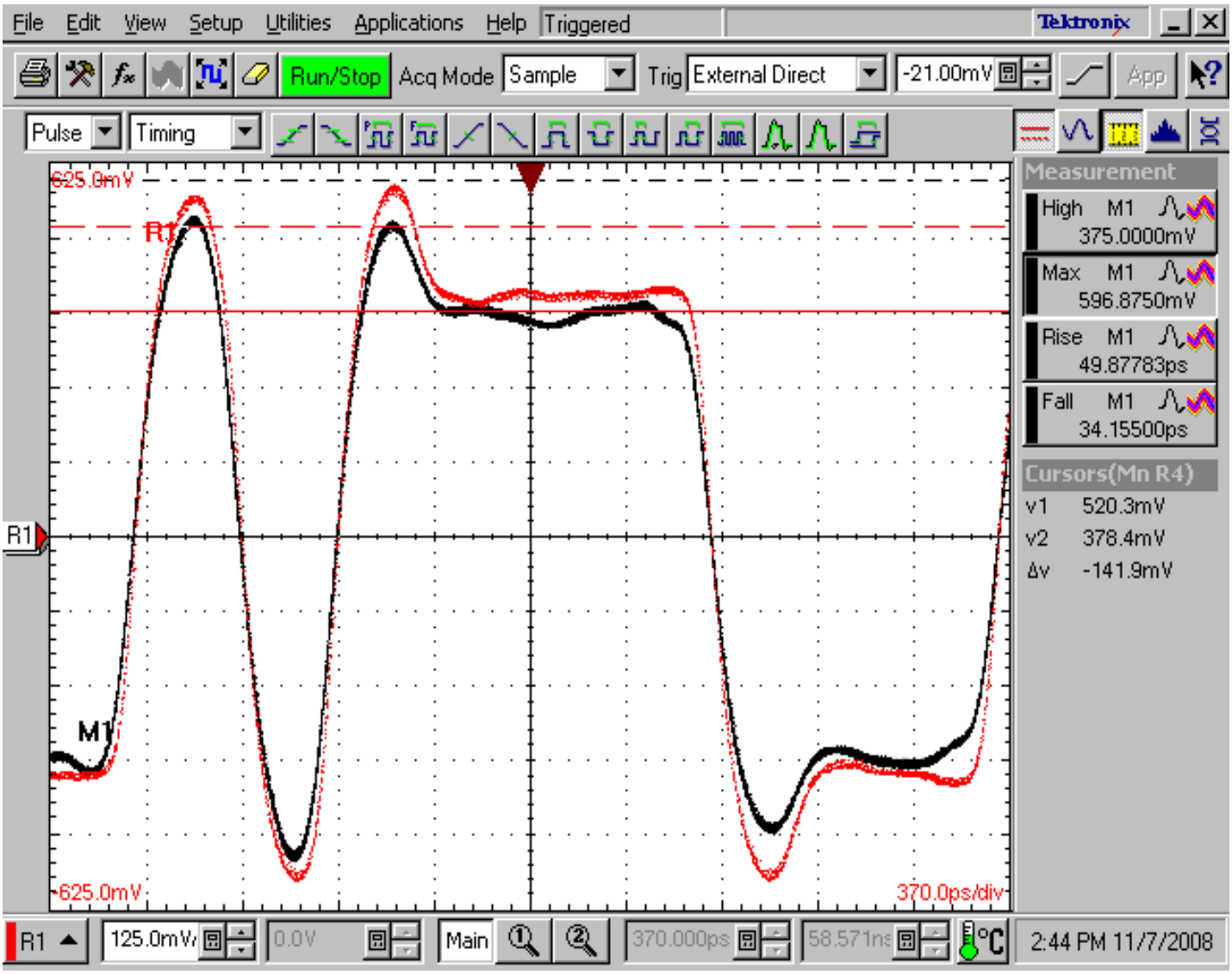
Input Pre-emphasis = 9.5dB; Red waveform is input of PI3VDP612-A & Black is output of PI3VDP612-A



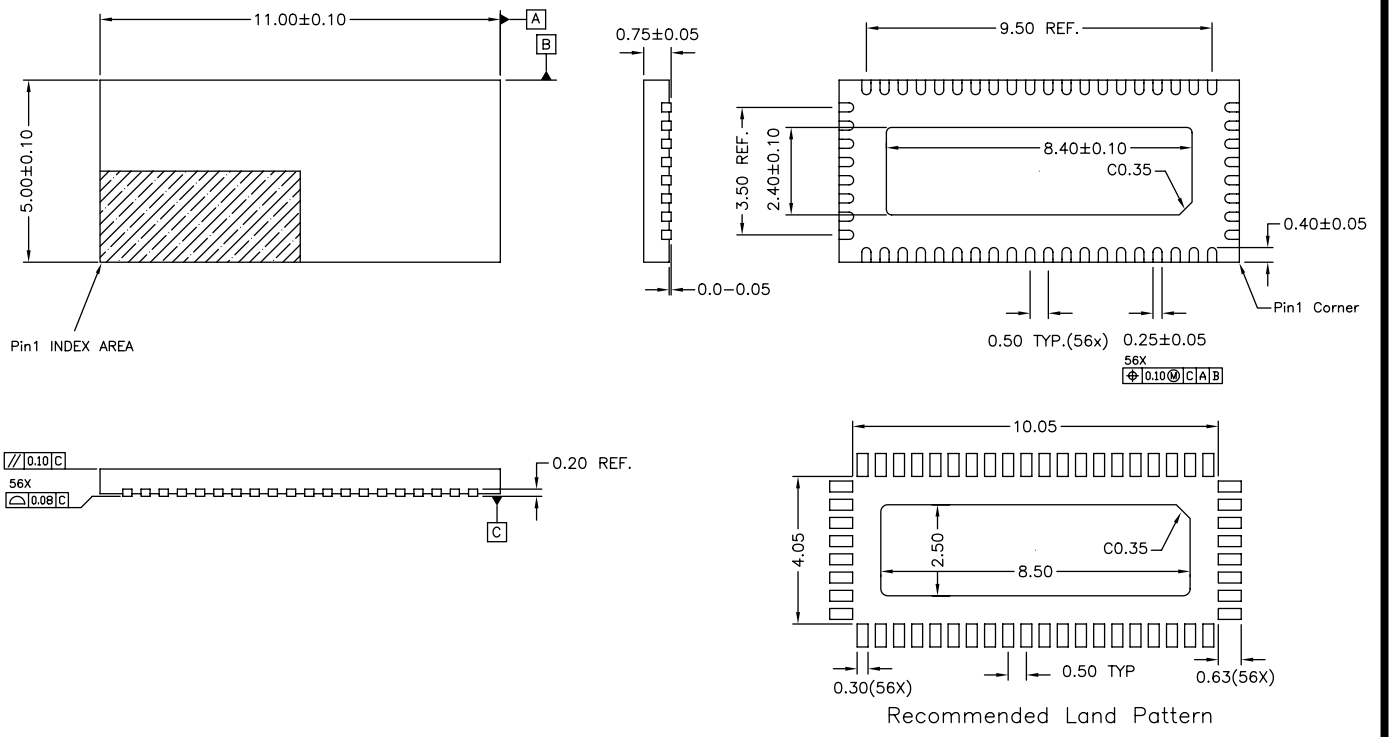
Input Pre-emphasis = 6dB; Red waveform is input of PI3VDP612-A and Black is output of PI3VDP612-A



Input Pre-emphasis = 3.5dB; Red waveform is input of PI3VDP612-A & Black is output of PI3VDP612-A



Packaging Mechanical: 56-Contact TQFN (ZF)



NOTE :
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−220 MODIFIED.
4. Thermal Via Diameter. Recommended 0.2~0.33mm
5. Thermal Via Pitch. Recommended 1.27mm

PERICOM Semiconductor Corporation — DATE: 05/15/08

DESCRIPTION: 56-contact, Thin Fine Pitch Quad Flat No-lead (TQFN)

PACKAGE CODE: ZF56

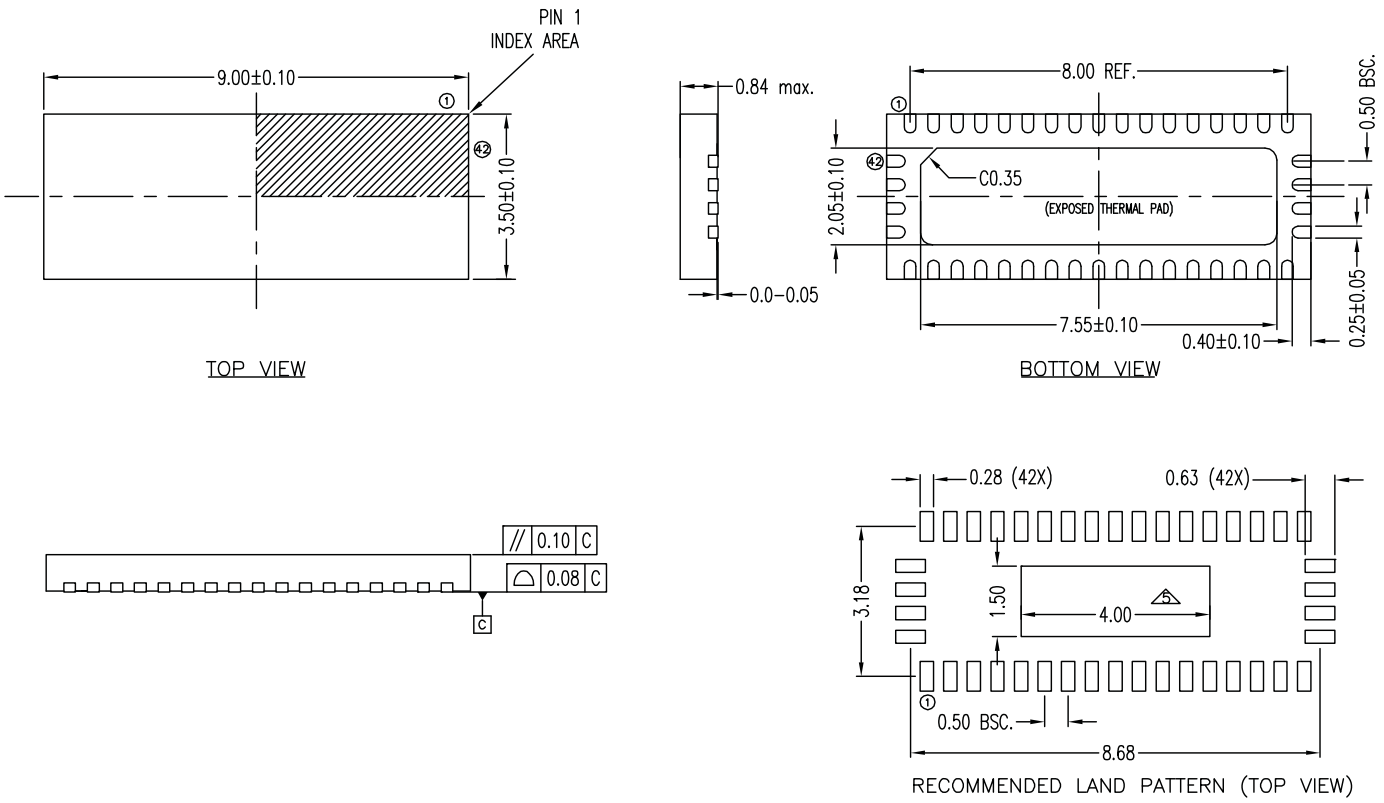
DOCUMENT CONTROL #: PD-2024 — REVISION: C

08-0208

Note:

- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Packaging Mechanical: 42-Pin TQFN (ZH)



Notes:
1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended Land Pattern is for reference only.
5. Thermal Pad Soldering Area

PERICOM Semiconductor Corporation — DATE: 02/17/09

DESCRIPTION: 42-contact Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH42)

DOCUMENT CONTROL #: PD-2035 — REVISION: C

09-0116

Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3VDP612-AZFE	ZF	Pb-free & Green, 56-contact TQFN
PI3VDP612-AZHE	ZH	Pb-free & Green, 42-contact TQFN

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging