

10.3Gbps Thunderbolt™ and DisplayPort™ Switch

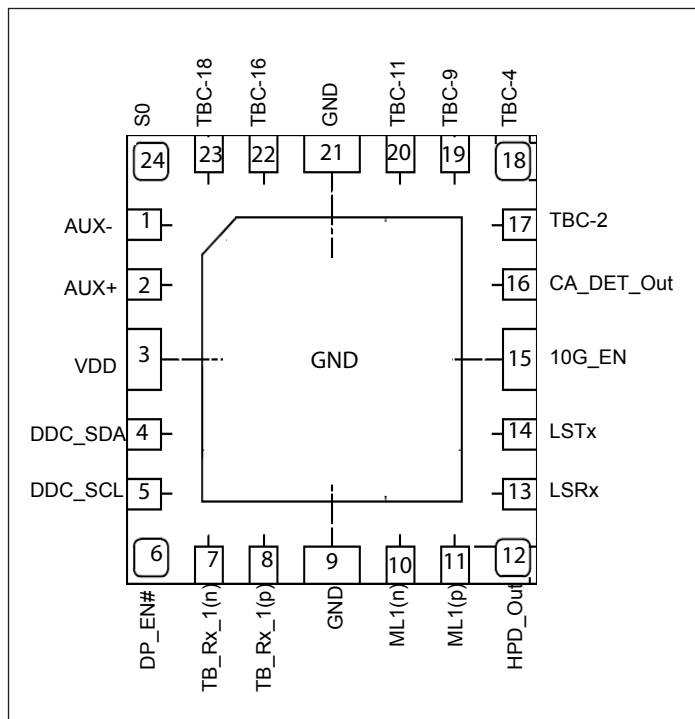
Features

- Supports 5.4Gbps for DisplayPort 1.2 and 10.3Gbps for Thunderbolt Electrical Standard
- Supports DP and DP++ Configuration
- Supports AUX and DDC MUX
- V_{DD} Operating Range for normal operation: 3.3V±10%
 - Extended operation down to 2.5V min on the LSTx/LSRx to TBC-9/TBC-11 channels (performance not guaranteed, but all buffers will still operate)
- ESD protection on all pins
 - 1.0kV HBM per JESD22 standard
- Packaging (Pb-free & Green):
 - 3.0 mm x 3.0 mm, 24-contact TQFN

Application

- Thunderbolt over mini-DP connector enablement

Pin Configuration (Top View)



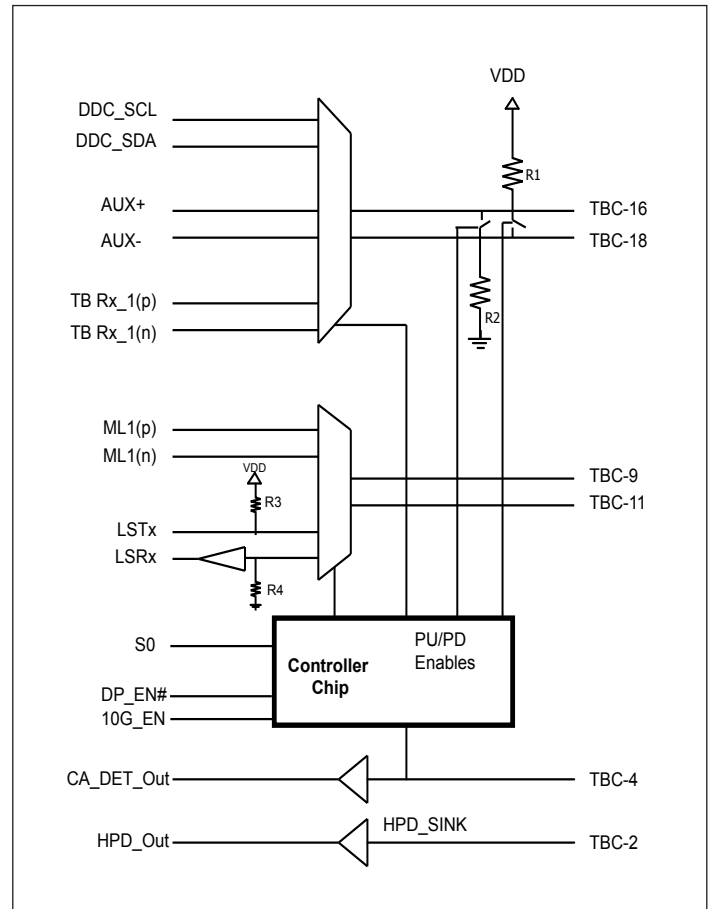
Description

Pericom Semiconductor's PI3TB212 is a high-speed multiplexer/demultiplexer switch. PI3TB212 can switch signals up to 10.3125Gbps for DisplayPort and Thunderbolt™(TB) applications. The device supports 5.4Gbps for DisplayPort and 10.3125Gbps for Thunderbolt.

PI3TB212 is a major advance over first-generation Thunderbolt solutions. PI3TB212 integrates the 10.3125 Gbps Thunderbolt path. This eliminates external PIN diode switches, thereby reducing board space, reducing cost, and improving link performance.

PI3TB212 achieves excellent signal integrity at 10.3125 Gbps as evidenced by measured results.

Block Diagram



Pin Description

| Pin # | Pin Name | Type | Description |
|----------------------|--------------------------|----------|--|
| 17 | TBC-2 | I | Connector Side Hot Plug Detect Input. Connect to mini-DP connector pin2 |
| 11 10 | ML1(p) ML1(n) | I/O | Controller Side Channel 1, DisplayPort Positive Signal (external AC coupling is required) Controller Side Channel 1, DisplayPort Negative Signal (external AC coupling is required) |
| 22 23 | TBC-16 TBC-18 | I/O | Sink Side TB Rx1(p) or AUX+ Signal or DDC_SCL. Connect to mini-DP connector pin 16. Sink Side TB Rx1(n) or AUX- Signal or DDC_SDA. Connect to mini-DP connector pin 18. |
| 19 20 | TBC-9 TBC-11 | I/O | Sink Side DP Main Link + Signal or LSTX. Connect to mini-DP connector pin 9. Sink Side DP Main Link - Signal or LSRX. Connect to mini-DP connector pin 11 |
| 2 1 | AUX+ AUX- | I/O | Controller Side AUX Positive Signal Controller Side AUX Negative Signal |
| 8 7 | TB Rx_1(p) TB Rx_1(n) | I/O | Controller Side 10Gbps Positive Signal (external AC coupling is required) Controller Side 10Gbps Negative Signal (external AC coupling is required) |
| 5 4 | DDC_SCL DDC_SDA | I/O | Controller Side DDC Clock Controller Side DDC Data |
| 18 | TBC-4 | I | Connector Side Cable Detect for DP++ Dongle. Connect to mini-DP connector pin 4. |
| 12 | HPD_Out | O | Controller Side Buffered Hot Plug Detect Output |
| 14 13 | LSTx LSRx | I/O O | Controller Side un-buffered UART TX Signal. Integrated 9KΩ pull-up Controller Side buffered UART RX Signal. 1MΩ pull-down present at buffer input |
| 24 | S0 | I | Control signal. See truth table for detailed functionality |
| 16 | CA_DET_Out | O | Cable detect buffered output coming from TBC-4 (pin 18) |
| 6 | DP_EN# | I | DisplayPort path enable. See truth table for detailed functionality. |
| 15 | 10G_EN | I | 10G path enable. See truth table for detailed functionality. |
| 3 | VDD | Power | 3.3V+/-10% power supply voltage |
| Center Pad, 9, 21 | GND | Ground | Ground. both pins and center pad must all be connected to GND plane. |

Description of Operation

Truth Table

| Device States | Control Pins | | | | Device and PU/PD Configurations | | | |
|----------------------|-------------------|--------|--------|-------|---------------------------------|---------|-------------------------------------|-------------------|
| | S0 | 10G_EN | DP_EN# | TBC-4 | 2:1 Mux | 3:1 Mux | LSRx, HPD_Out, & CA_DET_Out buffers | R1, R2 status |
| Thunderbolt 10G mode | 1 (System Active) | 1 | 1 | X | LSTx & LSRx | TB Rx_1 | ALL BUFFERS ON | R1 = R2 = OFF |
| | 0 (System Sleep) | 1 | 1 | X | LSTx & LSRx | Hi-z | | R1 = R2 = OFF |
| DisplayPort Mode | 1 (System Active) | 0 | 0 | 0 | DP ML1 (p, n) | AUX | ALL BUFFERS ON | R1 = R2 = ON |
| | 0 (System Sleep) | 0 | 0 | 0 | Hi-Z | Hi-z | | R1 = R2 = ON |
| TMDS Mode | 1 (System Active) | 0 | 0 | 1 | DP ML1 (p, n) | DDC | ALL BUFFERS ON | R1 = R2 = ON |
| | 0 (System Sleep) | 0 | 0 | 1 | Hi-Z | Hi-z | | R1 = R2 = ON |
| Detect Mode | X - don't care | 0 | 1 | X | LSTx & LSRx | Hi-z | ALL BUFFERS ON | R1 = R2 = ON |
| Chip Disable mode | X - don't care | 1 | 0 | x | hi-z | hi-z | ALL BUFFERS ON | R1 = ON, R2 = ON |
| Power off (VDD = 0V) | X - don't care | x | x | x | hi-z | hi-z | ALL BUFFERS OFF | R1 = OFF, R2 = ON |

| ThunderBolt Connector Pins | Controller Pin Names |
|----------------------------|----------------------------------|
| TBC-16 | DDC_SCL or AUX(p) or TB RX_1 (p) |
| TBC-18 | DDC_SDA or AUX(n) or TB RX_1 (n) |
| TBC-9 | ML1 (p) or LSTx |
| TBC-11 | ML1 (n) or LSRx |
| TBC-4 | CA_DET_Out |
| TBC-2 | HPD_Out |

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| | |
|--|-----------------|
| Storage Temperature | -65°C to +150°C |
| Supply Voltage to Ground Potential | -0.5V to +4.6V |
| I/O (Pin7 and 8) DC Input Voltage | -0.5V to 1.5V |
| I/O (pin 1, 2, 4, and 5) | -0.5V to 4.0V |
| I/O (pin 10 and 11)..... | -0.5V to 2.6V |
| I/O (pin 19 and 20) | -0.5V to 4.0V |
| DC Output Current | 120mA |
| Power Dissipation | 0.5W |
| Control Logic DC Input Voltage | VDD + 0.5V |

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics
 Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------|--|---|-----|-----|------|-------|
| VDD | 3.3V Power Supply | | 3.0 | 3.3 | 3.6 | V |
| I _{DD} | current consumption in normal operation | Control pins = GND or VDD, LSTx = VDD | | 300 | 780 | uA |
| I _{DDQ} (System off) | Current consumption when S0 = 0 | S0 = 0, TBC-2 and TBC-4 = GND or VDD, LSTx = VDD, all I/Os are floating | | 100 | 300 | |
| I _{DD_detect} | Current consumption during detect | S0 = VDD, 10G_EN = 0, DP_EN# = VDD, LSTx = VDD, all I/Os are floating | | 120 | 300 | |
| P _{DD} | Total Power from V _{DD} 3.3V supply | Control pins = GND or VDD, LSTx = VDD | | 1 | 2.8 | mW |
| P _{DDQ} (System off) | Power consumption when S0 = 0 | S0 = 0, TBC-2 and TBC-4 = GND or VDD, LSTx = VDD | | 330 | 1080 | uW |
| P _{DD_Detect} | Power consumption during detect | S0 = VDD, 10G_EN = 0, DP_EN# = VDD, LSTx = VDD | | 400 | 1080 | uW |
| T _{CASE} | Case operating temperature range | | 0 | | 105 | C |

DC Electrical Characteristics for Switching over Operating Range

| Parameters | Description | Test Conditions ⁽¹⁾ | Min | Typ ⁽¹⁾ | Max | |
|-----------------------------|---|---|-----|--------------------|------|----|
| V _{IH} | Input HIGH Voltage for S0, DP_EN#, 10G_EN, TBC-4, TBC-2, TBC-11 | VDD = 3.3V | 1.8 | | | V |
| V _{IL} | Input LOW Voltage for S0, DP_EN#, 10G_EN, TBC-4, TBC-2, TBC-11 | VDD = 3.3V | | | 0.8 | |
| V _{IK} | Clamp Diode Voltage | VDD= Max., I _{IN} = -18mA | | -0.7 | -1.2 | |
| I _{IH} | Input HIGH Current for S0, DP_EN#, 10G_EN, TBC-4, TBC-2 | VDD = Max., V _{IN} = V _{DD} | -1 | | 1 | uA |
| I _{IL} | Input LOW Current for S0, DP_EN#, 10G_EN, TBC-4, TBC-2 | VDD = Max., V _{IN} = 0V | -1 | | 1 | |
| I _{OFF} (TBC pins) | leakage from TBC-16 | VDD = 0V, 1.5V present on TBC-16 TB Rx_1 (p/n) is floating | -60 | | +60 | uA |
| | leakage from TBC-18 | VDD = 0V, 1.5V present on TBC-18 TB Rx_1 (p/n) is floating | -20 | | +20 | |
| | leakage from TBC-9, TBC-11, TBC-4, & TBC-2 | VDD = 0V, 3.3V present on TBC pins ML1(p/n) is floating | -20 | | +20 | |

DC Electrical Characteristics for Switching over Operating Range

| Parameters | Description | Test Conditions ⁽¹⁾ | Min | Typ ⁽¹⁾ | Max | Units |
|----------------------|---|---|------|--------------------|------|-------|
| I _{Leakage} | Leakage on TB-16/TB-18 Thunderbolt 10G Mode | VDD = 3.6V. TB path on. Vin = 1.0V, TBRx_1 (p/n) is floating | | 20 | 50 | μA |
| IOZL | I/O leakage for DDC/AUX | VDD = 3.6V. Vin = 0V | | 10 | 15 | |
| | I/O leakage for TB Rx1(p/n) | VDD = 3.6V. Vin = 0V; TBC16, 18 = 0.2V | | 20 | 50 | |
| | I/O leakage for ML1 | VDD = 3.6V. Vin = 0V; TBC9, 11 = 0.5V | | 10 | 15 | |
| | I/O leakage for LSTx | VDD = 3.6V. Vin = 0V | -600 | -400 | -300 | |
| | I/O leakage for TBC9 and 11 | VDD = 3.6V, Vin = 0V, ML1 (p/n) is floating | | 10 | 15 | |
| | I/O leakage for TBC16 and 18 | VDD = 3.6V, Vin = 0V, S0=low, 10G_EN = high, DP_EN# = high, TBRx_1 (p/n) is floating, Thunderbolt Mode | | 40 | 78 | |
| IOZH | I/O leakage for DDC/AUX | VDD = 3.6V. Vin = VDD | | 10 | 15 | |
| | I/O leakage for TB Rx1(p/n) | VDD = 3.6V. Vin = 0.5V | | 20 | 50 | |
| | I/O leakage for ML1 | VDD = 3.6V. Vin = 2.6V | | 10 | 15 | |
| | I/O leakage for LSTx | VDD = 3.6V. Vin = VDD | | 10 | 15 | |
| | I/O leakage for TBC9 and 11 | VDD = 3.6V, Vin = VDD, ML1(p/n) is floating | | 10 | 15 | |
| | I/O leakage for TBC16 and 18 | VDD = 3.6V, Vin = VDD, S0=low, 10G_EN = high, DP_EN# = high, TBRx_1 (p/n) is floating, Thunderbolt mode | | 80 | 150 | |

R_{ON} Table

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|--------------------------|--------------------------|--|------|------|------|-------|
| R _{ON} AUX/LSTx | AUX & LSTx On Resistance | VDD = 3.3V Vin _{input} = 3.3V, I _{input} = -40mA | | 9 | 15 | Ohms |
| R _{ON} TB | TB On Resistance | VDD = 3.3V Vin _{input} = 0V, I _{input} = -40mA | | 5 | 8 | |
| R _{ON} DP | DP On Resistance | VDD = 3.3V Vin _{input} = 0V, I _{input} = -40mA | | 5 | 8 | |
| R _{ON} DDC | DDC On Resistance | VDD = 3.3V Vin _{input} = 3.3V, I _{input} = -40mA | | 5 | 25 | |

Dynamic Electrical Characteristics

| Parameter | Description | Test Conditions | Min. | Typ. ⁽¹⁾ | Max. | Units |
|----------------------------------|---|---|------|----------------------|------|-------|
| DDIL ⁽²⁾ (TB RX_1) | Insertion Loss on TB Rx_1 (p, n) to TBC-16 and TBC-18 path (V _{IN} = -10dBm, DC = 0V) | f=4.0GHz f=5.0GHz f=8.0GHz | | -1.2 -1.5 -3.0 | | dB |
| DDIL (ML1) | Insertion Loss on ML1 (p, n) to TBC-9 and TBC-11 path (V _{IN} = -10dBm, DC = 0V) | f=810MHz (RBR) f=1.35GHz (HBR1) f=2.7GHz (HBR2) | | -0.5 -0.7 -1.1 | | dB |
| DDRL ⁽²⁾ (TB Rx_1) | Differential Return Loss on 10G thunderbolt path | f= 4.0GHz f= 5.0GHz f= 8.0GHz | | -24 -16 -9 | | dB |
| DDRL (ML1) | Differential Return Loss on DP path | f= 1.35GHz f= 2.7GHz f= 6.0GHz | | -31 -27 -17 | | dB |
| Off-Isolation ³ | Off-isolation for DP path | f = 810MHz f = 1.35GHz f = 2.7GHz | | -27 -22 -16 | | dB |
| | Off-isolation for TB path | f = 4.0GHz f = 5.0GHz | | -16 -15 | | dB |

Notes:

1. Guaranteed by design. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.
2. Refer to figure 1 for test setup
3. Refer to figure 3 for test setup

Buffers (HPD_Out, CA_DET_Out, TBC-2, TBC-4 and LSRx)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|------------|---|--|------|------|------|-------|
| VIH | Input high for TBC-2, TBC-4 and TBC-11 | VDD = 3.6V | 1.8 | | | V |
| VIL | Input Low for TBC-2, TBC-4 and TBC-11 | VDD = 3.6V | | | 0.8 | |
| VOH | Output high for HPD_Out, CA_DET_Out, and LSRx | VDD = 3.3V+/-10%, I _{oh} = -2mA | 2.4 | | VDD | |
| VOL | Output Low for HPD_Out, CA_DET_Out and LSRx | VDD = 3.6V, I _{ol} = 2mA | | | 0.8 | |

Timing

| Parameter | Description | Test Conditions | Min. | Typ. ⁽¹⁾ | Max. | Units |
|-----------|---|---|-----------------------|---------------------|------|-------|
| Tsw | Switching time between paths | VDD = 3.0V | | | 2 | us |
| Tstartup | VDD valid to channel enable | VDD valid = 2.7V VDD ramp is from 0V to 3.3V | | | 10 | us |
| Twakeup | From sleep mode to on mode (toggling S0) | VDD = 3.0V | | | 2 | us |
| Tb-b | Bit-to-bit skew within the same differential pair | VDD = 3.0V | (between pin 22 & 23) | 2 | 5 | ps |
| | | | (between pin 19 & 20) | 2 | 5 | |

Linear region for Analog switches (non-buffered paths)

| Parameter | Description | Test Conditions | Min. | Typ | Max. | Units |
|------------|--|--------------------------|------|-----|------|-------|
| Vp_TBT | TB Rx_1(p) and TB Rx_1(n) path ⁽²⁾ | VDD = 3.3V, Ipass = 10mA | 1.0 | 1.3 | | V |
| Vp_AUX/DDC | AUX+, AUX-, DDC_SCL, & DDC_SDA path ⁽²⁾ | VDD = 3.3V, Ipass = 10mA | 3.6 | 4.2 | | V |
| Vp_ML | ML1(p) and ML1(n) path ⁽²⁾ | VDD = 3.3V, Ipass = 10mA | 2.2 | 2.5 | | V |
| Vp_LSTx | LSTx signal path ⁽²⁾ | VDD = 3.3V, Ipass = 10mA | 3.6 | 4.2 | | V |

Pull-up/Pull-downs

| Parameter | Description | Test Conditions | Min. | Typ. ⁽¹⁾ | Max. | Units |
|-----------|------------------------------|---|------|---------------------|------------|-------|
| R2 | Pull-down value on AUX+ path | S0 = 10G_EN = DP_EN# = TBC-4 = 0V VDD = 3.3V, TBC-16 = 3.3V VDD = 0V, TBC-16 = 3.3V | | 88 88 | 105 105 | Kohm |
| R1 | Pull-up value on AUX- path | S0 = 10G_EN = DP_EN# = TBC-4 = 0V VDD = 3.3V, TBC-18 = 0V | | 88 | 105 | Kohm |
| R4 | Pull-down value on LSRx path | S0 = 10G_EN = 0V; DP_EN# = TBC-11 = 3.3V; VDD = 3.3V | 1 | 1.5 | | Mohm |
| R3 | Pull-up value on LSTx path | S0 = 10G_EN = 0V; DP_EN# = VDD; LSTx = 0V VDD = 3.3V | | 8.8 | 10.5 | Kohm |

Notes:

1. Typical values are at VDD = 3.3V, TA = 25°C ambient and maximum loading.
2. See figure 2 for test setup

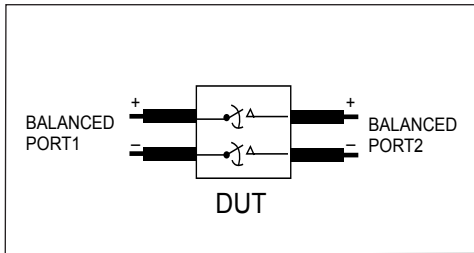


Fig 1: Diff. Insertion Loss and Return Test Circuit

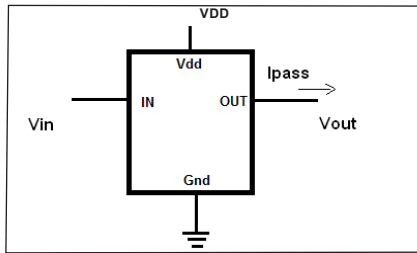


Fig 2: Linear Region Test Setup

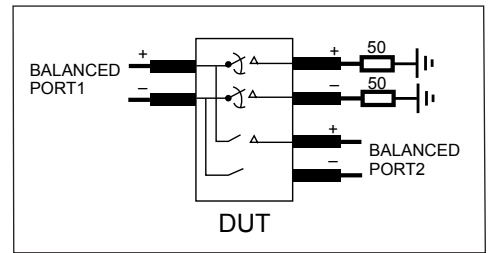
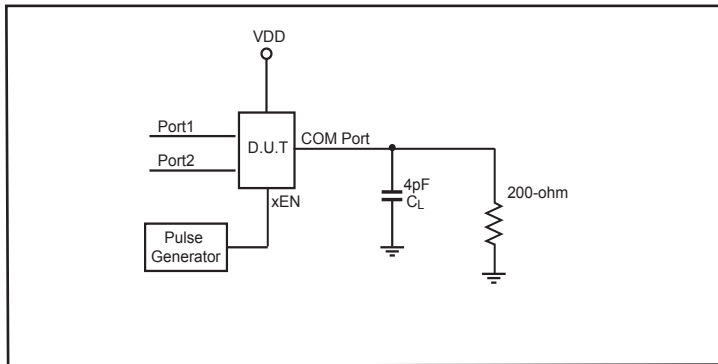


Fig 3: Diff. Off Isolation Test Circuit

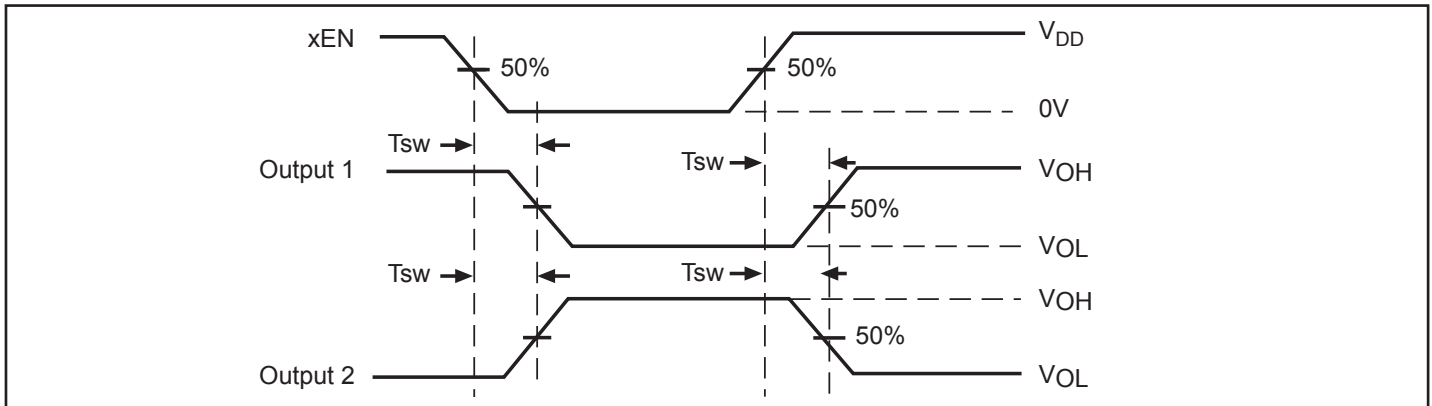
Test Circuit for Electrical Characteristics⁽¹⁻⁵⁾



Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: $PRR \leq \text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.5\text{ns}$, $t_F \leq 2.5\text{ns}$.
5. The outputs are measured one at a time with one transition per measurement.

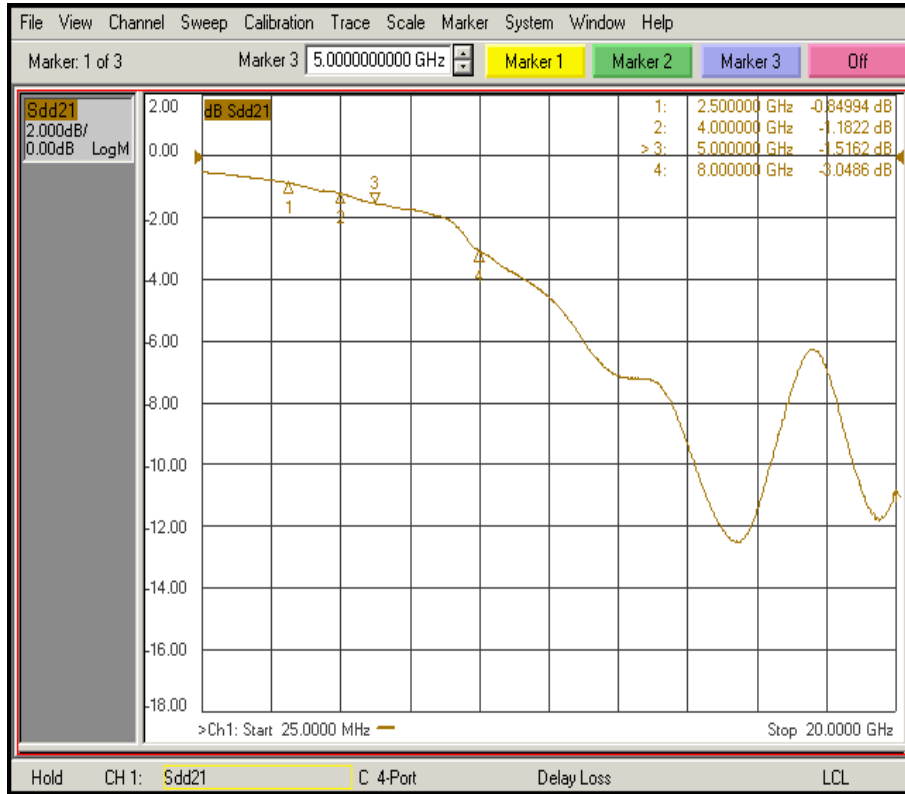
Switching Waveforms



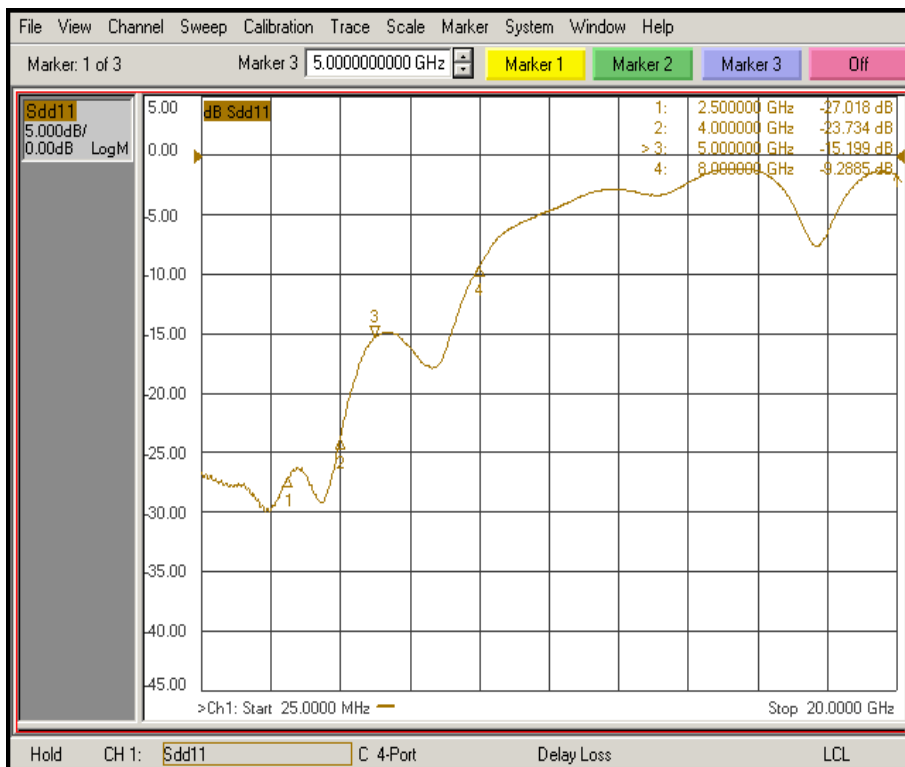
Test Condition:
Output1: Port 1=Low, Port 2=High
Output2: Port 1=High, Port 2=Low

Voltage Waveforms Switching Times

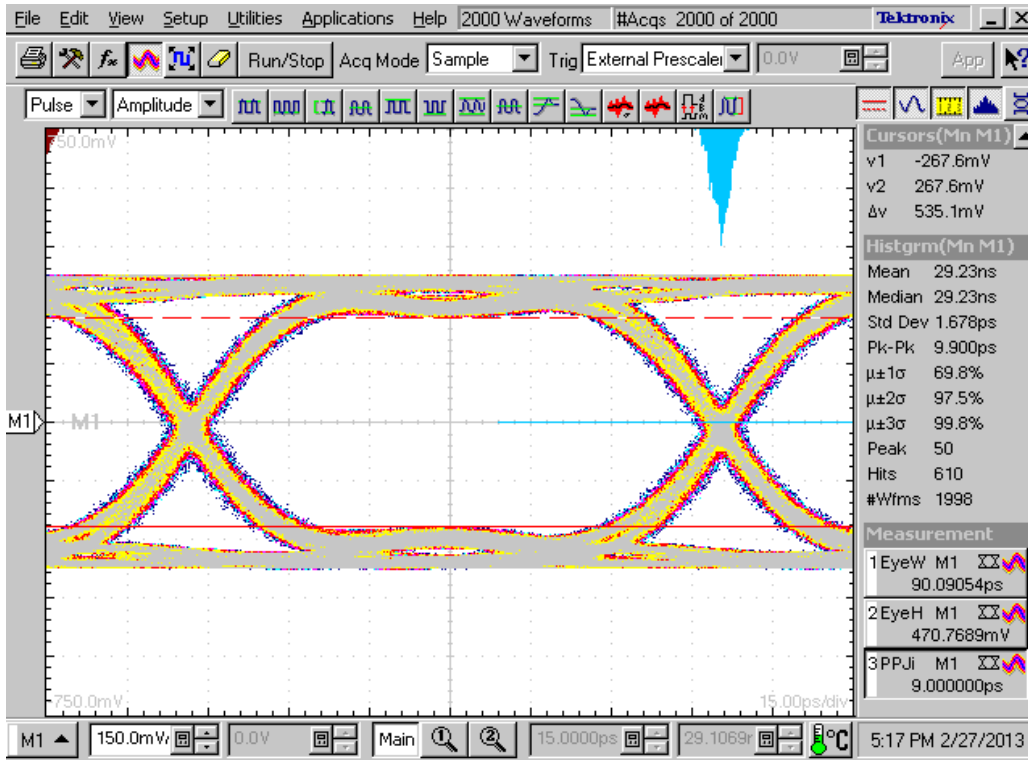
Measured Insertion loss for 10Gbps Thunderbolt Path at $V_{DD} = 3.3V$, $T_A = 25^\circ C$



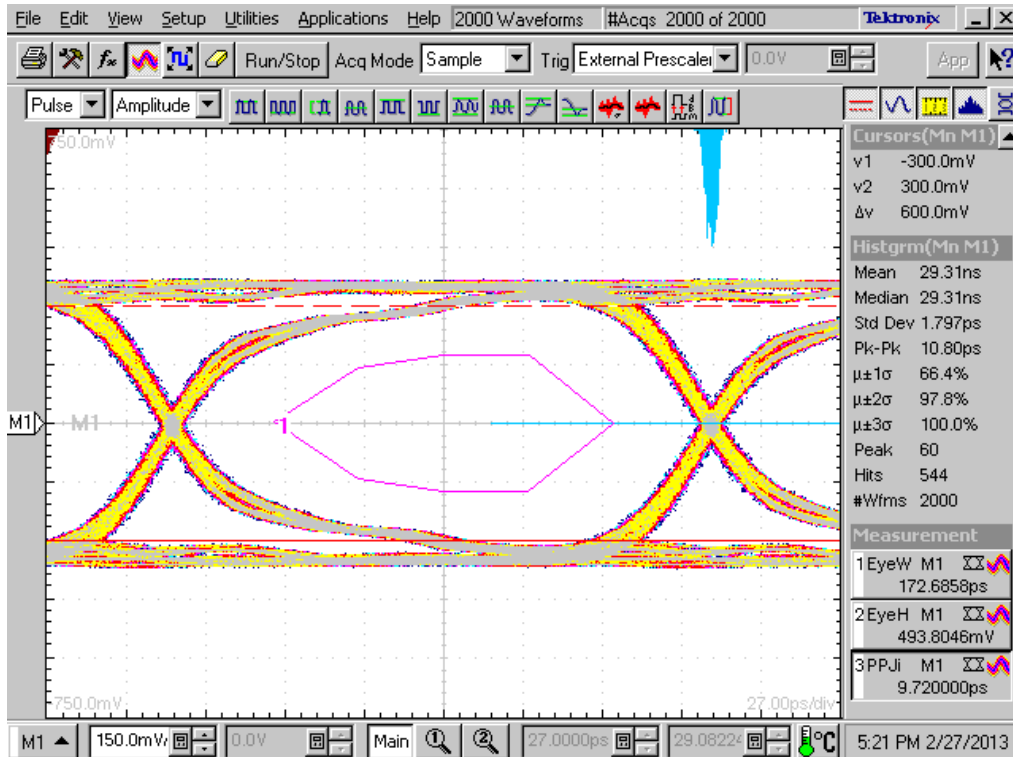
Measured Return loss for 10Gbps Thunderbolt Path at $V_{DD} = 3.3V$, $T_A = 25^\circ C$



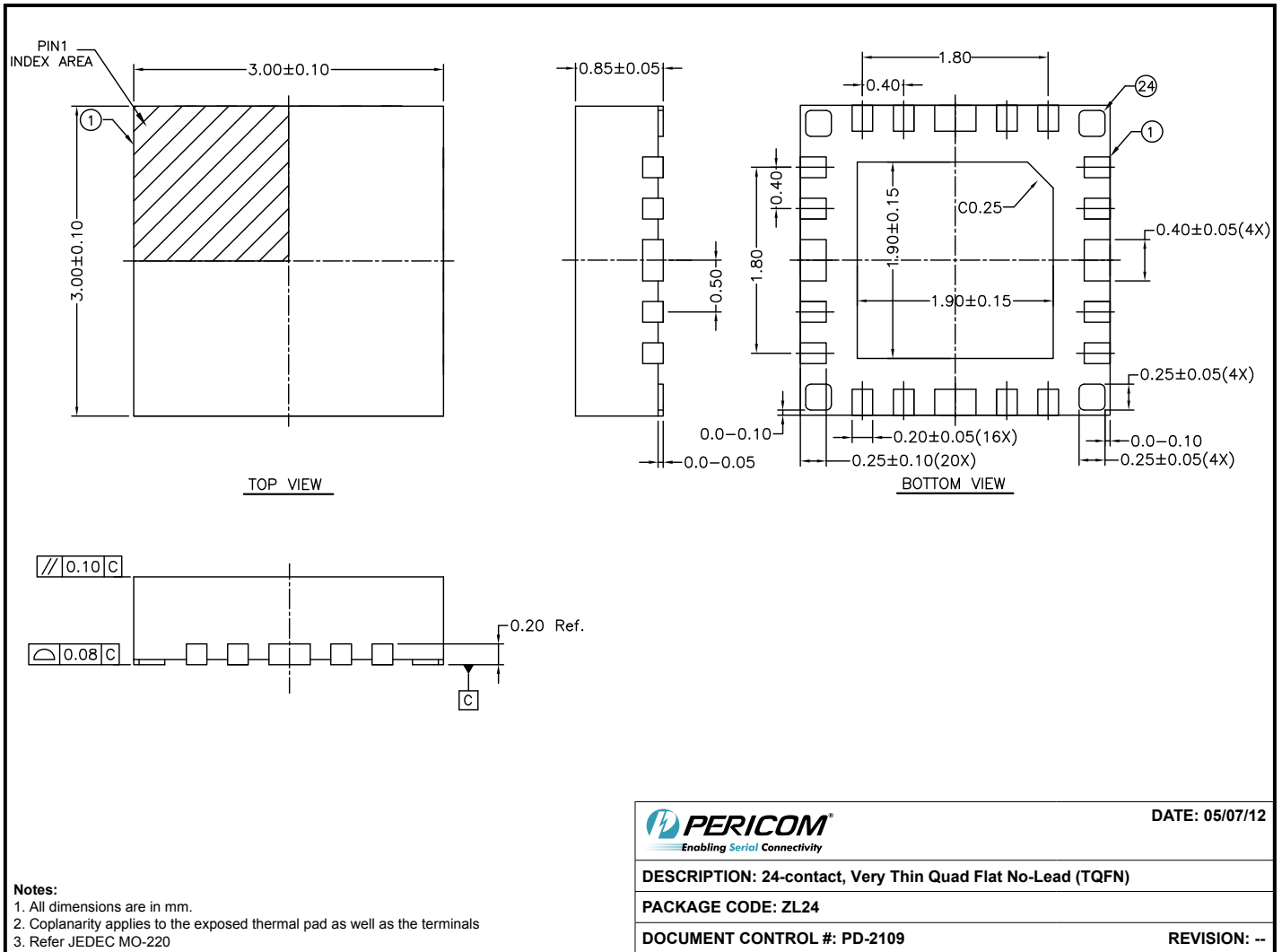
Measured Data Eye for 10.3125 Gbps Thunderbolt Path at $V_{DD} = 3.0V$, $T_A = 25^{\circ}C$, PRBS2⁷⁻¹



Measured Data Eye for 5.4 Gbps Display Port Path at $V_{DD} = 3.0V$, $T_A = 25^{\circ}C$, PRBS2⁷⁻¹



Packaging Mechanical: 24-Contact TQFN



Please check for the latest package information on the Pericom web site at www.pericom.com/packaging/

Ordering Information

| Ordering Number | Package Code | Package Description |
|-----------------|--------------|---------------------------------|
| PI3TB212ZLE | ZL | Pb-free & Green 24-Contact TQFN |

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel