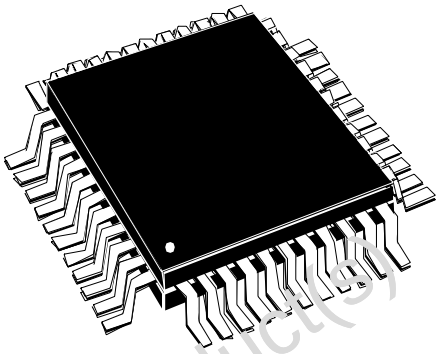
STV6618

Video Switch Matrix for DVDs

Main Features

- **I²C Bus Control**
- **5 Y/CVBS Inputs, 3 Y/CVBS Outputs**
- **3 C Inputs, 1 C Output**
- **2 RGB/YPrPb Inputs, 1 RGB/YPrPb Output**
- **6 dB Gain on all 150 Ω Buffer Outputs**
- **Integrated 150 Ω Buffers**
- **Video Muting on all Outputs**
- **Bottom Clamp on all CVBS/Y, Average Clamp on C Inputs, Bottom Clamp on RGB, Sync-tip Clamp on PrPb signals**
- **Bandwidth: 17 MHz**
- **Crosstalk: 50 dB**



TQFP44
(10 x 10 x 1.4 mm)
(Thin Full Plastic Quad Flat Pack)

ORDER CODE: STV6618

Description

The STV6618 is a highly integrated I²C bus-controlled video switch matrix, optimized for use in recordable Digital Video Disk applications or DVD players. It is adapted to video signals with 1H and 2H formats video routings. It provides required for connections to two external devices (Europe 2 SCARTs), internal tuners, digital encoders and recorders.

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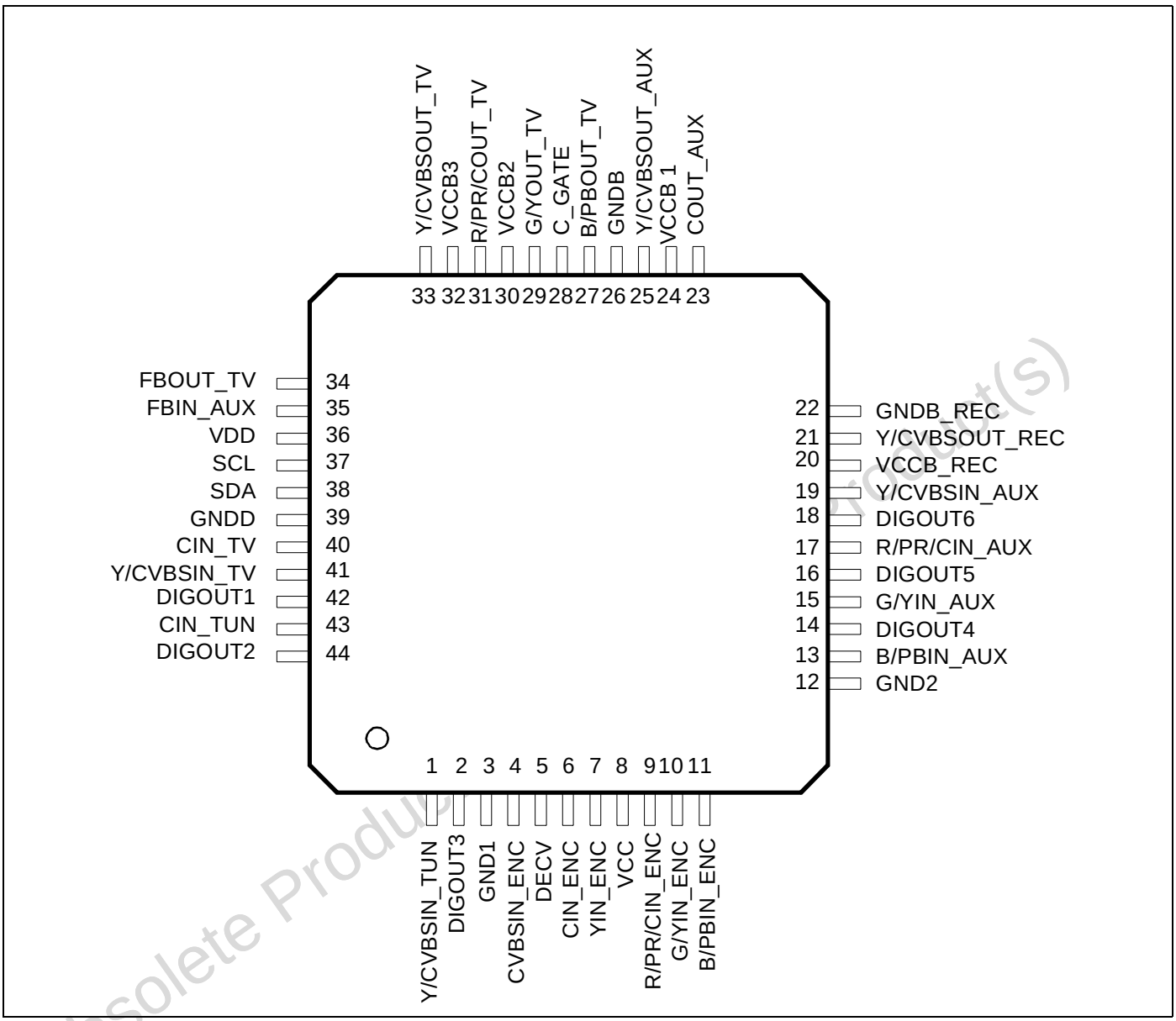
1 GENERAL OVERVIEW

1.1 Pin Connections

Figure 1: Pinout Diagram



1.2 Pin Description

Pin No.	Symbol	Description
1	Y/CVBSIN_TUN	Y/CVBS Input from Tuner
2	DIGOUT3	Digital Output Pin 3
3	GND1	Ground Supply 1 for Video Inputs
4	CVBSIN_ENC	CVBS Input from Encoder
5	DECV	Video decoupling capacitor
6	CIN_ENC	Chroma Input from Encoder
7	YIN_ENC	Y Input from Encoder
8	V_{CC}	+5 V Power Supply for Video Inputs
9	R/PR/CIN_ENC	Red or Pr or Chroma Input from Encoder
10	G/YIN_ENC	Green or Y Input from Encoder
11	B/PBIN_ENC	Blue or Pb Input from Encoder
12	GND2	Ground Supply 2 for Video Inputs
13	B/PBIN_AUX	Blue or Pb Input from Auxiliary (SCART2 or external Cinch)
14	DIGOUT4	Digital Output Pin 4
15	G/YIN_AUX	Green or Y Input from Auxiliary (SCART2 or external Cinch)
16	DIGOUT5	Digital Output Pin 5
17	R/PR/CIN_AUX	Red or Pr or Chroma input from Auxiliary (SCART2 or external Cinch)
18	DIGOUT6	Digital Output Pin 6
19	Y/CVBSIN_AUX	Y/CVBS Input from Auxiliary (SCART2 or external Cinch)
20	VCCB_REC	Video Output Recorder Buffer Supply Pin
21	Y/CVBSOUT_REC	Y/CVBS Output to Recorder
22	GNDB_REC	Ground Supply for Recorder Buffer
23	COUT_AUX	Chroma Output to Auxiliary (SCART2 or external Cinch)
24	VCCB1	Video Output Buffer Supply Pin
25	Y/CVBSOUT_AUX	Y/CVBS Output to Auxiliary (SCART2 or external Cinch)
26	GNDB	Ground Supply for Video Buffer
27	B/PBOUT_TV	Blue or Pb Output to TV (SCART1 or external Cinch)
28	C_GATE	External Transistor Command for Bidirectinnal B/C SCART I/O
29	G/YOUT_TV	Green or Y Output to TV (SCART1 or external Cinch)
30	VCCB2	Video Buffer
31	R/PR/COUT_TV	Red or Pr or Chroma Output to TV (SCART1 or external Cinch)
32	VCCB3	Video Output Buffer Supply Pin
33	Y/CVBSOUT_TV	Y/CVBS Output to TV (SCART1 or external Cinch)
34	FBOUT_TV	Fast Blanking Output to TV (SCART1)
35	FBIN_AUX	Fast Blanking Input from Auxiliary (SCART2)

Pin No.	Symbol	Description
36	VDD	+5 V Digital Power Supply
37	SCL	I²C Bus Clock
38	SDA	I²C Bus Data
39	GNDD	Digital Ground Supply
40	CIN_TV	Chroma Input from TV (SCART1 or external Cinch)
41	Y/CVBSIN_TV	Y/CVBS Input from TV (SCART1 or external Cinch)
42	DIGOUT1	Digital Output Pin 1
43	CIN_TUN	Chroma Input from Tuner
44	DIGOUT2	Digital Output Pin 2

Figure 2: STV6618 Input/Output Diagram

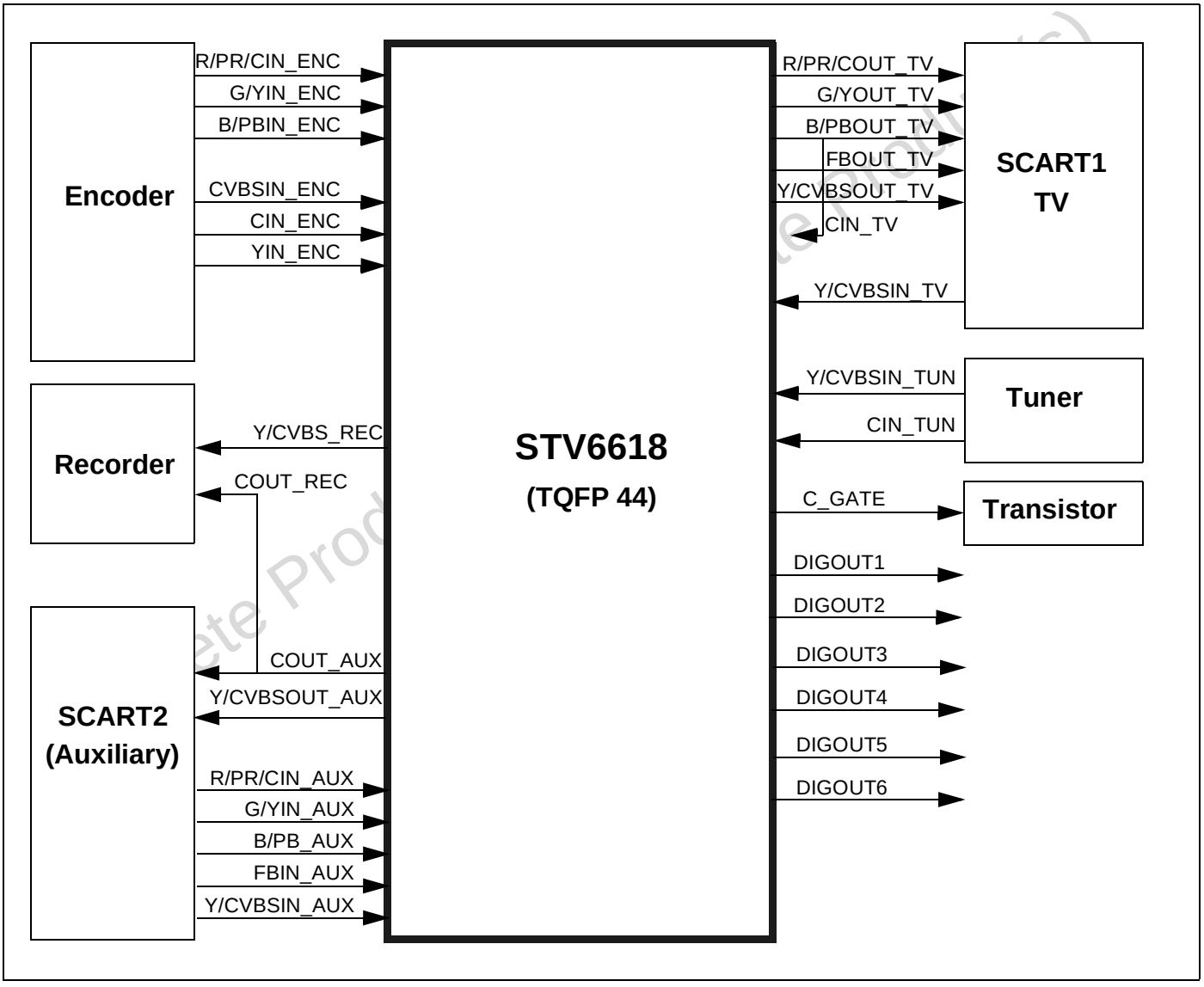
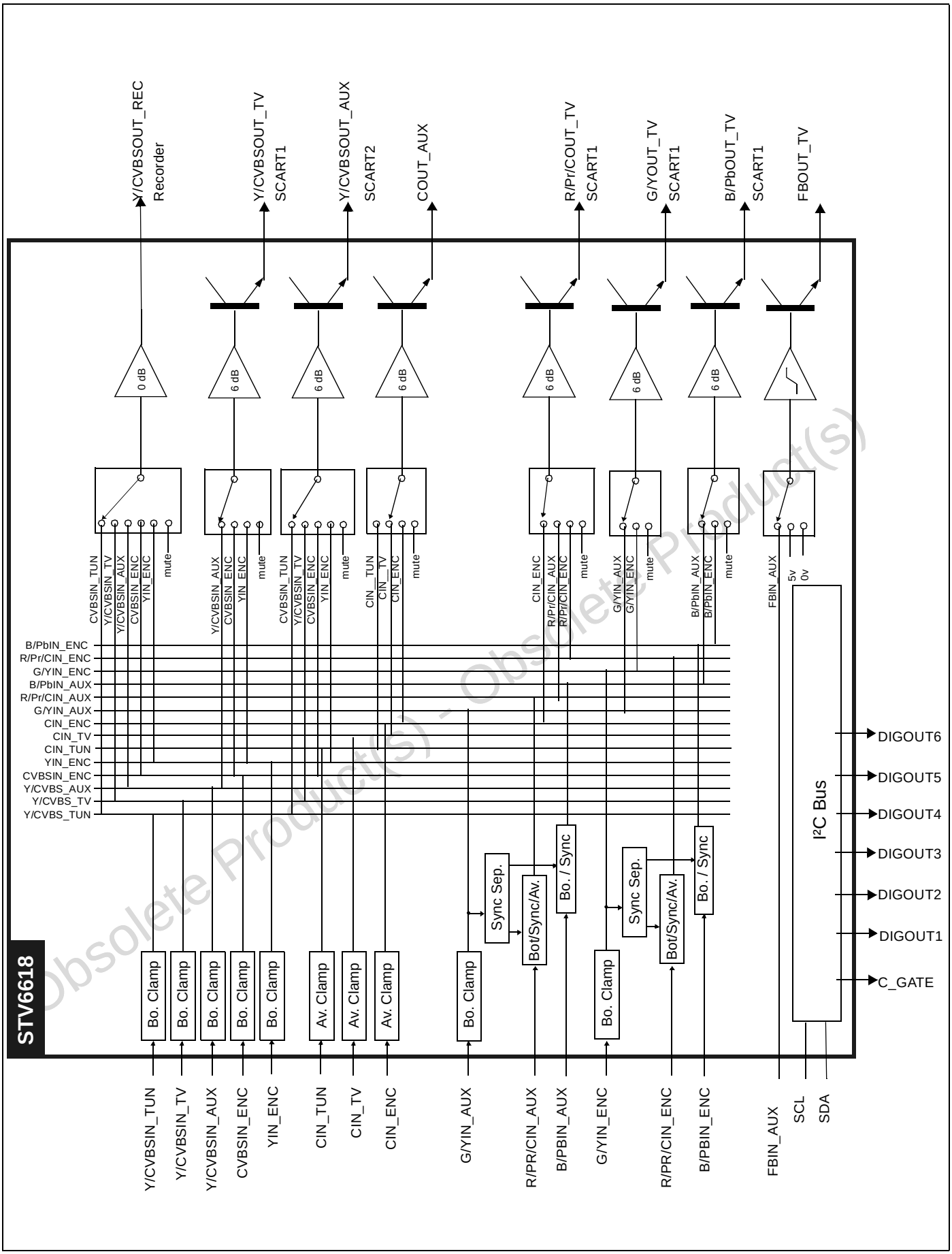


Figure 3: STV6618 Block Diagram



2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Digital Section	6	V
V_{CCV}	Video Section	6	V
V_I	Voltage at Pin 1 to GND - Video pins - Bus pins, DIGOUT1,2,3 and C_GATE	 0, 5.5 0, 5.5	V
$V_{DIGOUT4-5-6}$	Voltage at pin DIGOUT4-5-6	0, 13	V
V_{ESD}	Maximum ESD voltage allowed. 100 pF capacitor discharged through 1.5 kΩ serial resistor (Human Body Model)	±4	kV
T_{OPER}	Operating Ambient Temperature	0, +70	°C
T_{STG}	Storage Temperature	-20, +150	°C

2.2 Thermal Data

Symbol	Parameter	Value	Unit
R_{thJA}	Junction-ambient Thermal Resistance (Maximum) on a single-layer board	70	°C/W

2.3 Recommended Operating Conditions

T_{AMB} = 25 °C, V_{CCV} = 5 V, V_{DD} = 5 V, R_{OUT_VREC} = 4.7 kΩ, R_{OUT_VBUF} = 150 Ω, unless otherwise specified. Output impedances of sources: R_{GV} = 75 Ω.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltages						
V_{DD}	Digital Supply Voltage		4.75	5.00	5.25	V
V_{CCV}	Video Operating Supply Voltage		4.75	5.00	5.25	V
Active Mode (All channels ON)						
I_{DD}	Digital Supply Current	V_{DD} = 5 V,	3.5	5.0	6.5	mA
I_{CCV}	Total Video Supply Current	V_{CCV} = 5 V, No Load	31	45	58	mA
Standby Mode (All channels OFF)						
I_{DD}	Digital Supply Current	V_{DD} = 5 V	3.0	4.5	6.0	mA
I_{CCVSTD}	Total Video Supply Current	V_{CC} = 5 V		0.5	1.0	mA

2.4 Video Section Characteristics

T_{AMB} = 25 °C, V_{CCV} = 5 V, V_{DD} = 5 V, R_{OUT_VREC} = 4.7 kΩ, R_{OUT_VBUF} = 150 Ω, unless otherwise specified. Output impedances of sources: R_{GV} = 75 Ω.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DCIN_BOT}	DC Input Level	Bottom Sync Pulse	1.9	2.0	2.2	V
I_{CLAMP_BOT}	Clamping Current, Bottom clamp	at V_{DCIN} - 400 mV	1	2	3	mA
I_{LEAK}	Input Leakage Current	V_{IN} = V_{DCIN} + 1 V, Bottom clamp input		1	5	µA
V_{DCIN_YSYNC}	DC Input Level	Y input, YPrPb mode, Black Level	2.2	2.3	2.5	V
V_{DCIN_SYNC}	DC Input Level	Sync clamp input (Pr,Pb) Sync signal on Y input	2.9	3.0	3.1	V
I_{CLAMP_SYNC}	Max. Clamping Current during Sync Clamp	Sync clamp input (Pr,Pb) at V_{DCIN} - 400 mV		100		µA
C_{IN}	Input Capacitance			2		pF
V_{IN}	Maximum Input Signal	Y/CVBS, RGB Pr, Pb			1.5 1.0	V_{PP}
DYN	Dynamic Output Signal	Y/CVBS, RGB Pr, Pb			3 2	V_{PP}
BW	Bandwidth at -3 dB Y/CVBS OUT RGB OUT Pr/Pb OUT	 V_{IN} = 0.7 V_{PP} V_{IN} = 0.7 V_{PP} V_{IN} = 0.7 V_{PP}	 14 14 14	 17 17 17		MHz
Flatness	Video Band Gain Spread (15 kHz to 5 MHz) Y/CVBS OUT RGB OUT Pr/Pb OUT	 V_{IN} = 1 V_{PP} V_{IN} = 1 V_{PP} V_{IN} = 0.7 V_{PP}			 ±0.5 ±0.5 ±0.5	dB
CTi	Crosstalk Isolation between Input Channel	V_{IN} = 1 V_{PP} at 4.43 MHz on 1 point	54[1]	60		dB
CTo	Crosstalk Isolation between Output Channel	V_{IN} = 1 V_{PP} at 4.43 MHz on 1 point, R_{LOAD} = 150 Ω	50[1]	55		dB
R_{OUT}	Output Resistance			5	10	Ω
G0V	Gain at video outputs (0 dB), recorder output	V_{IN} = 1 V_{PP} and Gain = 0 dB at 1 MHz	-0.5	0.0	0.5	dB
G6V	Gain at video outputs (6 dB)	V_{IN} = 1 V_{PP} and Gain = 6 dB at 1 MHz	5.5	6.0	6.5	dB
RGBmatch	Gain matching Between RGB outputs	V_{IN} = 0.7 V_{PP} and Gain = 6 dB at 1 MHz	-0.3		0.3	dB
$DC_{OUTZY/CVSS}$	DC Output Voltage, TV and AUX Y/CVBS outputs	Bottom Sync Pulse[2] Mute[2]	0.32 0.57	0.40 0.60	0.43 0.67	V
DC_{OUTREC}	DC Output Voltage, Recorder Y/CVBS Output	Bottom Sync Pulse[2] Mute[2]	1.2 1.3	1.3 1.4	1.4 1.5	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC_{OUTRGB}	DC Output Voltage, RGB outputs	Black Level[2] Mute[2]	0.45 0.50	0.60 0.60	0.70 0.70	V
$DC_{OUTYOUT}$	DC Output Voltage, TV Y Output (G/YOUT_TV, YPrPb mode)	Bottom Sync Pulse[2] Mute[2]	0.50 0.45	0.60 0.60	0.70 0.70	V
$DC_{OUTPrPb}$	DC Output Voltage, PrPb outputs	Black Level[2] Mute[2]	1.4 1.4	1.5 1.5	1.6 1.6	V
DPHI	Differential Phase, Y/CVBS	V_{IN} = 1 V_{PP} at 4.43 MHz		0.2	2.5	deg.
DG	Differential Gain, Y/CVBS	V_{IN} = 1 V_{PP} at 4.43 MHz		0.3	5	%
Mute	Mute Suppression	V_{IN} = 1 V_{PP} at 5 MHz on 1 point	-55			dB
LNL	Luminance non-linearity			0.3	3	%
VSN	Video Signal-to-Noise Ratio[3]		75			dB

1. Minimum Crosstalk values estimated during Qualification phase, based on ST Evaluation Board measurement, TQFP44 package soldered on board.
2. Measured at IC output pin.
3. Signal-to-Noise = 20log (VOUTblack-to-white = 0.7 V_{PP} / Vnoise(mVrms) weighted CCIR 567)

2.5 Fast Blanking Section Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT MODE						
$FB_{LOW/HIGH}$	Input Low/High Level Threshold		0.4	0.7	0.9	V
I_{IN}	Input Current			2	10	µA
OUTPUT MODE						
FB_{LOW}	Output Low Level	R_{LOAD} = 150 Ω			0.5	V
FB_{HIGH}	Output High Level	R_{LOAD} = 150 Ω	3.0	3.4	3.8	V
FB_{DEL}	Fast Blanking RGB delay	At 50% on digital RGB transients, at 2 V on FB rise transient, at 1 V on FB fall, C_{LOAD} = 10 pF maximum		15		ns
FB_{TRANS}	FB Transitions at FB output Rise Time Fall Time	C_{LOAD} = 10 pF maximum between 10% and 90% between 90% and 10%		 10 10		ns

2.6 Chroma Section Characteristics

T_{AMB} = 25 °C, V_{CCV} = 5 V, V_{DD} = 5 V, R_{OUT_VREC} = 4.7 kΩ, R_{OUT_VBUF} = 150 Ω, unless otherwise specified. Output impedances of sources: R_{GV} = 75 Ω.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DCIN}	DC Input Level		2.9	3.0	3.1	V
R_{IN}	Input Resistance		30	50		kΩ
C_{IN}	Input Capacitance			2		pF
V_{IN}	Max Input Signal				1.0	V_{PP}
DYN	Dynamic Output Signal				2.0	V_{PP}
DC_{OUT}	DC Output Voltage AUX C Output	No Chroma input signal[1]	1.4	1.5	1.6	V
CBW	Chroma Bandwidth	V_{IN} = 1 V_{PP} at -3 dB	10	15		MHz
CTi	Crosstalk Isolation between Input Channel	V_{IN} = 1 V_{PP} at 4.43 MHz, on one input	54[2]	60		dB
CTo	Crosstalk Isolation between Output Channel	V_{IN} = 1 V_{PP} at 4.43 MHz, on one input, R_{LOAD} = 150 Ω	50 [2]	55		dB
R_{OUT}	Output Resistance			5	10	Ω
G6C	Gain at Chroma Outputs	V_{IN} = 1 V_{pp} and Gain = 6 dB at 1 MHz	5.5	6.0	6.5	dB
Mute	Mute Suppression	V_{IN} = 1 V_{PP} at 4.43 MHz, on one input	-55			dB
CToYdel	Chroma to Luma Delay, Source Y/C	V_{IN} = V_{PP} at 4.43 MHz			20	ns

1. Measured at IC output pin.
2. Minimum Crosstalk values estimated during Qualification phase, based on ST Evaluation Board measurement, TQFP44 package soldered on board.

2.7 Digital Outputs

T_{AMB} = 25 °C, V_{CCV} = 5 V, V_{DD} = 5 V.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_gate_H	Pull-up resistor value to VccB3		16	20	24	kΩ
C_gate_L	Output Low level	I_{IN} = 0 mA I_{IN} = 1 mA			0.3 0.7	V
C_gate_H	Output High level	R_{LOAD} = 20 kΩ			V_{DD}	V
DIGOUT1-2-3 Load	External pull-up resistor value to VDD			10		kΩ
DIGOUT1-2-3 Low	Output low level, DIGOUT1-2-3	R_{LOAD} = 10 kΩ			0.7	V
DIGOUT1-2-3 Middle	Output middle level, DIGOUT1-2-3	R_{LOAD} = 10 kΩ		2.2		V
DIGOUT1-2-3 High	Output high level,DIGOUT1-2-3	R_{LOAD} = 10 kΩ, Opened collector output			V_{DD}	V
DIGOUT4-5-6 Low	Output low level, DIGOUT4-5-6	I_{LOAD} = 2 mA			0.7	V
DIGOUT4-5-6 High	Output high level, DIGOUT4-5-6	Opened Collector Output			13	V

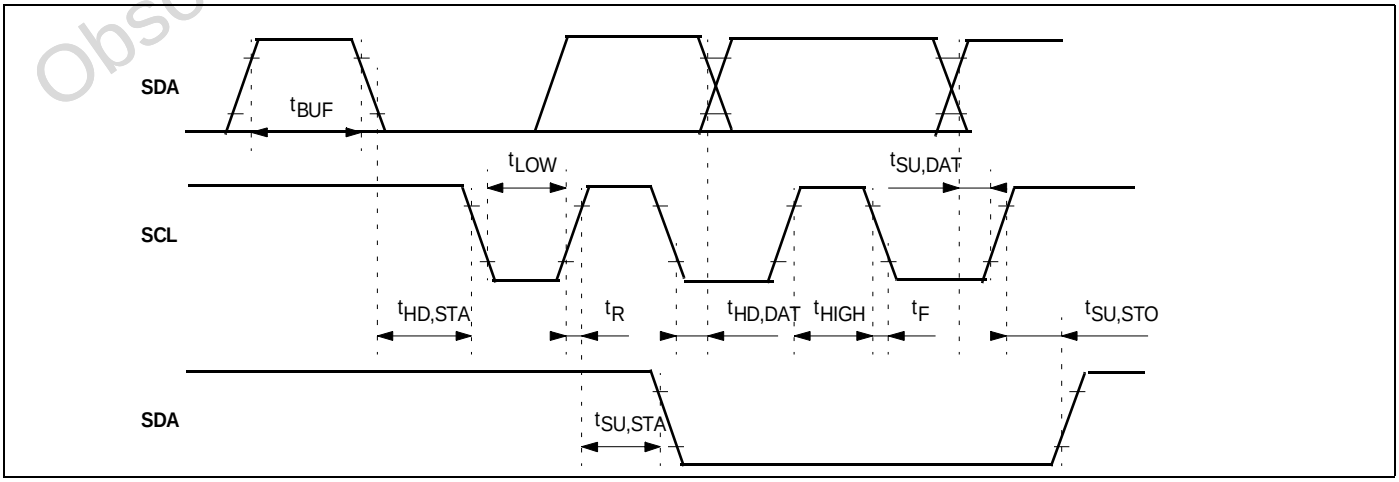
2.8 I²C Bus Characteristics

T_{AMB} = 25 °C, V_{CCV} = 5 V, V_{DD} = 5 V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SCL						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		2.3		5.5	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V	-10	0	10	µs
SDA						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		2.3		5.5	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V	-10	0	10	µs
C_I	Input Capacitance				10	pF
t_R	Input Rise Time	1.5 V to 3 V			1	µs
t_F	Input Fall Time	3 V to 1.5 V			300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3 mA			0.4	V
t_F	Output Fall Time	3 V to 1.5 V			250	ns
C_L	Load Capacitance				400	pF
TIMING						
t_{LOW}	Clock Low Period		4.7			µs
t_{HIGH}	Clock High Period		4			µs
$t_{SU,DAT}$	Data Setup Time		250			ns
$t_{HD,DAT}$	Data Hold Time		0		340	ns
$t_{SU,STO}$	Setup Time from Clock High to Stop		4			µs
t_{BUF}	Start Setup Time following a Stop		4.7			µs
$t_{HD,STA}$	Start Hold Time		4			µs
$t_{SU,STA}$	Start Setup Time following Clock Low to High Transition		4.7			µs

Note: The device can also operate at 400 kHz and can interface with +3.3 V or + 5 V logic levels.

Figure 4: I²C Bus Timing



3 I²C BUS SELECTION

Data transfers follow the usual I²C format; i.e. after the start condition (S), a 7-bit slave address is sent, followed by an eight-bit data direction bit (W). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register. The IC's I²C bus decoder enables the automatic incrementation mode in write mode.

String Format

Write only mode (S = Start condition, P = Stop condition, A = Acknowledge)

S	Slave Address	0	A	Sub-address	A	Data	A	P

Read only mode

S	Slave Address	1	A	Data	A	P

Slave Address

Address	A7	A6	A5	A4	A3	A2	A1
Value	1	0	0	1	0	1	0

Auto Increment Mode

S	Slave Address	0	A	Sub-address	A	DATA0	A	DATA1	A	....	DATAn	A	P
						Sub-Address		Sub-Address +1			Sub-Address + N		

3.1 I²C Bus Addresses

Write Address: 1001 0100 = 94(hex)
Input Signal Summary (Write Mode)

Reg Addr (Hex)	Data							
	d7	**d6**	**d5**	**d4**	**d3**	**d2**	**d1**	**d0**
Y/CVBS and C Output Selection								
00	DigOUT6	Not Used		TV Y/CVBS Output Selection		Recorder Y/CVBS Output Selection		
01	DigOUT5	Not Used		Auxiliary C Output Selection		Auxiliary Y/CVBS Output Selection		
RGB/YPrPb & Fast Blanking Selection								
02	RGB/YPrPb High Impedance State		RGB or YPrPb or C mode Selection		Auxiliary or Encoder Selection		Fast Blanking Selection	
Digital Outputs								
03	DIGOUT4	DIGOUT3		DIGOUT2 Control		DIGOUT1 Control		C_GATE Control

Reg Addr (Hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
Standby								
04	TV Output Standby	AUX Chroma Output Standby	AUX CVBS Output Standby	REC Output Standby	AUX Input Disable	TV Input Disable	TUN Input Disable	ENC Input Disable

Note: Unused data must be set to "0".

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
00	Recorder Y/CVBS Output Selection	3	X	X	X	X	X	0	0	0	Mute
			X	X	X	X	X	0	0	1	YIN_ENC
			X	X	X	X	X	0	1	0	CVBSIN_ENC
			X	X	X	X	X	0	1	1	Y/CVBSIN_AUX
			X	X	X	X	X	1	0	0	Y/CVBSIN_TV
			X	X	X	X	X	1	0	1	YCVBSIN_TUN
			X	X	X	X	X	1	1	0	Not allowed
			X	X	X	X	X	1	1	1	Not allowed
	TV Y/CVBS Output Selection	2	X	X	X	0	0	X	X	X	Y/CVBS_AUX
			X	X	X	0	1	X	X	X	YIN_ENC
			X	X	X	1	0	X	X	X	CVBSIN_ENC
			X	X	X	1	1	X	X	X	Mute
	DigOUT6 Control	1	0	X	X	X	X	X	X	X	0 = Low Level
			1	X	X	X	X	X	X	X	1 = High Level
01	AUX (SCART2) Y/CVBS Output Selection	3	X	X	X	X	X	0	0	0	Y/CVBSin_TV
			X	X	X	X	X	0	0	1	YIN_ENC
			X	X	X	X	X	0	1	0	CVBSIN_ENC
			X	X	X	X	X	0	1	1	YCVBSIN_TUN
			X	X	X	X	X	1	0	0	Mute
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
			X	X	X	X	X	1	1	1	Not allowed
	AUX (SCART2) Chroma Output Selection	2	X	X	X	0	0	X	X	X	Mute
			X	X	X	0	1	X	X	X	CIN_ENC
			X	X	X	1	0	X	X	X	CIN_TV
			X	X	X	1	1	X	X	X	CIN_TUN
	DigOUT5 Control	1	0	X	X	X	X	X	X	X	0 = Low Level
			1	X	X	X	X	X	X	X	1 = High Level

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
02	Fast Blanking Output Control	2	X	X	X	X	X	X	0	0	FBIN_AUX
			X	X	X	X	X	X	0	1	FB forced to Low Level
			X	X	X	X	X	X	1	0	FB forced to High Level
			X	X	X	X	X	X	1	1	Not allowed
	RGB/YPrPb Output Selection	2	X	X	X	X	0	0	X	X	RGB/YPrPb_AUX
			X	X	X	X	0	1	X	X	RGB/YPrPb_ENC
			X	X	X	X	1	0	X	X	CIN_ENC (pin 6) at R/Pr/COUT_TV, B/PbOUT & G/YOUT muted
			X	X	X	X	1	1	X	X	RGB/YPrPb mute
	RGB or YPrPb or C Selection	2	X	X	0	0	0	0	X	X	RGB mode selection, bottom clamp at RGB inputs, AUX. input selected
			X	X	0	0	0	1	X	X	RGB mode selection, bottom clamp at RGB inputs, ENC. input selected
			X	X	0	1	0	0	X	X	CIN_AUX (pin 17)selected, average clamp at R/Pr/CIN_AUX input, GIN_AUX (bottom clamp) selected, BIN_AUX (bottom clamp) selected
			X	X	0	1	0	1	X	X	CIN_ENC (pin 9)selected, average clamp at R/Pr/CIN_ENC input, GIN_ENC (bottom clamp) selected, BIN_ENC (bottom clamp) selected
			X	X	1	0	0	0	X	X	YPrPb mode selection, sync pulse clamp at Pr Pb inputs, black clamp at Y input, AUX. input selected
			X	X	1	0	0	1	X	X	YPrPb mode selection, sync pulse clamp at Pr Pb inputs, black clamp at Y input, ENC. input selected
			X	X	1	1	0	0	X	X	YPrPb mode selection, delayed sync pulse clamp at Pr Pb inputs, black clamp at Y input, AUX. input select
			X	X	1	1	0	1	X	X	YPrPb mode selection, delayed sync pulse clamp at Pr Pb inputs, black clamp at Y input, ENC. input select
	RGB/YPrPb Control	2	0	0	X	X	X	X	X	X	RGB/YPrPb outputs active
			0	1	X	X	X	X	X	X	RGB/YPrPb outputs high imp state
			1	X	X	X	X	X	X	X	Red output active, Green and Blue high imp. state

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
03	C_Gate Output Control	1	X X	X X	X X	X X	X X	X X	X X	0 1	Low Level High Level
	DIGOUT1	2	X X X	X X X	X X X	X X X	X X X	0 1 1	X 0 1	X X X	Low Level Mid Level High Level
	DIGOUT2	2	X X X	X X X	X X X	0 1 1	X 0 1	X X X	X X X	X X X	Low Level Mid Level High Level
	DIGOUT3	2	X X X	0 1 1	X 0 1	X X X	X X X	X X X	X X X	X X X	Low Level Mid Level High Level
	DIGOUT4 Control	1	0 1	X X	X X	X X	X X	X X	X X	X X	0 = Low Level 1 = High Level
04	ENC Inputs	1	X X	X X	X X	X X	X X	X X	X X	0 1	Inputs Active Inputs Disabled
	TUN Inputs	1	X X	X X	X X	X X	X X	X X	0 1	X X	Inputs Active Inputs Disabled
	TV Inputs	1	X X	X X	X X	X X	X X	0 1	X X	X X	Inputs Active Inputs Disabled
	AUX Inputs	1	X X	X X	X X	X X	0 1	X X	X X	X X	Inputs Active Inputs Disabled
	REC Outputs	1	X X	X X	X X	0 1	X X	X X	X X	X X	Y/CVBSOUT_REC Outputs ON Y/CVBSOUT_REC Outputs OFF
	AUX Outputs	1	X X	X X	0 1	X X	X X	X X	X X	X X	Y/CVBSOUT_AUX Outputs ON Y/CVBSOUT_AUX Outputs OFF
	COUT_AUX Output	1	X X	0 1	X X	X X	X X	X X	X X	X X	COUT_AUX Outputs ON COUT_AUX Outputs OFF (high imped.)
	TV Outputs	1	0 1	X X	X X	X X	X X	X X	X X	X X	TV Video Outputs ON TV Video Outputs OFF
	Full Stop	8	1	1	1	1	1	1	1	1	Only I²C bus supplied, and digital outputs

3.2 Power-on Reset: Bus Register Initial Conditions

Power-on Reset is active when supply V_{DD} < 3.5 V. Non-significant bits (X) are pre-set to “0”.

Reg. Addr (Hex)	Data								Comments
	d7	d6	d5	d4	d3	d2	d1	d0	
00	0	0	0	0	0	0	0	0	Rec. CVBS output muted, TV CVBS output to Aux. CVBS input, Digital output low level
01	0	0	0	0	0	0	0	0	Aux. CVBS output to TV CVBS input, Aux. Chroma output muted, Digital output low level
02	0	0	0	0	0	0	0	0	FB output to Aux. FB input, TV RGB output to Aux. RGB inputs, RGB outputs active
03	0	0	0	0	0	0	0	0	C_gate output low level, DIGOUT outputs low level
04	0	0	0	0	0	0	0	0	All inputs outputs active

4 INPUT/OUTPUT GROUPS

Figure 5: C_Gate Logic Output (Pin 28)

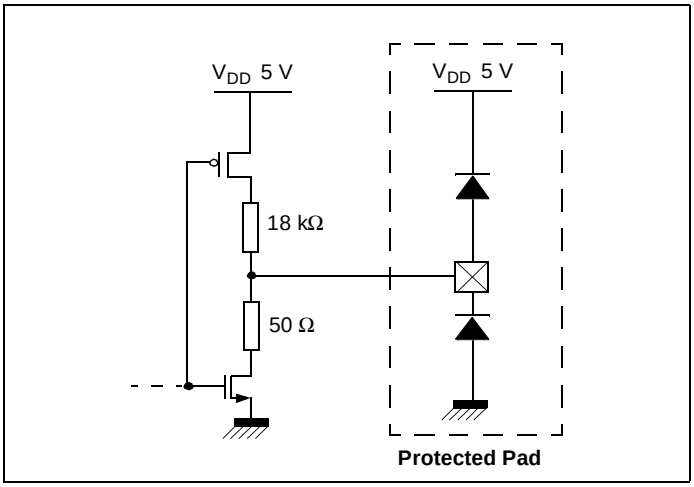


Figure 6: Video Outputs (Pins 23, 25, 27, 29, 31 and 33)

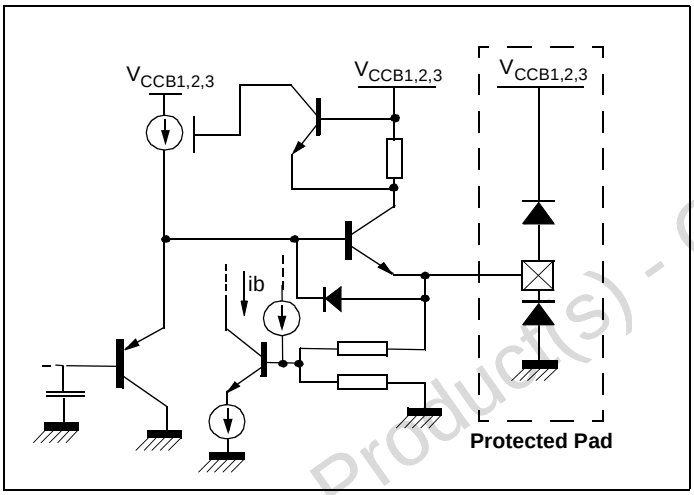


Figure 7: YCVBSOUT_REC Recorder Output (Pin 21)

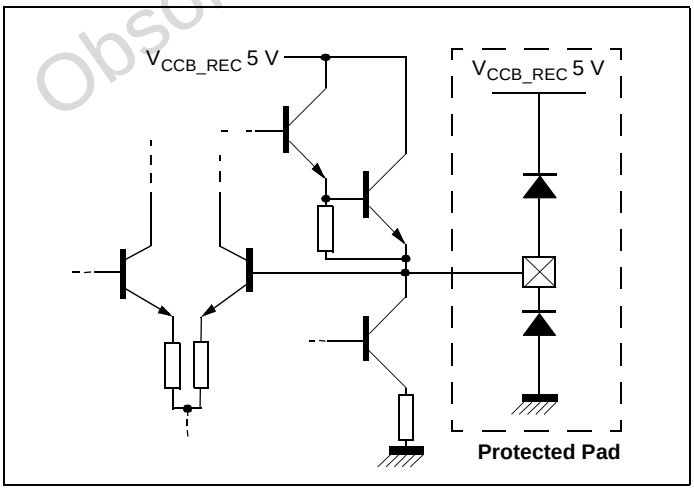


Figure 8: Fast Blanking Inputs (Pin 35)

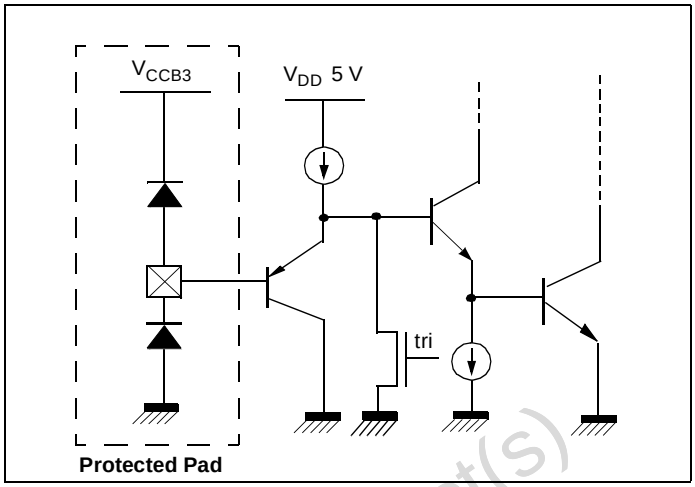


Figure 9: I²C Bus SCL I/O (Pin 37)

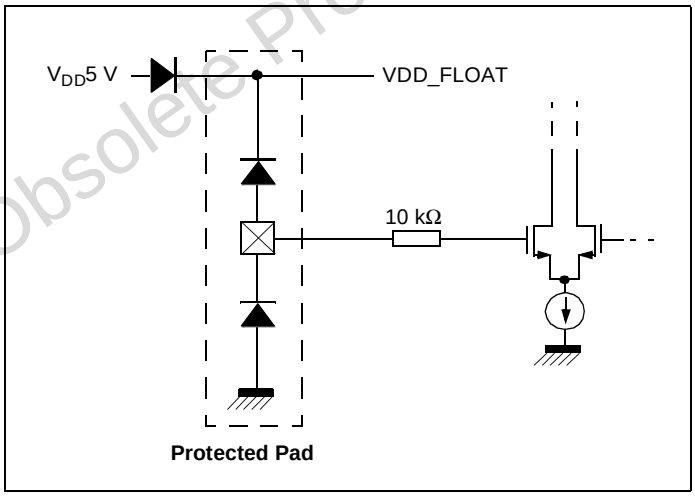


Figure 10: Fast Blanking Output (Pin 34)

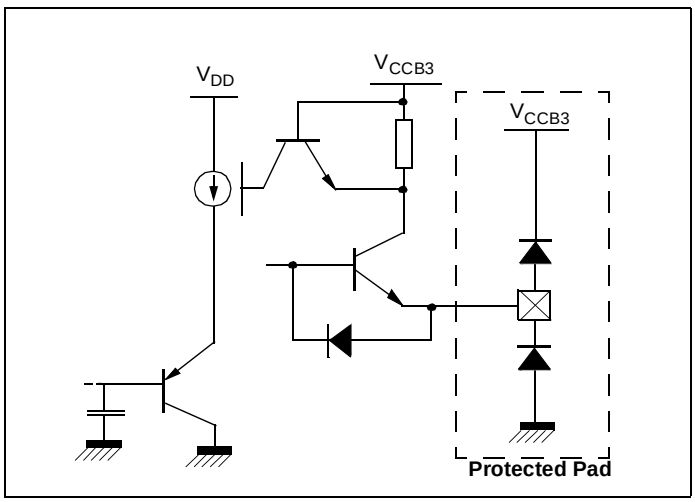


Figure 11: Bottom Clamped Video Inputs (Pins 1, 4, 7, 19 and 41)

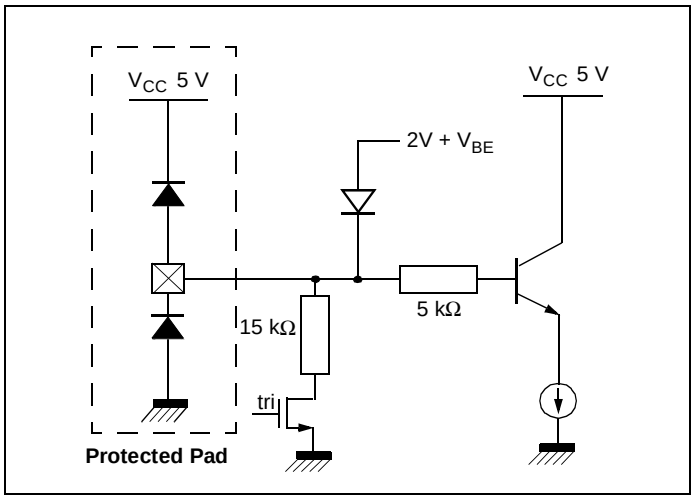


Figure 12: DIGOUT 1, 2 and 3 (Pins 42, 44 and 2)

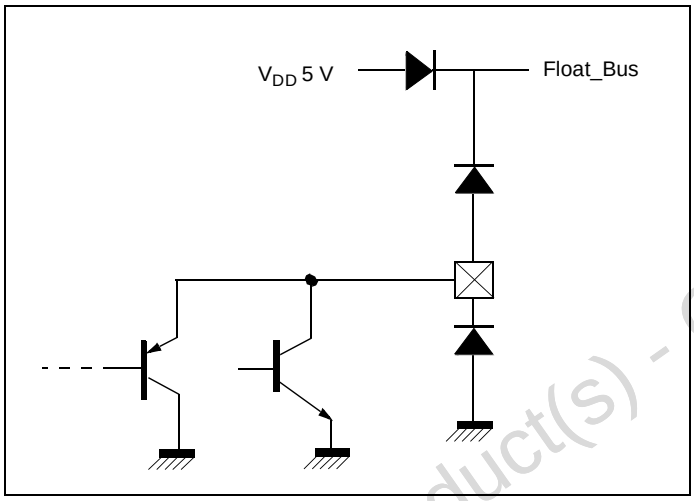


Figure 13: DIGOUT 4, 5 and 6 (Pins 14, 16 and 18)

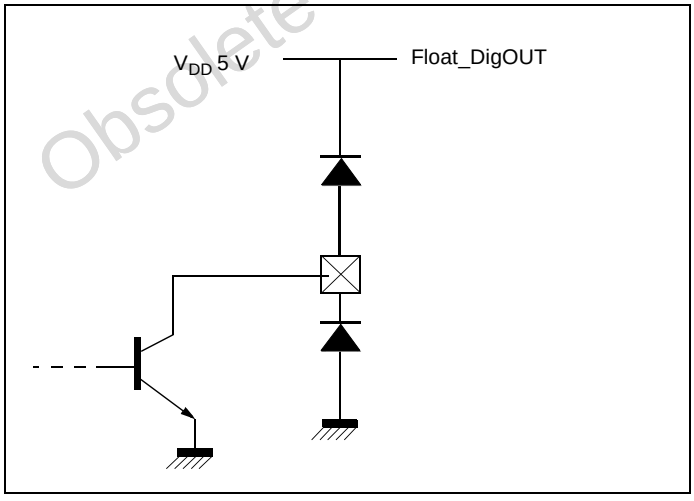


Figure 14: Average Clamped Video Inputs (Pins 6, 40 and 43)

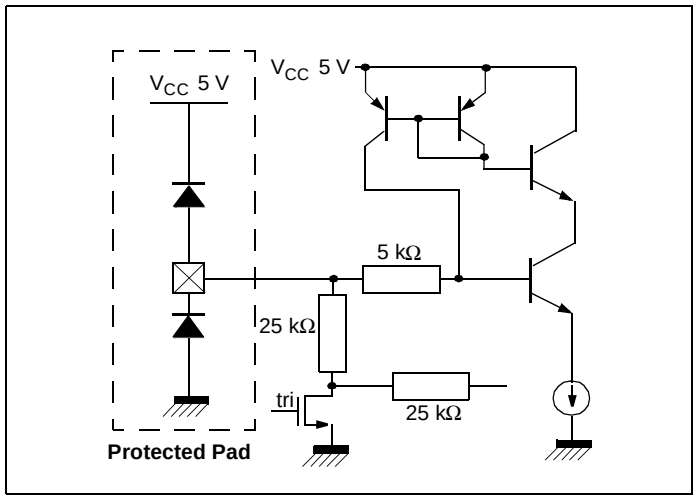


Figure 15: DECV (Pin 5)

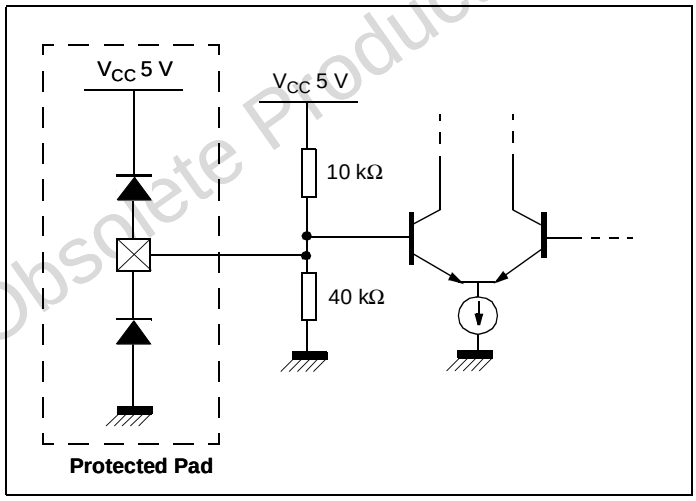


Figure 16: I²C Bus SDA I/O (Pin 38)

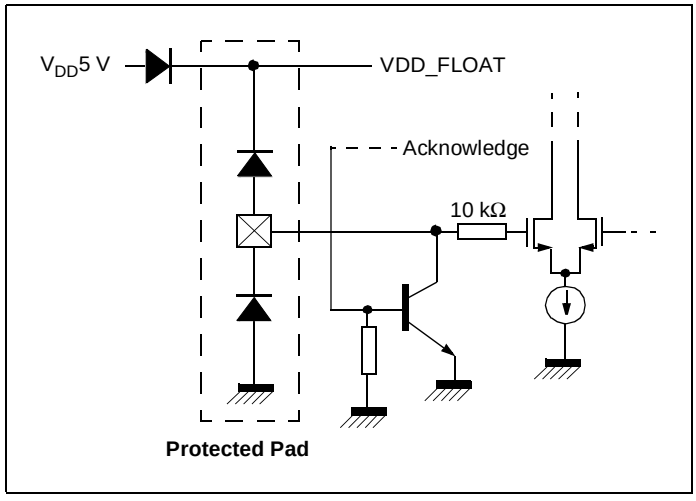


Figure 17: R/Pr/C Inputs (Pins 9 and 17)

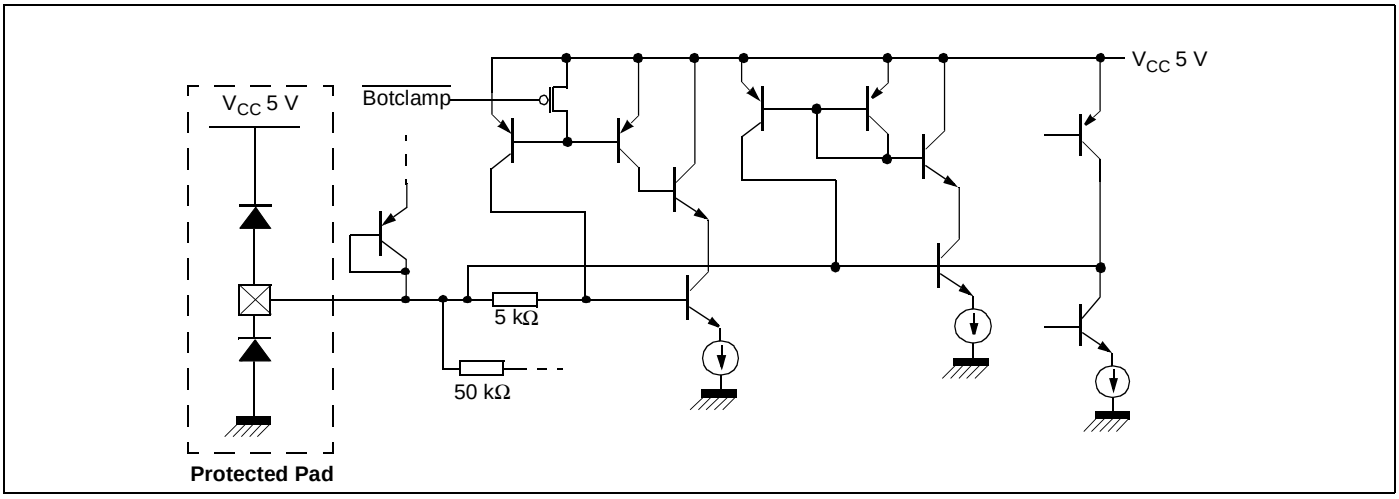


Figure 18: G/Y Inputs (Pins 10 and 15)

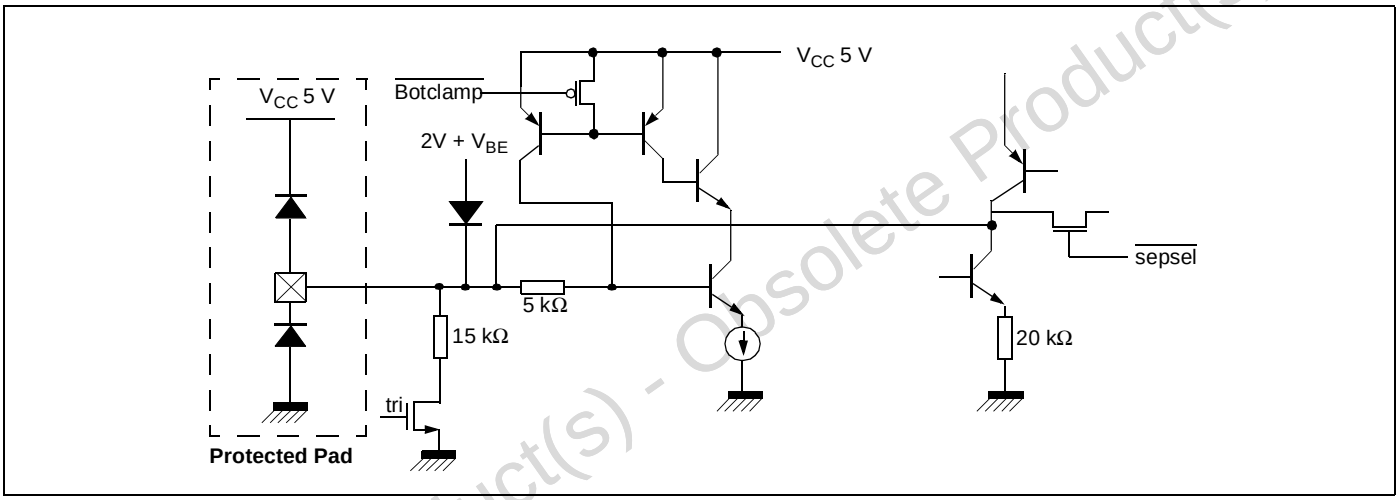


Figure 19: B/Pb Inputs (Pins 11 and 13)

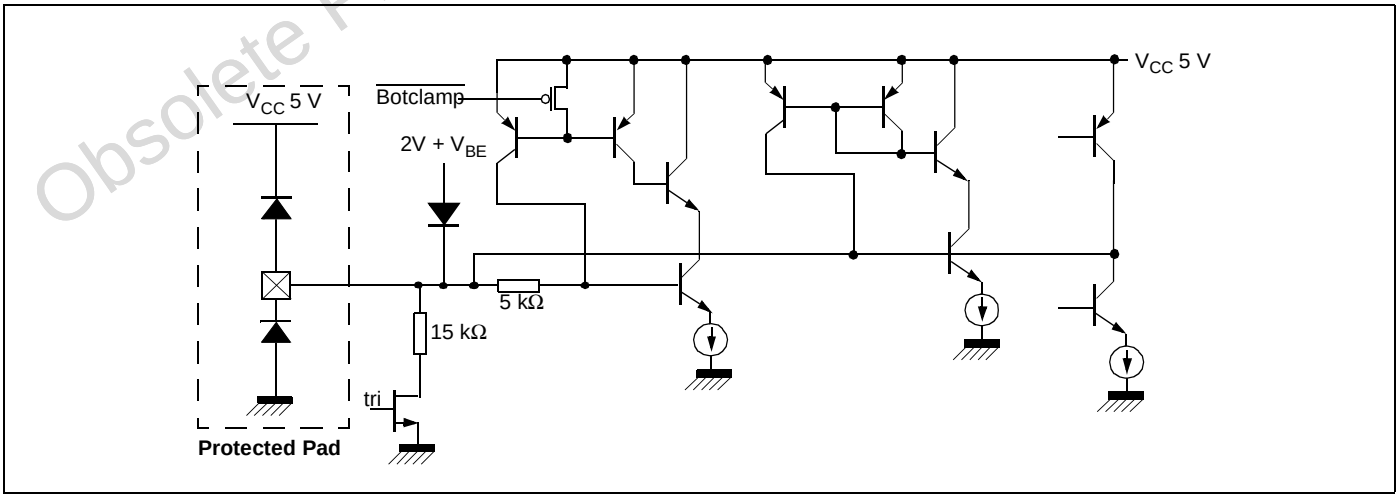
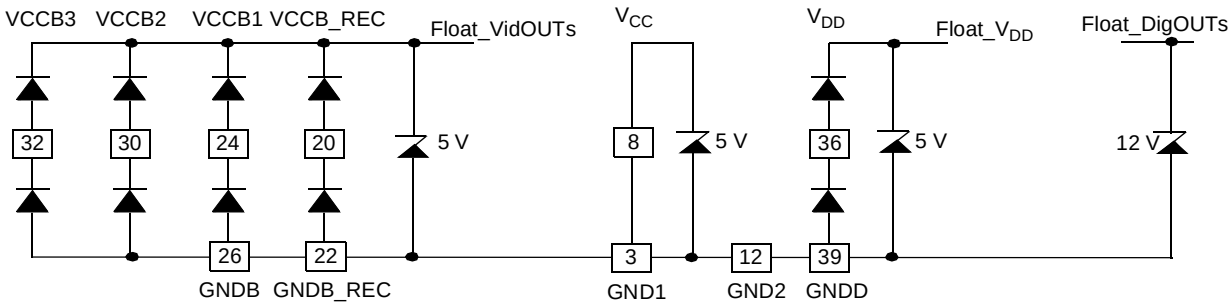
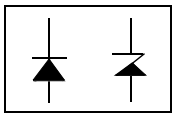


Figure 20: Power Supply Connection





These symbols represent some huge diode and Zener-like components used for ESD protection of the device.
They are not supposed to be paths for any current in normal operation mode.

5 APPLICATION DIAGRAMS

Figure 21: YPrPb Application

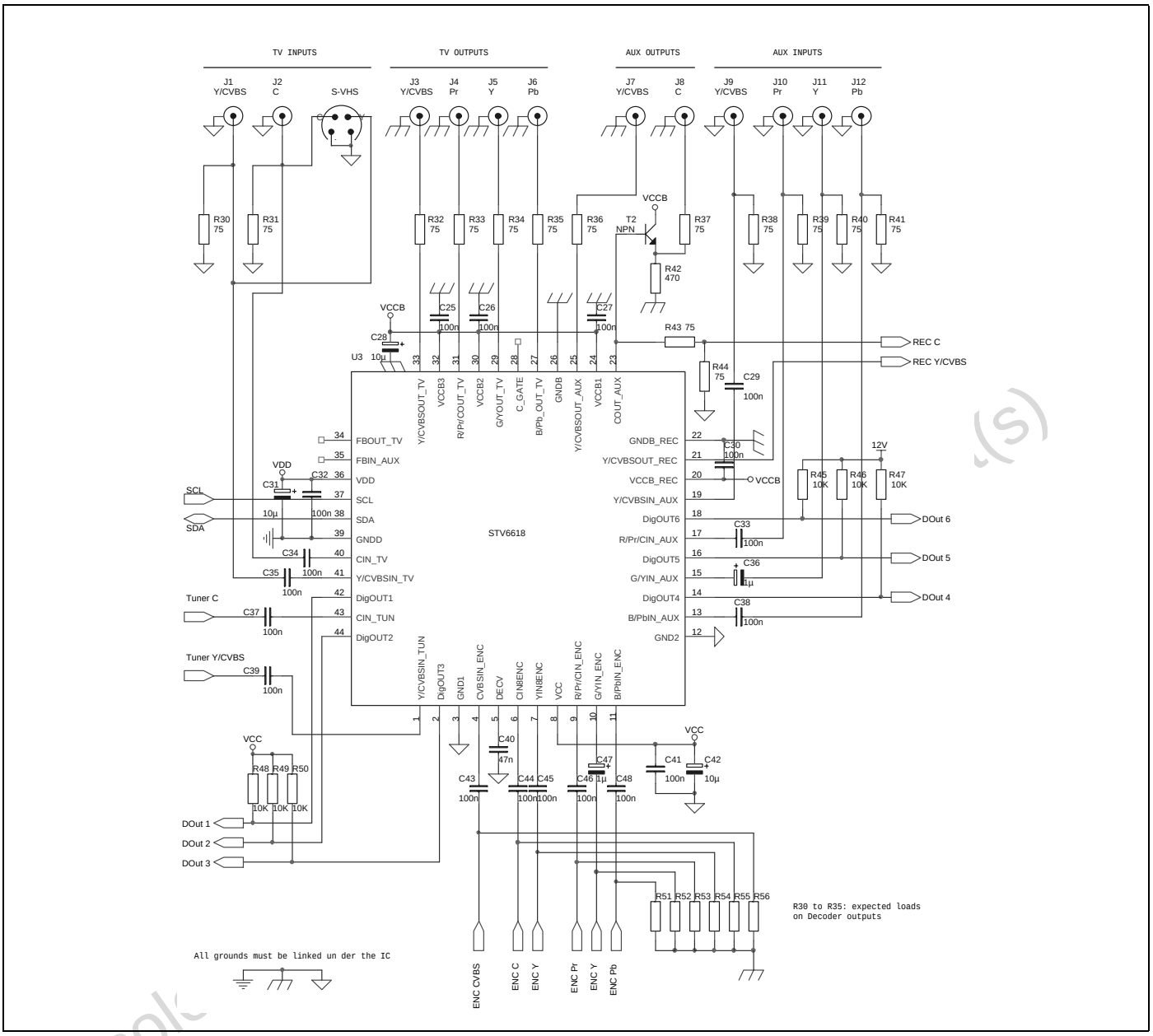
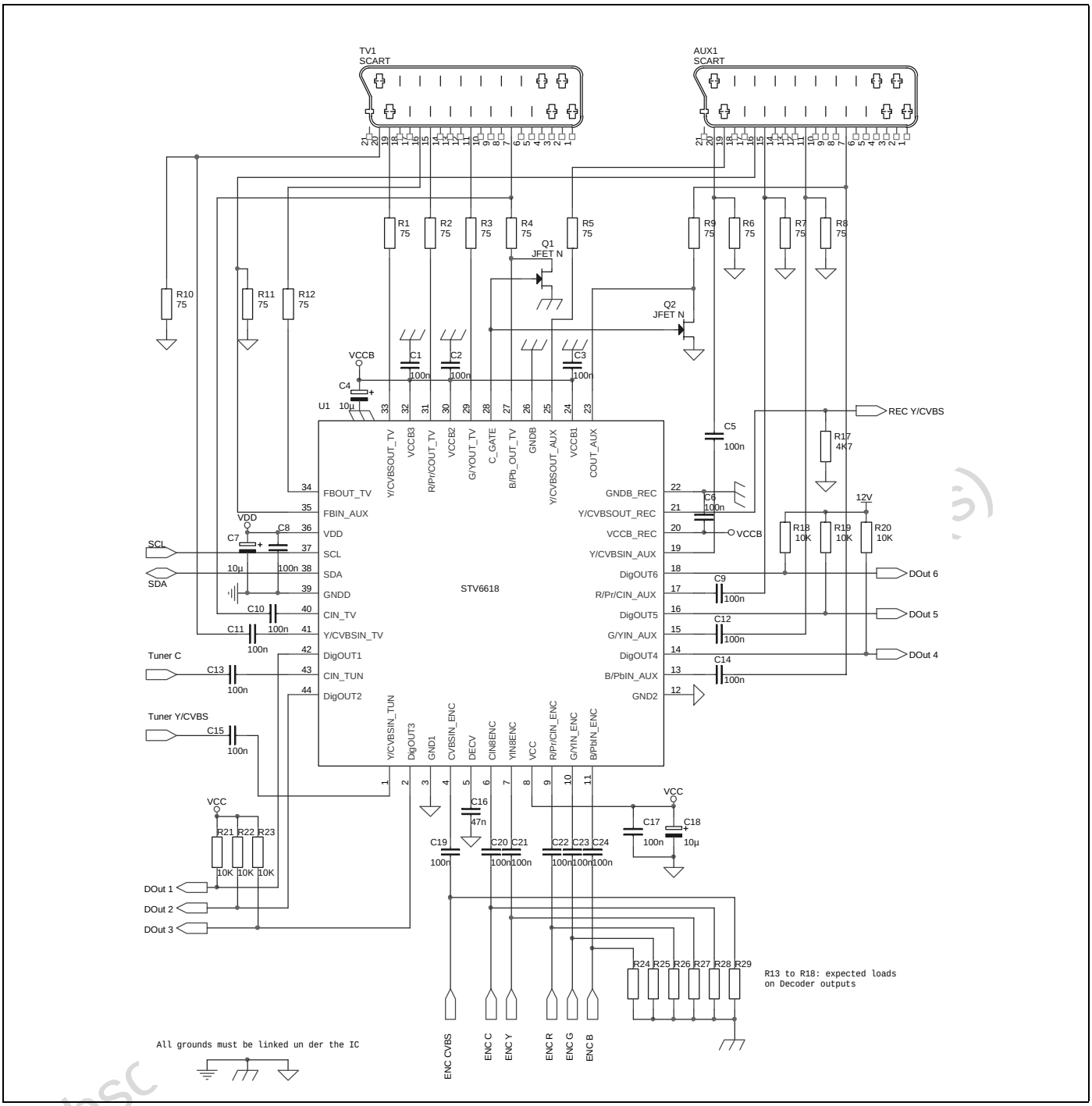
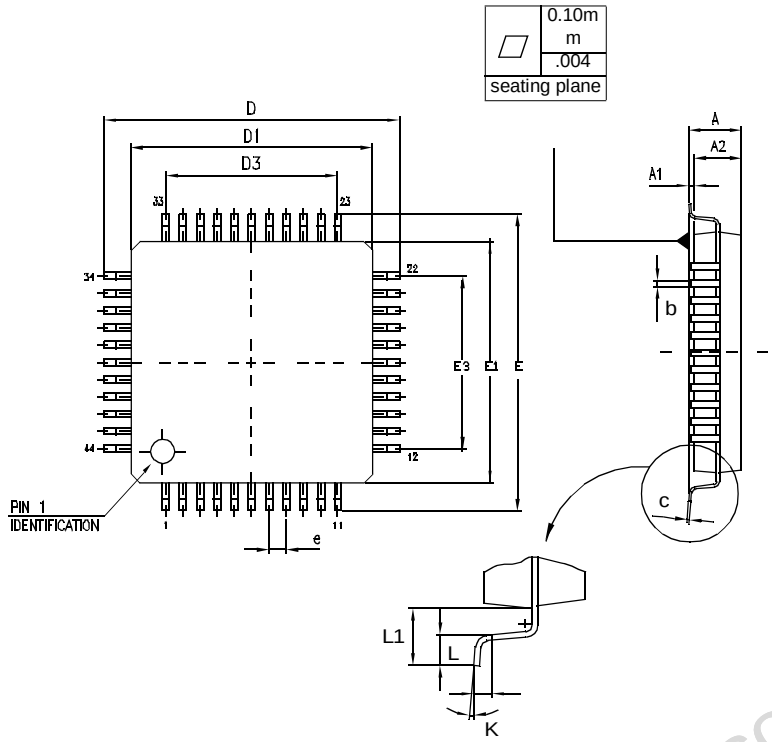


Figure 22: 2 SCART / RGB Signal Application



6 PACKAGE MECHANICAL DATA

Figure 23: 44-Pin Thin Quad Flat Package



A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.012	0.015	0.018
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
e		0.80			0.031	
K	0°	3.5°	7°			
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	44					

7 REVISION HISTORY

The following table summarizes the modifications applied to this document.

Revision	Description	Date
1.0	First Issue	24 April 2001
	New pinout proposal, to improve connection to TV SCART. Slight correction of electrical parameters (changed value in Bold). Correction of DigOUT1-2-3 I²C control specification (changed value in bold)	27 April 2001
	New pinout proposal, To improve connection to SCARTs. Application layout hypothesis: 1 layer PCB, IC on lower side (copper side), SCART on upper side	7 May 2001
	Application diagrams added. VDCin chroma section: 3.0V instead of 2.3V previously. VDCin , video section, PrPb: 3.0V instead of 2.3V previously	11 May 2001
	Add Fast Blanking Section Electrical Characteristics. Update Application Schematic Diagrams	7 June 2001
1.1	Addition of Section 4: INPUT/OUTPUT GROUPS on page 16.	21 June 2001
1.2	Document reformatted. Replaced Figure 22: 2 SCART / RGB Signal Application on page 21.	6 July 2001
1.3	CIN = 1 VPP changed to "VIN = 1 VPP in CBW Parameter in Section 2.6. Symbols for a PNP, NPN and current source as well as their connections added to Figure 17.	2 Oct 2001
1.4	Update of Crosstalk and DC Output voltage data in Section 2.4 and Section 2.6. Modification of Register 2 data in Section 3.1. Replaced Figure 21 and Figure 22.	10 Oct 2001
1.5	Update of Crosstalk data and Output Voltage values in Section 2.4 and Section 2.6. Updated Figure 3 and Figure 22.	26 Oct 2001
1.6	Chroma Output Gain (G6C) parameters updated in Section 2.6.	14 Jan 2002
1.7	Addition of minimum/maximum values for certain parameters in Section 2: ELECTRICAL CHARACTERISTICS. Document upgraded to Datasheet status.	24 May 2002
1.8	Modification of Bandwidth parameter (17 MHz) and Figure 3.	24 Sept. 2002