ISL54405

CD/MP3 Quality Stereo 2:1 Multiplexer with Click and Pop Elimination

FN6699
Rev 2.00
May 6, 2014

The Intersil ISL54405 is a single supply, bidirectional, dual single-pole/double-throw (SPDT) ultra low distortion, high OFF-Isolation analog switch that can pass analog signals that are positive and negative with respect to ground. It is primarily targeted at consumer and professional audio switching applications such as computer sound cards and home theater products. The inputs can accommodate ground referenced signals up to $2V_{RMS}$ while operating from a single 3.3V or 5V DC supply. The digital logic inputs are 1.8V logic-compatible when using a single 3.3V or 5V supply. It can be used in both AC or DC coupled ground referenced applications.

The ISL54405 features a soft-switch feature and click/pop circuitry at each signal pin that eliminates clicks and pops associated with power-up/down conditions of the preceding amplifier outputs.

With -106dB THD+N performance with a $2V_{RMS}$ signal into 20kΩ load, superior signal muting, high PSRR and very flat frequency response, the ISL54405 meets the exacting requirements of consumer and professional audio engineers.

The ISL54405 is available in 16 Ld TSSOP, 16 Ld 3mmx3mm TQFN, and 16 Ld 2.6mmx1.8mm µTQFN packages. It's specified for operation over the -40°C to +85°C temperature range.

Related Literature

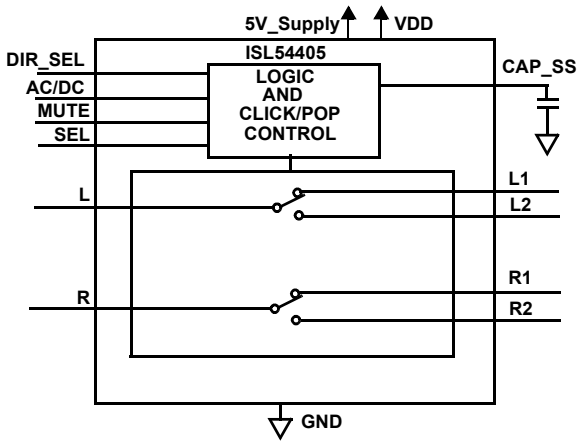
- TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- AN557 "Recommended Test Procedures for Analog Switches"

Features

- Clickless audio switching
- 2 switches
- Switch type SPDT or 2 to 1 MUX
- $2V_{RMS}$ signal switching from 3.3V or 5V supply
- -106dB THD+N into 20kΩ load at $2V_{RMS}$
- -108dB THD+N into 32Ω load at 3.9mW
- Signal to noise . . . . . >124dBV
- ±0.01dB insertion loss at 1kHz, 20kΩ load
- ±0.007dB gain variation 20Hz to 20kHz
- 125dB signal muting into 20kΩ load
- 90dB PSRR 20Hz to 20kHz
- Single supply operation . . . . . 3.3V or 5V
- Available in 16 Ld TSSOP, 16 Ld TQFN, and 16 Ld µTQFN
- Pb-Free (RoHS compliant)

Applications

- Computer sound cards
- Home theater audio products
- SACD/DVD audio
- DVD player audio output switching
- Headsets for MP3/cellphone switching
- Hi-Fi audio switching application

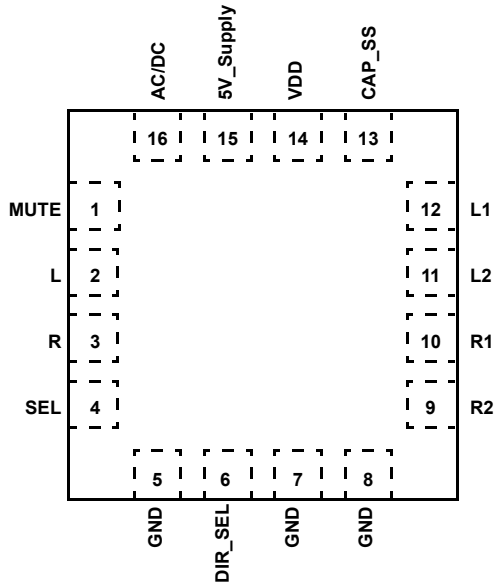


For 5V operation connect the 5V_Supply pin to 5V and float the VDD pin. For 3.3V operation connect the VDD pin to 3.3V and float the 5V_Supply pin.

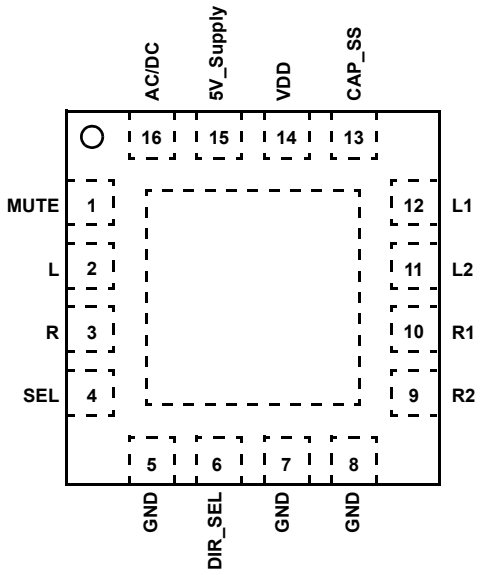
FIGURE 1. ISL54405 BLOCK DIAGRAM

Pin Configurations (Note 1)

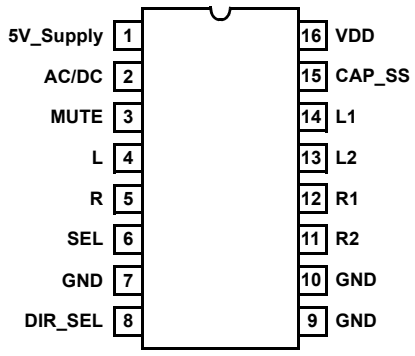
ISL54405
(16 LD µTQFN)
TOP VIEW



ISL54405
(16 LD TQFN)
TOP VIEW



ISL54405
(16 LD TSSOP)
TOP VIEW



NOTE:
1. See Figure 1 on page 1.

Truth Table

INPUTS				OUTPUTS				
AC/DC	DIR	MUTE	SEL	L1, R1	L2, R2	COM (L, R) C/P SHUNTS	L1, R1 C/P SHUNTS	L2, R2 C/P SHUNTS
0	X	0	0	ON	OFF	OFF	OFF	OFF
0	X	0	1	OFF	ON	OFF	OFF	OFF
0	X	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF	ON
1	0	0	1	OFF	ON	OFF	ON	OFF
1	0	1	X	OFF	OFF	OFF	ON	ON
1	1	0	0	ON	OFF	OFF	OFF	OFF
1	1	0	1	OFF	ON	OFF	OFF	OFF
1	1	1	X	OFF	OFF	ON	OFF	OFF

NOTE: MUTE, AC/DC, DIR: Logic “0” ≤ 0.5V, Logic “1” ≥ 1.4V or float with a 3.3V supply or 5V supply.
SEL: Logic “0” ≤0.5V, Logic “1” ≥ 1.4V with a 3.3V supply or 5V supply.
X = Don’t Care

Pin Descriptions

PIN # TSSOP	PIN # µTQFN, TQFN	PIN NAME	DESCRIPTION
16	14	VDD	System power supply pin (+3V to +3.6V) (float pin for 5V applications)
1	15	5V_Supply	5V supply pin (+4.5V to +5.5V) (float pin for 3.3V applications)
7, 9, 10	5, 7, 8	GND	Ground connection
15	13	CAP_SS	Soft-start capacitor pin
3	1	MUTE	Signal mute control pin
6	4	SEL	Input select control pin
2	16	AC/DC	AC/DC select control pin
8	6	DIR_SEL	Direction select control pin
5	3	R	Analog switch common pin
4	2	L	Analog switch common pin
11, 13	9, 11	R2, L2	Analog switch normally open pin
12, 14	10, 12	R1, L1	Analog switch normally closed pin

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54405IVZ (Notes 3, 4)	54405 IVZ	-40 to +85	16 Ld TSSOP	M16.173
ISL54405IRTZ (Notes 3, 4)	05TZ	-40 to +85	16 Ld 3x3 TQFN	L16.3x3A
ISL54405IRUZ-T (Notes 2, 5)	GAD	-40 to+ 85	16 Ld µTQFN	L16.2.6x1.8A

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

VDD to GND . . . . . -0.3V to 4.0V
5V_Supply to GND . . . . . -0.3V to 6.0V
Input Voltages
SEL, MUTE, AC/DC, DIR_SEL (Note 6) . . . . . -0.3 to ((V_{DD}) + 0.3V)
L1, L2, R1, R2 (Note 6) . . . . . -3.1 to ((V_{DD}) + 0.3V)
Output Voltages
R, L (Note 6) . . . . . -3.1 to ((V_{DD}) + 0.3V)
Continuous Current L1, L2, R1, R2 or L, R . . . . . ±300mA
Peak Current L1, L2, R1, R2 or L, R
(Pulsed 1ms, 10% Duty Cycle, Max). . . . . ±500mA
ESD Rating:
Human Body Model . . . . . >5kV
Machine Model . . . . . >200V
Charged Device Model . . . . . >2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TSSOP Package (Note 7)	110	41
16 Ld TQFN Package (Notes 8, 9)	75	11
16 Ld µTQFN Package (Note 8)	93	N/A

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on L1, L2, R1, R2, MUTE, SEL, AC/DC, DIR_SEL, R, and L exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
9. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

3.3V Supply: V_{DD} = +3.0V to +3.6V, GND = 0V, V_{DIR_SEL} = VAC/DC = GND, V_{5V_SUPPLY} = Float, V_{SIGNAL} = $2V_{RMS}$, R_{LOAD} = 20kΩ , f = 1kHz, V_{SELH} = V_{MUTEH} = 1.4V, V_{SELL} = V_{MUTEL} = 0.5V, CAP_SS = 0.1µF, (Note 10), Unless otherwise specified.

PARAMETER	TEST CONDITIONS	SUPPLY (V)	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS							
Analog Signal Range, V_{ANALOG}		3.3, 5	Full	-	2	-	V_{RMS}
ON-Resistance, r_{ON}	V_{DD} = 3.3V, I_R or I_L = 80mA, V_{Lx} or V_{Rx} = -2.828V to +2.828V (See Figure 5)	3.3	25	-	1.9	-	Ω
			Full	-	2.6	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3V, I_R or I_L = 80mA, V_{Lx} or V_{Rx} = Voltage at max r_{ON} over -2.828V to +2.828V (Note 15)	3.3	25	-	0.023	-	Ω
			Full	-	0.045	-	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.3V, I_R or I_L = 80mA, V_{Lx} or V_{Rx} = -2.828V, 0V, +2.828V (Note 13)	3.3	25	-	0.003	0.01	Ω
			Full	-	0.009	-	Ω
L, R, Lx, Rx Pull-down Resistance	V_{DD} = 3.6V, V_{Lx} or V_{Rx} = -2.83V, 2.83V, V_L or V_R = -2.83V, 2.83V, $V_{AC/DC}$ = 0V, V_{MUTE} = 3.6V, measure current, calculate resistance.	3.6	25	225	300	375	kΩ
			Full	-	345	-	kΩ
DYNAMIC CHARACTERISTICS							
THD+N	V_{SIGNAL} = $2V_{RMS}$, f = 1kHz, A-weighted filter, R_{LOAD} = 20kΩ	3.3, 5	25	-	-106	-	dB
	V_{SIGNAL} = $1.9V_{RMS}$, f = 1kHz, A-weighted filter, R_{LOAD} = 20kΩ		25	-	-113	-	dB
	V_{SIGNAL} = $1.8V_{RMS}$, f = 1kHz, A-weighted filter, R_{LOAD} = 20kΩ		25	-	-116	-	dB
	V_{SIGNAL} = $0.707V_{RMS}$, f = 1kHz, A-weighted filter, R_{LOAD} = 32Ω		25	-	-100	-	dB
SNR	f = 20Hz to 20kHz, A-weighted filter, inputs grounded, R_{LOAD} = 20kΩ or 32Ω	3.3, 5	25	-	>124	-	dBV
Insertion Loss, G_{ON}	f = 1kHz, R_{LOAD} = 20kΩ	3.3	25	-	±0.01	-	dB

Electrical Specifications

3.3V Supply: V_{DD} = +3.0V to +3.6V, GND = 0V, V_{DIR_SEL} = VAC/DC = GND, V_{5V_SUPPLY} = Float, V_{SIGNAL} = $2V_{RMS}$, R_{LOAD} = 20kΩ , f = 1kHz, V_{SELH} = V_{MUTEH} = 1.4V, V_{SELL} = V_{MUTEL} = 0.5V, CAP_SS = 0.1µF, (Note 10), Unless otherwise specified.

PARAMETER	TEST CONDITIONS	SUPPLY (V)	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
Gain vs Frequency, G_f	f = 20Hz to 20kHz, R_{LOAD} = 20kΩ, reference to G_{ON} at 1kHz	3.3	25	-	±0.007	-	dB
Stereo Channel Imbalance L1 and R1, L2 and R2	f = 20Hz to 20kHz, R_{LOAD} = 20kΩ	3.3	25	-	±0.003	-	dB
OFF-Isolation (Muting)	f = 20Hz to 22kHz, L = R = $2V_{RMS}$, R_{LOAD} = 20kΩ, MUTE = AC/DC = 3.3V, DIR_SEL = GND, SEL = "X"	3.3, 5	25	-	120	-	dB
	f = 20Hz to 22kHz, L1, R1, L2, R2 = $2V_{RMS}$, R_{LOAD} = 20kΩ, MUTE = AC/DC = DIR_SEL = 3.3V, SEL = "X"		25	-	120	-	dB
	f = 20Hz to 22kHz, V_L or V_R = $0.7V_{RMS}$, R_{LOAD} = 32Ω		25	-	125	-	dB
Crosstalk (Channel-to-Channel)	R_L = 20kΩ, f = 20Hz to 20kHz, V_{SIGNAL} = $2V_{RMS}$, signal source impedance = 20Ω, Note 16	3.3	25	-	120	-	dB
	R_L = 32Ω, f = 20Hz to 20kHz, V_{SIGNAL} = $0.7V_{RMS}$, signal source impedance = 20Ω, Note 16		25	-	120	-	dB
PSRR	f = 1kHz, V_{SIGNAL}= $100mV_{RMS}$, inputs grounded	3.3, 5	25	-	110	-	dB
	f = 20kHz, V_{SIGNAL}= $100mV_{RMS}$, inputs grounded		25	-	90	-	dB
Bandwidth, -3dB	R_{LOAD} = 50Ω	3.3	25	-	230	-	MHz
ON to Mute Time, $T_{TRANS-OM}$	CAP_SS = 0.1µF	3.3	25	-	50	-	ns
Mute to ON Time, $T_{TRANS-MO}$	CAP_SS = 0.1µF (Selectable via soft-start capacitor value)	3.3	25	-	58	-	ms
Turn-ON Time, t_{ON}	V_{DD} = 3.3V, V_{Lx} or V_{Rx} = 1.5V, V_{MUTE} = 0V, R_L = 20kΩ (See Figure 2)	3.3	25	-	45	-	µs
Turn-OFF Time, t_{OFF}	V_{DD} = 3.3V, V_{Lx} or V_{Rx} = 1.5V, V_{MUTE} = 0V, R_L = 20kΩ (See Figure 2)	3.3	25	-	50	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 3.6V, V_{Lx} or V_{Rx} = 1.5V, V_{MUTE} = 0V, R_L = 20kΩ (See Figure 3)	3.6	25	-	45	-	µs
OFF-Isolation	R_L = 50Ω, f = 1MHz, V_L or V_R = $1V_{RMS}$ (See Figure 4)	3.3	25	-	100	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, f = 1MHz, V_L or V_R = $1V_{RMS}$ (See Figure 6)	3.3	25	-	70	-	dB
Lx, Rx OFF Capacitance, C_{OFF}	f = 1MHz, V_{Lx} or V_{Rx} = V_L or V_R = 0V (See Figure 7)	3.3	25	-	10	-	pF
L, R ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{Lx} or V_{Rx} = V_{COM} = 0V (See Figure 7)	3.3	25	-	27	-	pF
POWER SUPPLY CHARACTERISTICS							
Power Supply Range, VDD	5V_Supply = Float	3.3	Full	3	-	3.6	V
Power Supply Range, 5V_Supply	V_{DD} = Float	5	Full	4.5	-	5.5	V
Positive Supply Current, I+	V_{DD} = +3.6V, V_{MUTE} = 0V, V_{SEL} = 0V or V_{DD}	3.6	25	-	54	65	µA
			Full	-	59	-	µA
	V_{DD} = +3.6V, V_{MUTE} = V_{DD}, V_{SEL} = 0V or V_{DD}	3.6	25	-	14	18	µA
		3.6	Full	-	15	-	µA
	V_{DD} = +3.6V, V_{MUTE} = 0V, V_{SEL} = 1.8V	3.6	25	-	55	65	µA
		3.6	Full	-	58	-	µA
DIGITAL INPUT CHARACTERISTICS							
Input Voltage Low, V_{SELL}, V_{MUTEL}		3.3, 5	Full	-	-	0.5	V

Electrical Specifications

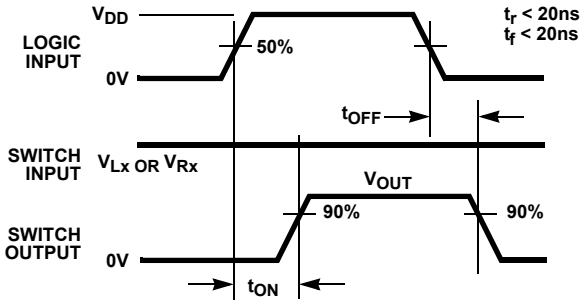
3.3V Supply: V_{DD} = +3.0V to +3.6V, GND = 0V, V_{DIR_SEL} = VAC/DC = GND, V_{5V_SUPPLY} = Float, V_{SIGNAL} = $2V_{RMS}$, R_{LOAD} = 20kΩ , f = 1kHz, V_{SELH} = V_{MUTEH} = 1.4V, V_{SELL} = V_{MUTEL} = 0.5V, CAP_SS = 0.1µF, (Note 10), Unless otherwise specified.

PARAMETER	TEST CONDITIONS	SUPPLY (V)	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
Input Voltage High, V_{SELH}, V_{MUTEH}		3.3, 5	Full	1.4	-	-	V
Input Current, I_{SELH}, I_{SELL}	V_{DD} = 3.6V, V_{MUTE} = 0V, V_{SEL} = 0V or V_{DD}	3.6	Full	-0.5	0.01	0.5	µA
Input Current, $I_{AC/DCL}$, I_{DIR_SELL}	V_{DD} = 3.6V, $V_{AC/DC}$, V_{DIR_SEL} = 0V, V_{MUTE} = Float, V_{SEL} = V_{DD}	3.6	Full	-1.3	-0.7	0.3	µA
Input Current, $I_{AC/DCH}$, I_{DIR_SELH}	V_{DD} = 3.6V, $V_{AC/DC}$, V_{DIR_SEL} = V_{DD}, V_{MUTE} = 0V, V_{SEL} = 0V	3.6	Full	-0.5	0.01	0.5	µA
Input Current, I_{MUTEL}	V_{DD} = 3.6V, V_{SEL} = V_{DD}, V_{MUTE} = 0V	3.6	Full	-1.3	-0.7	0.3	µA
Input Current, I_{MUTEH}	V_{DD} = 3.6V, V_{SEL} = 0V, V_{MUTE} = V_{DD}	3.6	Full	-0.5	0.01	0.5	µA

NOTES:

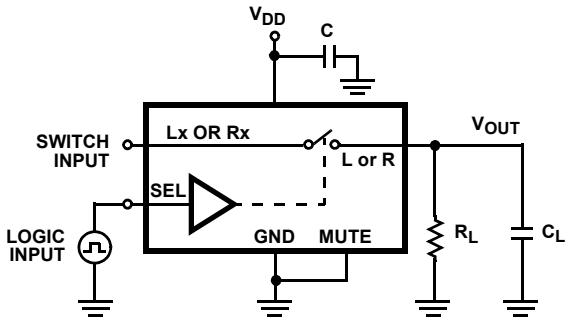
10. V_{IN} = input voltage to perform proper function.
11. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
12. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
13. Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.
14. Limits established by characterization and are not production tested.
15. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
16. Crosstalk is inversely proportional to source impedance.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(Lx\ or\ Rx)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 2B. TEST CIRCUIT

FIGURE 2. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

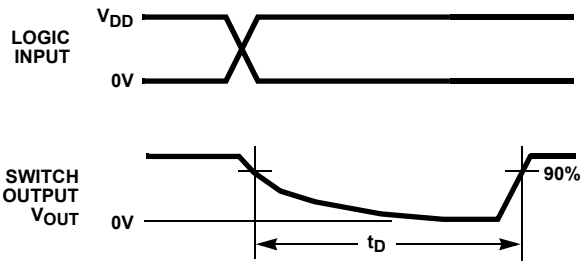
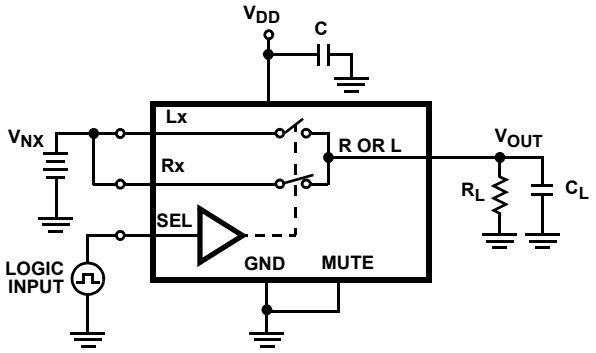


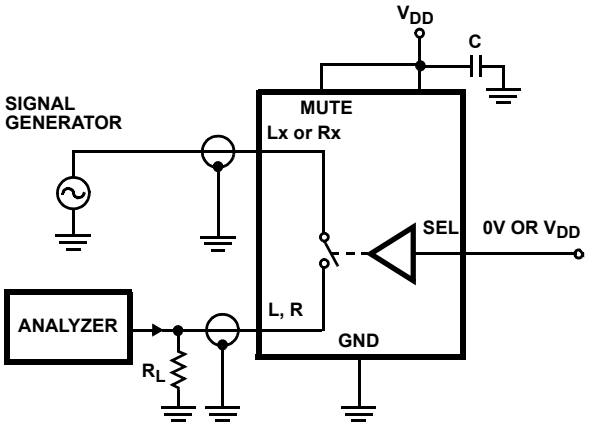
FIGURE 3A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

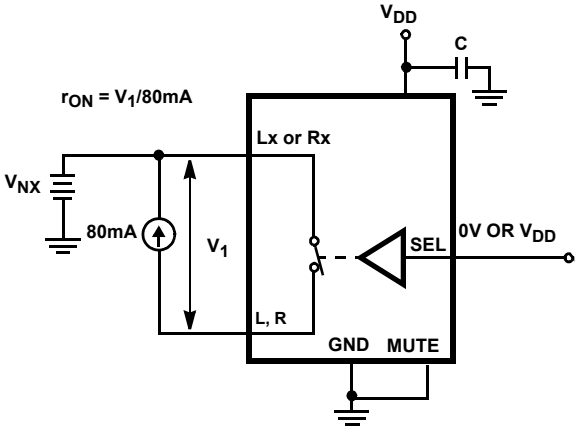
FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME



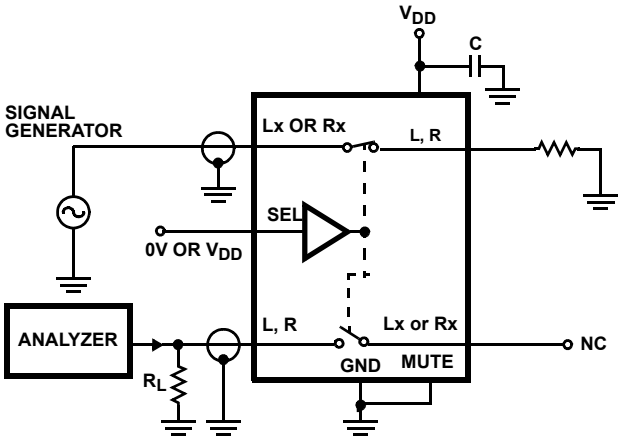
Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 4. OFF-ISOLATION TEST CIRCUIT



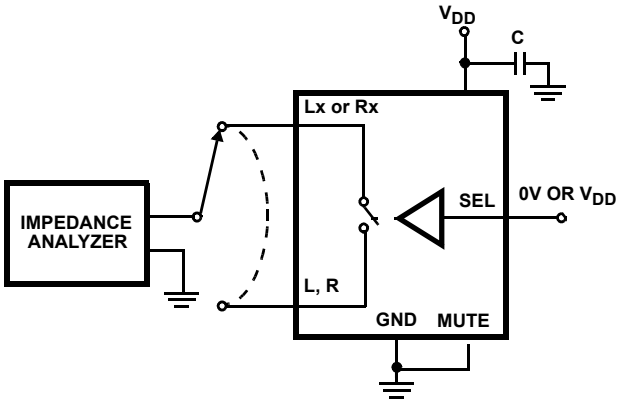
Repeat test for all switches.

FIGURE 5. r_{ON} TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

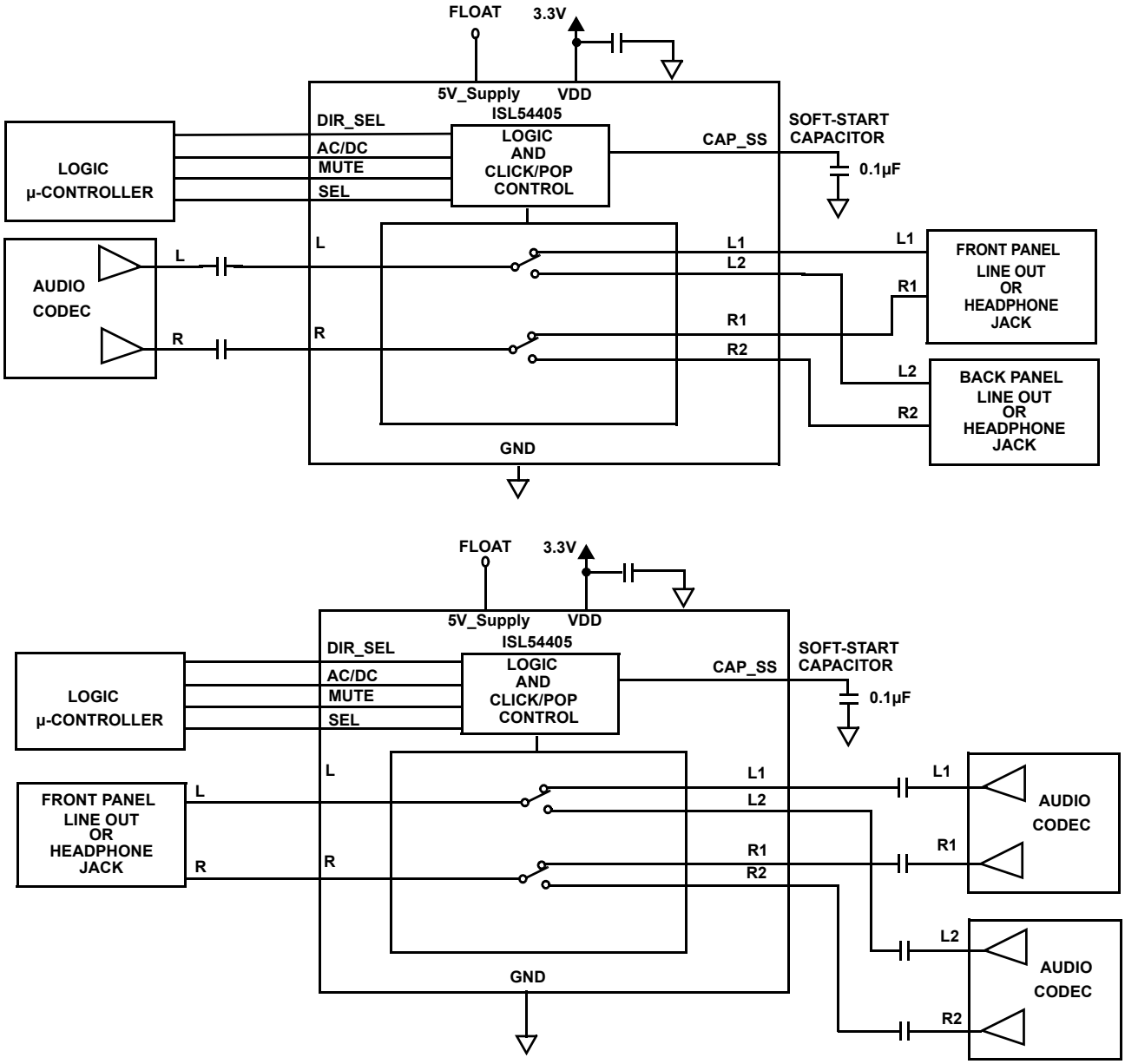
FIGURE 6. CROSSTALK TEST CIRCUIT



Repeat test for all switches.

FIGURE 7. CAPACITANCE TEST CIRCUIT

Sound Card AC Coupled Application Block Diagrams



Detailed Description

The ISL54405 is a single supply, bidirectional, dual single pole/double throw (SPDT) ultra low distortion, high OFF-Isolation analog switch. It was designed to operate from either a 3.3V or 5V single supply. When operated with a 3.3V or 5V single supply, the switches can accommodate $\pm 2.83V_{PEAK}$ ($2V_{RMS}$) ground reference analog signals. The switch r_{ON} flatness across this range is extremely small resulting in excellent THD+N performance (0.0006% with 20kΩ load and 0.0014% with 32Ω load at $707mV_{RMS}$). The T-Type configuration of the switch cells prevents signals from getting through to the output when a switch is in the OFF-state providing for superior mute performance (>120dB) in audio applications.

The ISL54405 has special circuitry to eliminate click and pops in the speakers during power-up and power-down of the audio CODEC drivers, during removal and insertion of headphones, and while switching between sources and loads.

The ISL54405 was designed primarily for consumer and professional audio switching applications such as computer sound cards and home theater products. The "Sound Card AC Coupled Application Block Diagrams" show two typical sound card applications. In the upper block diagram the ISL54405 is being used to route a single stereo source to either the front or back panel line outs of the computer sound card. In the lower block diagram the ISL54405 is being used to multiplex two stereo sources to a single line out of the computer sound card.

SPDT Switch Cell Architecture and Performance Characteristics

The normally open (L_2, R_2) and normally closed (L_1, R_1) of the SPDT switches are T-Type switches that have a typical r_{ON} of 1.9Ω and an off-isolation of >120dB. The low on-resistance (1.9Ω) and r_{ON} flatness (0.003Ω) provide very low insertion loss and minimal distortion to applications that require hi-fidelity signal reproduction.

The SPDT switch cells have internal charge pumps that allow for signals to swing below ground. They were specifically designed to pass audio signals that are ground referenced and have a swing of ± $2.828V_{PEAK}$ while driving either 10k/20kΩ (receiver) or 32Ω (headphone) loads.

Each switch cell incorporates special circuitry to gradually decrease the switch resistance when transitioning from the OFF-state (high impedance) to the ON-state (1.9Ω). The gradual decrease in the switch resistance provides for a slow ramp of the voltage at the load side of the switch which helps to eliminate clicks and pops in the speaker by suppressing the transient during switching events. The output voltage ramp time is determined by the capacitor value of the soft-start capacitor connected at the CAP_SS pin. With a 0.1µF ceramic chip capacitor the ramp time is approximately 4.6V/s. The slow ramping of the signal at the output can be disabled by floating the CAP_SS pin.

In addition to the slow ramp feature (soft-start feature) of the in line switches, the part has special click and pop (C/P) shunt circuitry at each of the signal pins (L, R, L_1, L_2, R_1, and R_2). A pin's C/P shunt circuitry is activated or deactivated depending on the logic levels applied at the AC/DC and DIR_SEL control pins. This shunt circuitry serves two functions:

1. In an AC coupled application they are activated and directed to the source side of the switch to suppress or eliminate click/pop noise in the speaker load when powering up or down of the audio CODEC drivers.
2. For superior muting the C/P shunt circuitry is activated and directed to the load side of the switch which gives >120dB of OFF-Isolation when driving a 10k/20kΩ receiver load with an audio signal in the range of 20Hz to 22kHz.

If the AC/DC pin is driven LOW, all C/P shunt circuitry at all the signal pins (L, R, L1, R1, L2, and R2) are deactivated and not operable.

If the AC/DC pin is driven HIGH, then the logic at the DIR_SEL pin will determine whether the L and R (COM) C/P shunt circuitry is activated or the L1, L2, R1, and R2 (NOx, NCx) C/P shunt circuitry is activated. When the DIR_SEL is driven LOW, the L1, R1, L2, R2 C/P shunt circuitry will be activated while the L and R C/P shunt circuitry will be deactivated. When the DIR_SEL is driven HIGH, the L and R C/P shunt circuitry will be activated while the L1, R1, L2, R2 C/P shunt circuitry will be deactivated. Note: Shunt circuitry that is activated will be turned ON when a switch cell is turned OFF and will be OFF when a switch cell is turned ON.

MUTE TO ON

When the MUTE pin is driven LOW, the ISL54405 will transition to the ON-state in the following sequence:

Supply Voltage, Signal Amplitude, and Grounding

The power supply connected at VDD or the 5V_Supply pin provides power to the ISL54405 part. The ISL54405 is a single supply device that was designed to be operated with a 3.3V ±10% DC supply connected at the VDD pin or a 5V ±10% DC supply connected at the 5V_Supply pin.

It was specifically designed to accept ground referenced $2V_{RMS}$ (± $2.828V_{PEAK}$) audio signals at its signal pins while driving either 10k/20kΩ receiver loads or 32Ω headphone loads.

When using the part in a 3.3V application the 5V_Supply pin should be left floating. A 0.1µF decoupling capacitor should be connected from the VDD pin to ground to minimize power supply noise and transients. This capacitor should be located as close to the pin as possible.

The part also has a 5V supply pin (5V_Supply) to allow it to be used in 5V ±10% applications. Special circuitry within the device converts the 5V, connected at the 5V_Supply pin, too 3.3V to properly power the internal circuitry of the device.

When using the part in a 5V application the VDD pin should be left floating. A 0.1µF decoupling capacitor should be connected from the 5V_Supply pin to ground to minimize power supply noise. This capacitor should be located as close to the pin as possible.

Grounding of the ISL54405 should follow a star configuration (see Figure 8). All grounds of the IC should be directly connected to the power supply ground return without cascading to other grounds. This configuration isolates shunt currents of the Click and Pop transients from the IC ground and optimizes device performance.

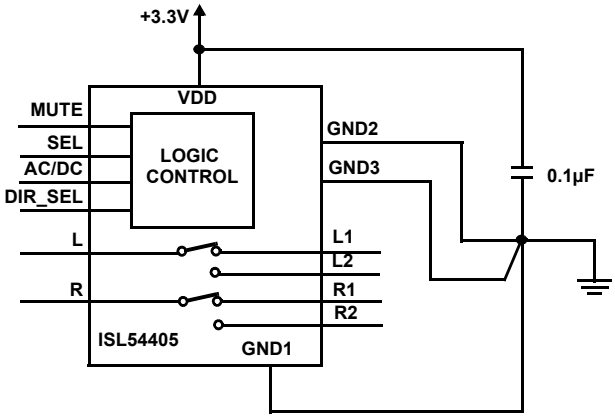


FIGURE 8. STAR GROUNDING CONFIGURATION

Mute Operation

When the MUTE logic pin is driven HIGH the part will go into the mute state. In the mute state all switches of the SPDTs are open while the T-Shunt switches are closed. In addition any activated click and pop shunt circuitry at the signal pins is turned on. See "Logic Control" on page 10 for more details.

1. All active shunt switches turn off quickly.
2. The resistance of the switches selected by the SEL pin will gradually decrease in resistance. They will decrease from their high OFF-resistance to their ON-resistance of 1.9Ω. This gradual decrease in resistance will allow for the voltage at the load to increase gradually. The voltage ramp rate at the load is determined by the value of the capacitor connected at the CAP_SS pin, see Figures 28 and 29 on page 16.

Table 1 indicates how the signal ramp rate at the load changes as you change the CAP_SS capacitor value. It also shows how the mute turn-on time is affected.

TABLE 1. SIGNAL RAMP-RATE LOAD CHANGE WITH CAP SS

CAPACITOR VALUE	RAMP RATE	TURN-ON TIME
No Capacitor	6250V/s	65µs
0.05µF	10.3V/s	30ms
0.1µF	4.6V/s	58ms

ON TO MUTE

When the MUTE pin is driven HIGH, the switches will turn off quickly (50ns) and the active shunt switches will turn on quickly. Note: There is no gradual ramping of the switch resistance in this direction.

OFF-ISOLATION IN THE MUTE STATE

When in the mute state, the level of OFF-Isolation across the audio band is dependent on the signal amplitude, external loading, and location of the activated C/P (click/pop) shunt circuitry. During muting, the logic of the ISL54405 can be configured to activate the C/P shunt circuitry on the load side of the switch or on the source side of the switch, or deactivated on both sides of the switch.

With a 0.707V_{RMS} signal driving a 32Ω headphone load, the location of the C/P shunt circuitry has little effect on the off-isolation performance (>120dB of off-isolation in all configurations), see Figure 12 on page 13.

With a 2V_{RMS} signal driving a 20kΩ amplifier load, the best OFF-Isolation is achieved by placing the C/P shunt circuitry on the load side of the switch (>120dB across the audio band). The OFF-Isolation decreases when placing the C/P shunt circuitry on the source side of the switch (>85dB across the audio band), see Figure 11 on page 13.

Note: For AC coupled applications when powering up or down of the audio drivers the C/P shunts should be activated on the source side of the switch. See "Click and Pop Operation" on page 11.

When using the switch for muting of the audio signal the C/P shunt circuitry should be deactivated on the source side of the switch and directed to the load side of the switch for best possible OFF-Isolation.

Logic Control

The ISL54405 has four logic control pins; the AC/DC, DIR_SEL, MUTE, and SEL. The MUTE and SEL control pins determine the state of the switches. The AC/DC and DIR_SEL control pins determine the location of the C/P (click/pop) shunt circuitry and if it will be active or not. See "Truth Table" on page 3.

The ISL54405 logic is 1.8V CMOS compatible (Low ≤ 0.5V and High ≥ 1.4V) over a supply range of 3.0V to 3.6V at the VDD pin or 4.5V to 5.5V at the 5V_Supply pin. This allows control via 1.8V or 3V µ-controller.

SEL, MUTE CONTROL PINS

The state of the SPDT switches of the ISL54405 device is determined by the voltage at the MUTE pin and the SEL pin.

The SEL control pin is only active when MUTE is logic "0". The MUTE has an internal pull-up resistor to the internal 3.3V supply rail and can be driven HIGH or tri-stated (floated) by the µ-processor.

These pins are 1.8V logic compatible. When powering the part by the VDD pin the logic voltage can be as high as the V_{DD} voltage which is typically 3.3V. When powering the part by the 5V_Supply pin the logic voltage can be as high as the 5V_Supply voltage which is typically 5V.

Logic Levels:
MUTE = Logic "0" (Low) when ≤0.5V
MUTE = Logic "1" (High) when ≥1.4V or floating
SEL = Logic "0" (Low) when ≤ 0.5V
SEL = Logic "1" (High) when ≥1.4V

AC/DC AND DIR_SEL CONTROL PINS

The ISL54405 contains C/P (click/pop) shunt circuitry on its COM pins (L, R) and on its signal pins (L1, R1, L2, R2). The activation of this circuitry and whether it is located on the COM or signal side of the switch is determined by the logic levels applied at the AC/DC and DIR_SEL pins. The DIR_SEL control pin is only active when AC/DC is logic "1". Note: Any activated C/P shunt circuitry is ON when in the mute state (MUTE = Logic "1") and OFF in the audio state (MUTE = Logic "0").

When AC/DC is logic "0", all of the C/P shunt circuitry on both sides of the switch is deactivated and not operable.

When AC/DC is logic "1" then the DIR_SEL logic level determines whether the shunt circuitry will be activated on the COM side of the switch or on the signal side of the switch. When DIR_SEL = Logic "1" the C/P shunts on the COM side (L,R) are activated and inoperable on the signal side (L1, R1, L2, R2) of the switch. When DIR_SEL = Logic "0" the C/P shunts are activated on the signal side (L1, R1, L2, R2) and inoperable on the COM side (L, R).

Logic Levels:
AC/DC, DIR_SEL = Logic "0" (Low) when ≤0.5V
AC/DC, DIR_SEL = Logic "1" (High) when ≥1.4V or Floating.

The AC/DC and DIR_SEL have internal pull-up resistors to the internal 3.3V supply rail and can be driven HIGH or tri-stated (floated by the µ-processor). They should be driven to ground for a logic "0" (Low). Note: For 5V applications, the AC/DC and DIR_SEL pins should never be driven to the external 5V rail. They need to be driven with 1.8V logic or 3V logic circuit.

AC Coupled or DC Coupled Operation

The Audio CODEC drivers can be directly coupled to the ISL54405 when the audio signals from the drivers are ground referenced or do not have a significant DC offset voltage, <50mV. Otherwise, the signal should be AC coupled to the ISL54405 part.

CLICK AND POP OPERATION

The ISL54405 has special circuitry to eliminate click and pops in the speakers during power-up and power-down of the Audio CODEC Drivers and during removal and insertion of headphones.

A different click and pop scheme is required depending on whether the audio CODEC drivers are AC coupled or DC coupled to the inputs of the ISL54405 part.

AC COUPLED CLICK AND POP OPERATION

Single supply audio drivers have their signal biased at a DC offset voltage, usually at 1/2 the DC supply voltage of the driver. As this DC bias voltage comes up or goes down during power up or down of the driver a transient can be coupled into the speaker load through the DC blocking capacitor (see the "Sound Card AC Coupled Application Block Diagrams" on page 8).

When a driver is off and suddenly turned on, the rapidly changing DC bias voltage at the output of the driver will cause an equal voltage at the input side of the switch due to the fact that the voltage across the blocking capacitor cannot change instantly. If the switch is in audio mode or there is no low impedance path to discharge the capacitor voltage at the input of the switch, before turning on the switch, a transient discharge will occur in the speaker, generating a click and pop noise.

Proper elimination of a click/pop transient at the speaker load while powering up or down of the audio driver requires that the ISL54405 have its C/P shunts activated on the source side of the switch and then placed in mute mode. This allows the transient generated by the audio drivers to be discharged through the click and pop shunt circuitry.

Once the driver DC bias has reached VDD/2 and the transient on the switch side of the DC blocking capacitor has been discharged to ground through the C/P shunt circuitry, the switches can be turned on and connected through to the speaker loads without generating an undesirable click/pop in the speakers.

With a typical DC blocking capacitor of 220µF and the C/P shunt circuitry designed to have a resistance of 40Ω, allowing a 100ms wait time to discharge the transient before placing the switch in the audio mode will prevent the transient from getting through to the speaker load. See Figures 26 and 27 on page 15.

CLICK AND POP ELIMINATION WHEN CONNECTED TO HIGH IMPEDANCE SOURCE AND LOAD

By design, in order to flatten the RON resistance of the switch across the signal range (±3V) a current gets added to the signal path. When the ISL54405 part is connected to a high impedance source (i.e. AC coupled to the input of the switch) and a high impedance load, (such as the impedance of a 20kΩ to 100kΩ preamplifier stage) a DC offset voltage will be present on the signal line in the range of 35mV to 135mV.

When the switch is turned off, this offset voltage gets pulled to ground. During switching, this change in the offset voltage can cause a click and pop noise to be heard in the downstream speaker.

Placing a 1kΩ resistor from the output of the switch to ground will lower the offset voltage to around 1.5mV, thereby effectively eliminating the click and pop noise. The 1kΩ resistor is small enough to reduce the voltage offset significantly while not increasing power dissipation dramatically. Power consumption will need to be considered when using a smaller impedance under this scenario.

When connected to a low impedance load such as headphones (32Ω), the current added to the signal line results in a minimal DC offset voltage on the signal line and does not cause click and pop noise when the switch is turned off.

DC COUPLED CLICK AND POP OPERATION

The ISL54405 can pass ground referenced audio signals which allows it to be directly connected to audio drivers that output ground referenced audio signals, eliminating the need for a DC blocking capacitor.

Audio drivers that swing around ground, however, do generate some DC offset, from a few millivolts to tens of millivolts. When switching between audio channels or muting the audio signal, these small DC offset levels of the drivers can generate a transient that can cause unwanted clicks and pops in the speaker loads.

In a DC coupled application the C/P shunt resistors placed at the source side of the switch have no effect in eliminating the transients at the speaker loads when transitioning in and out of the mute state or switching between channels. In fact, having these C/P shunts active on the source side unnecessarily increases the power consumption. So, for DC coupled connection, the C/P shunt circuitry should not be applied at the source (driver) side of the switch.

For DC coupled applications the ISL54405 has a special soft-start feature that slowly ramps the DC offset voltage from the audio driver to the speaker load when turning on a switch channel. The ramp rate at the load is determined by the capacitor value connected at the CAP_SS pin.

Lab experimentation has shown that if you can slow the voltage ramp rate at the speaker to <10V/s, you can eliminate click/pop noise in a speaker. A soft-start capacitor value of 0.1µF provides for 4.5V/s ramp rate and is recommended. See Figures 28 and 29 on page 16. See "MUTE to ON" on page 9 for more detail of how soft-start works.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes or diode stacks from the pin to V_{DD} and to GND (see Figure 9). To prevent forward biasing these diodes,

V_{DD} must be applied before any input signals, and the signal voltages must remain between V_{DD} and -3V and the logic voltage must remain between V_{DD} and ground.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin goes below ground by more than -3V or above the V_{DD} rail and the logic pin goes below ground or above the V_{DD} rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 9). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting Schottky diodes to the signal pins, as shown in Figure 9 will shunt the fault current to the supply or to ground thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current and to clamp when the voltage reaches the overvoltage limit.

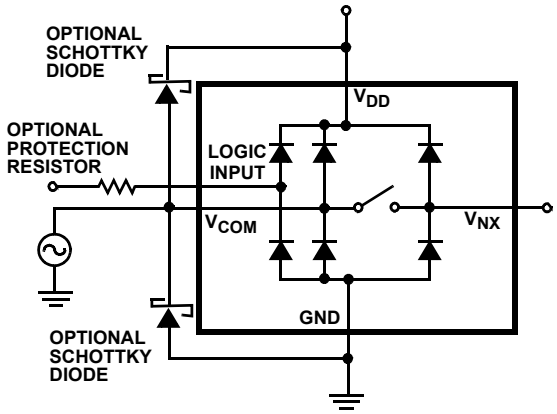


FIGURE 9. OVERVOLTAGE PROTECTION

High-Frequency Performance

In 50Ω systems, the ISL54405 has a -3dB bandwidth of 230MHz (see Figure 30). The frequency response is very consistent over varying analog signal levels.

An OFF-switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed-through from a switch's input to its output. OFF-Isolation is the resistance to this feed-through, while crosstalk indicates the amount of feed-through from one switch to another. Figure 31 details the high OFF-Isolation and crosstalk rejection provided by this part. At 1MHz, Off-Isolation is about 100dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease OFF-Isolation and crosstalk rejection due to the voltage divider action of the switch off impedance and the load impedance.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

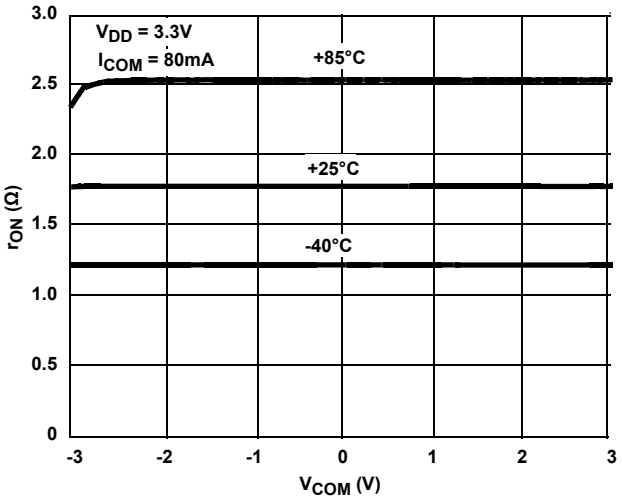


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

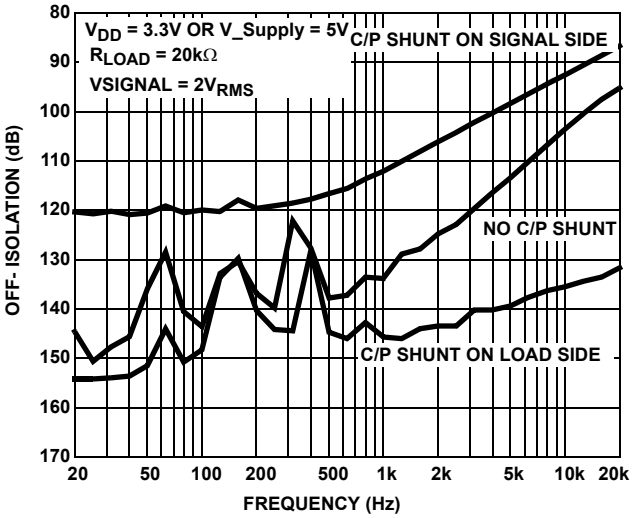


FIGURE 11. OFF-ISOLATION, $2V_{RMS}$ SIGNAL, 20kΩ LOAD

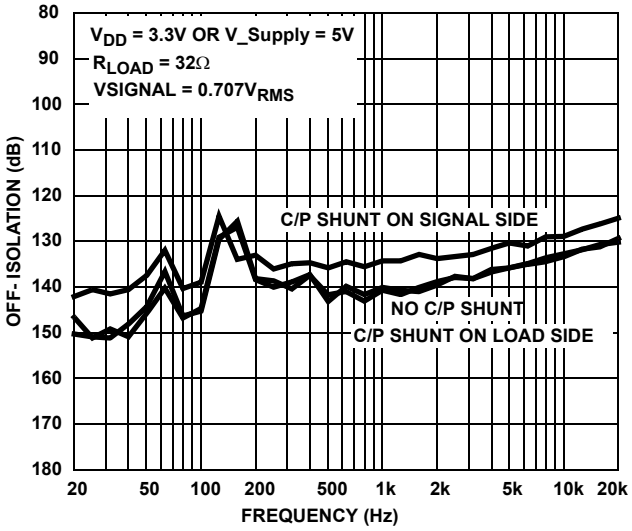


FIGURE 12. OFF-ISOLATION, $0.707V_{RMS}$ SIGNAL, 32Ω LOAD

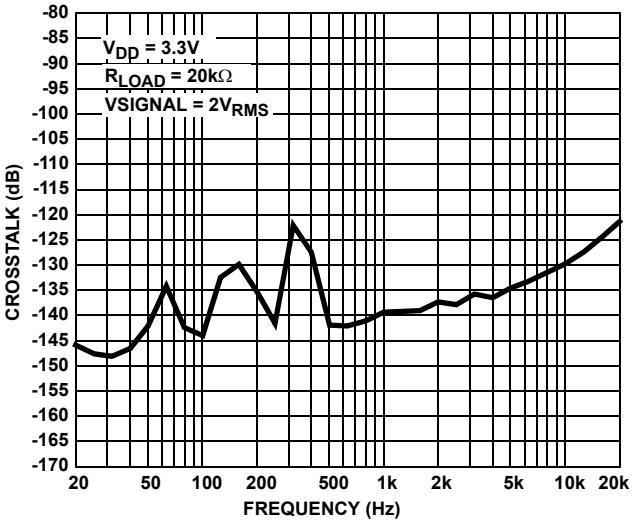


FIGURE 13. CHANNEL-TO-CHANNEL CROSSTALK

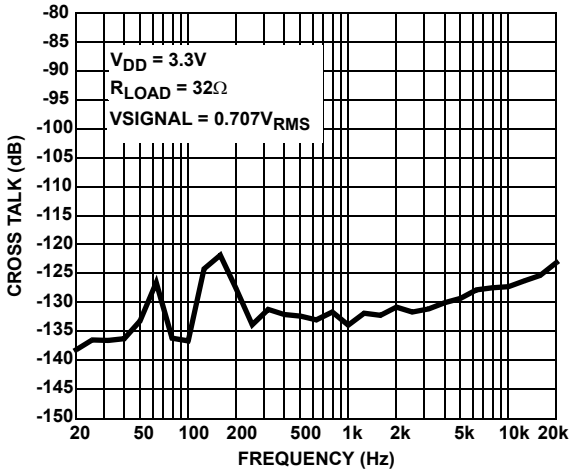


FIGURE 14. CHANNEL-TO-CHANNEL CROSSTALK

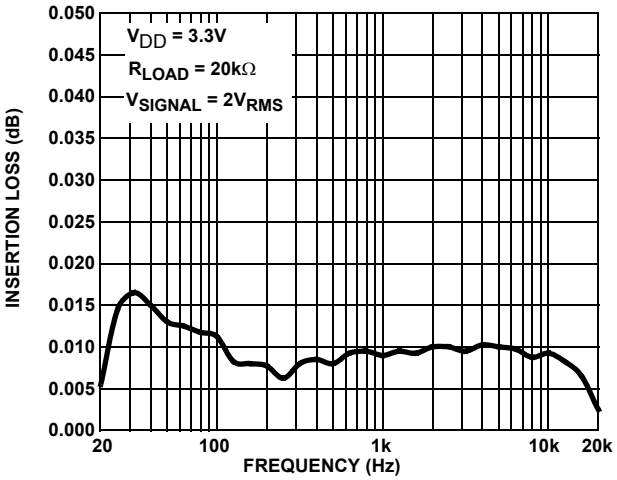


FIGURE 15. INSERTION LOSS vs FREQUENCY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified (Continued)

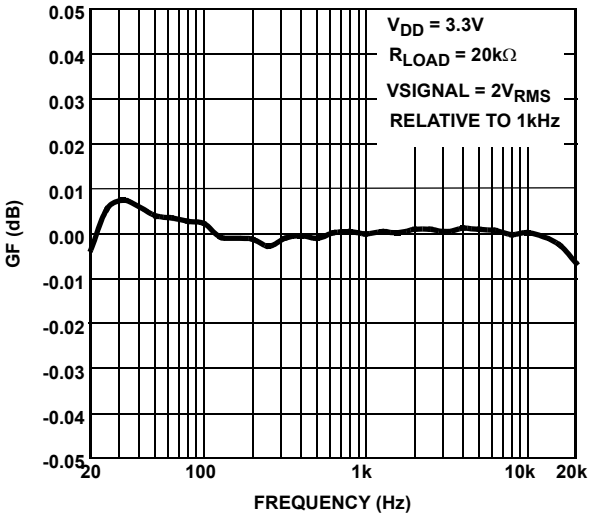


FIGURE 16. GAIN vs FREQUENCY

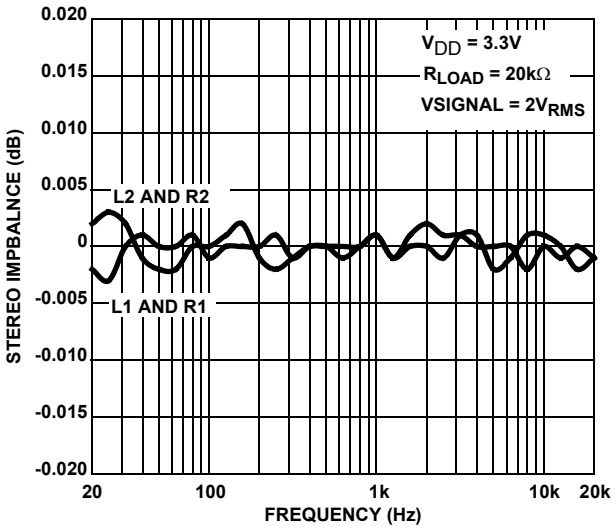


FIGURE 17. STEREO IMBALANCE vs FREQUENCY

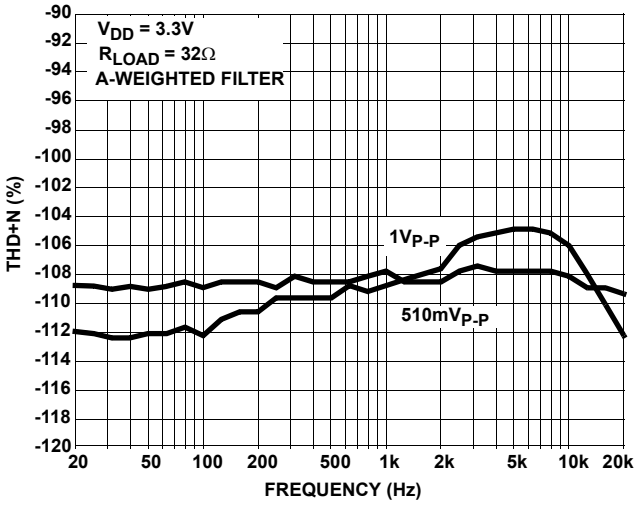


FIGURE 18. THD+N vs SIGNAL LEVELS vs FREQUENCY

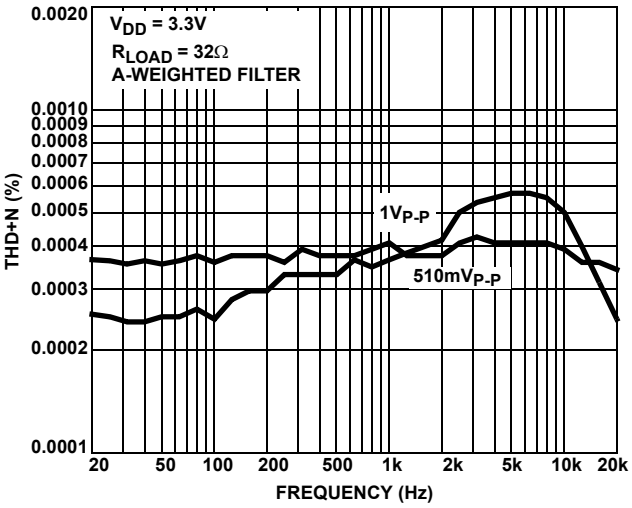


FIGURE 19. THD+N vs SIGNAL LEVELS vs FREQUENCY

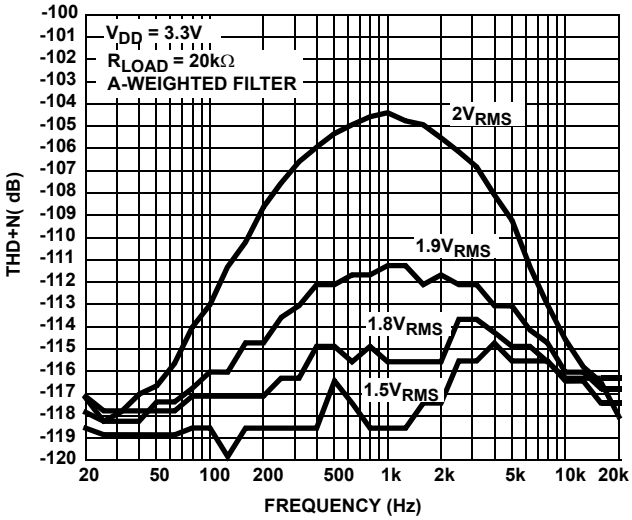


FIGURE 20. THD+N vs SIGNAL LEVELS vs FREQUENCY

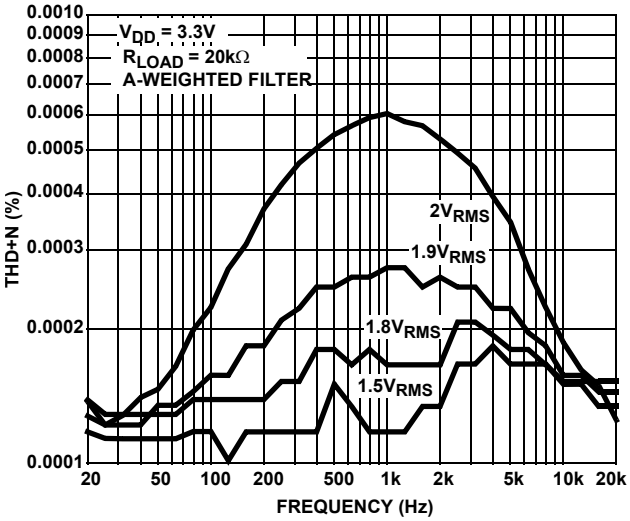


FIGURE 21. THD+N vs SIGNAL LEVELS vs FREQUENCY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified (Continued)

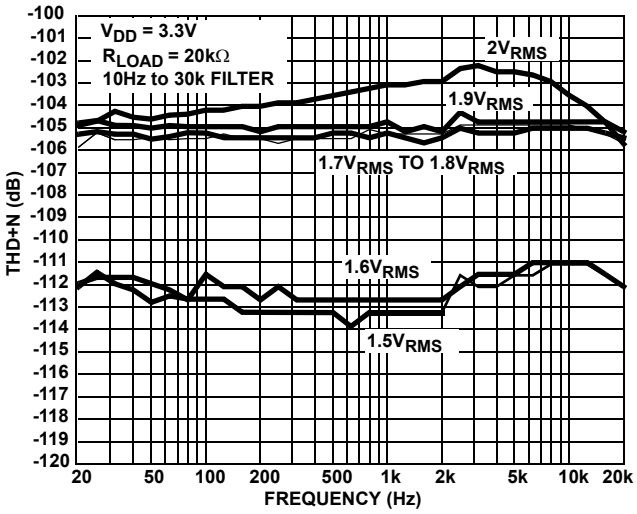


FIGURE 22. THD+N vs SIGNAL LEVELS vs FREQUENCY

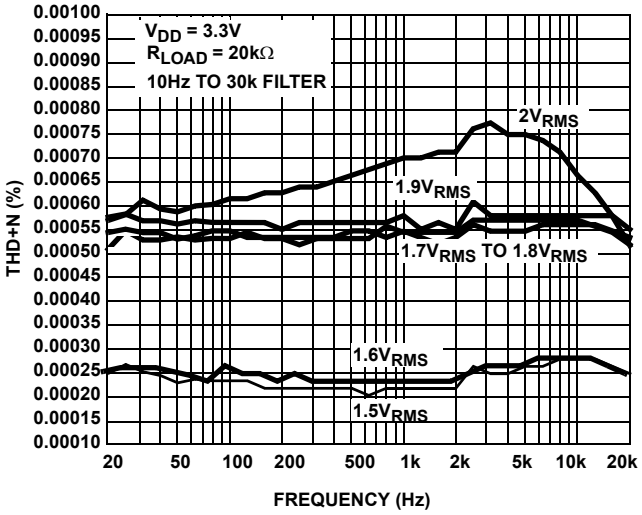


FIGURE 23. THD+N vs SIGNAL LEVELS vs FREQUENCY

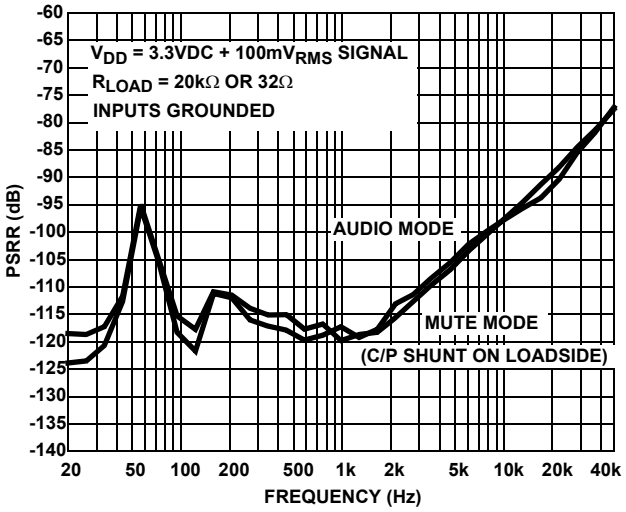


FIGURE 24. PSRR vs FREQUENCY

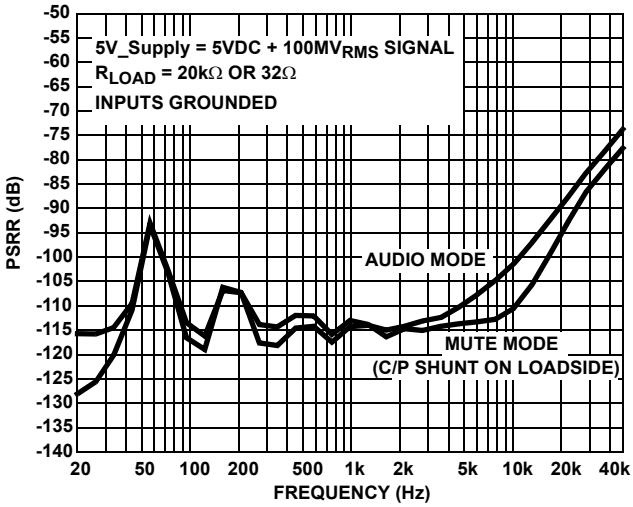


FIGURE 25. PSRR vs FREQUENCY

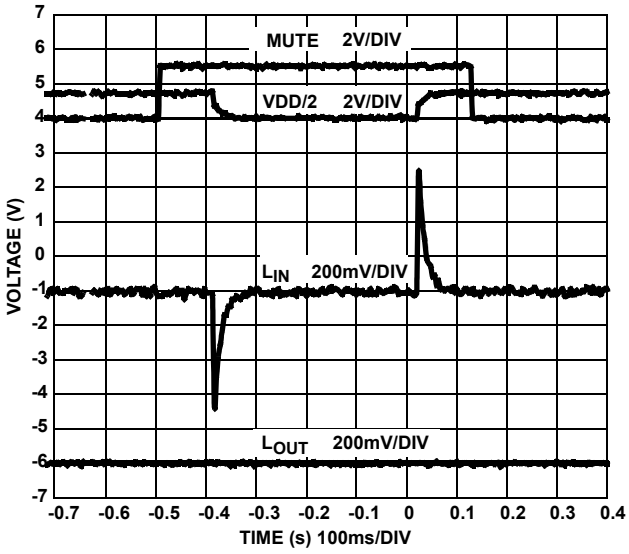


FIGURE 26. 20kΩ AC COUPLED CLICK/POP REDUCTION

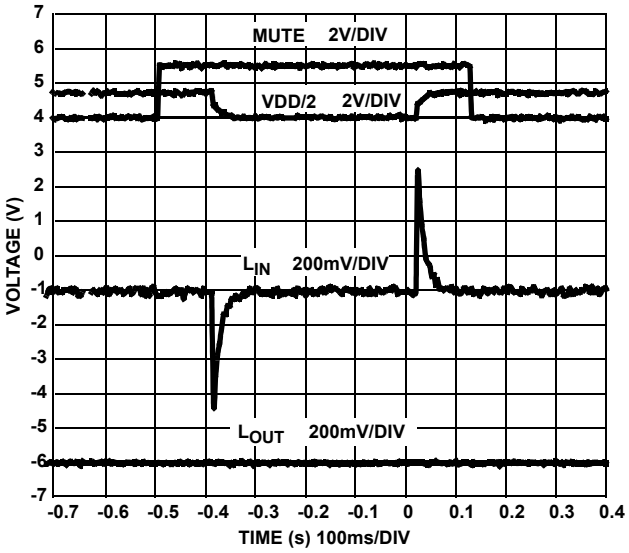


FIGURE 27. 32Ω AC COUPLED CLICK/POP REDUCTION

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified (Continued)

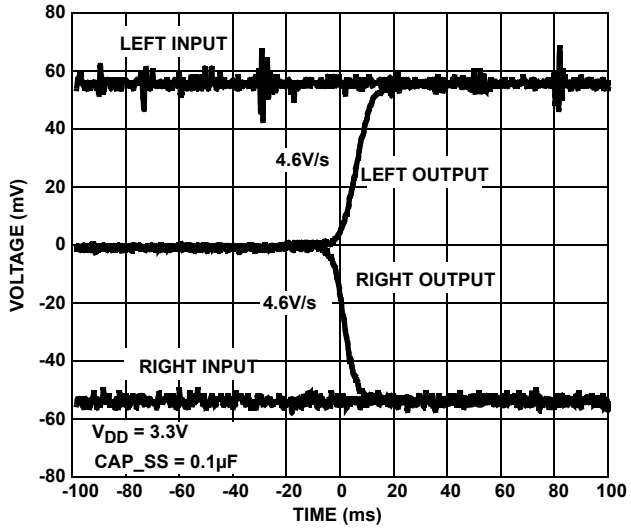


FIGURE 28. SOFT-START (0.1µF) CLICK/POP REDUCTION

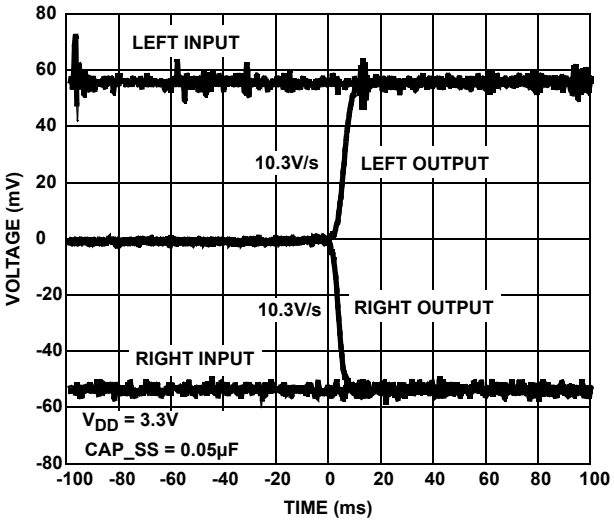


FIGURE 29. SOFT-START (0.05µF) CLICK/POP REDUCTION

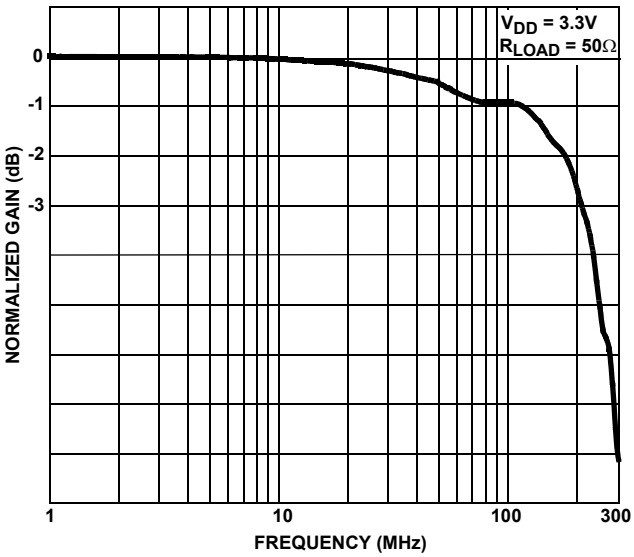


FIGURE 30. FREQUENCY RESPONSE

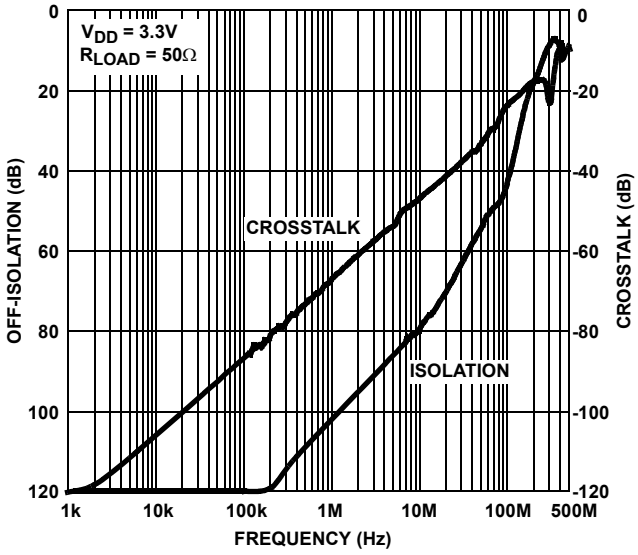


FIGURE 31. CROSSTALK AND OFF-ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

3376

PROCESS:

Submicron CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 6, 2014	FN6699.2	Updated entire datasheet to new format. Updated Ordering Information on page 3. Updated Θ_{JA} and Θ_{JC} for the TSSOP package on page 4. Added section, "Click and POP Elimination When Connected to High Impedance Source and Load" on page 11 Replaced the PODs with the latest revision.
June 5, 2008	FN6699.1	Updated typo in Figure 28 on page 16 - changed "CAP_SS = 0.5µF" to be "CAP_SS = 0.05µF" to match value in title.
May 15, 2008	FN6699.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

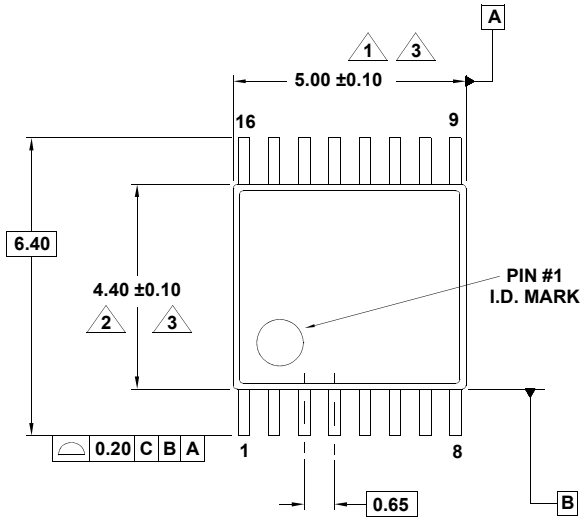
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

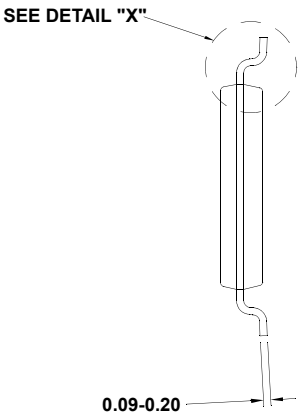
Package Outline Drawing

M16.173

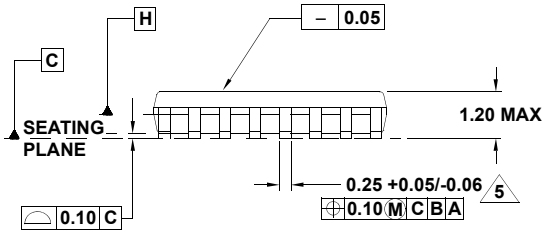
16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



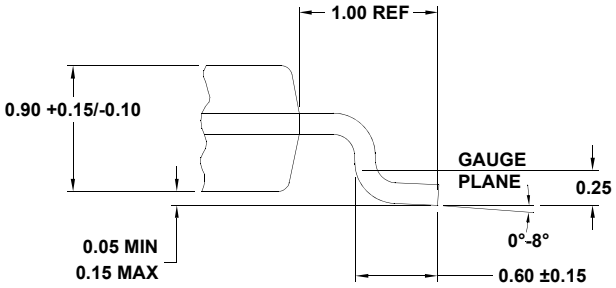
TOP VIEW



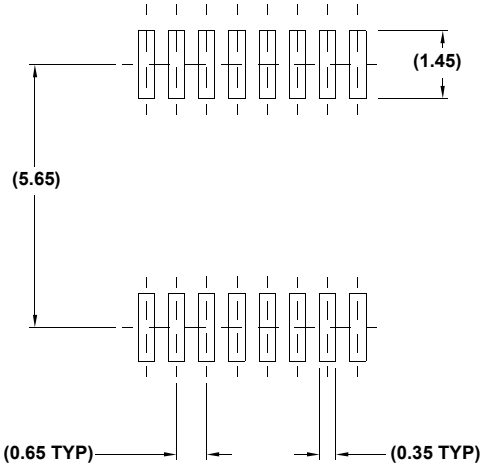
END VIEW



SIDE VIEW



DETAIL "X"

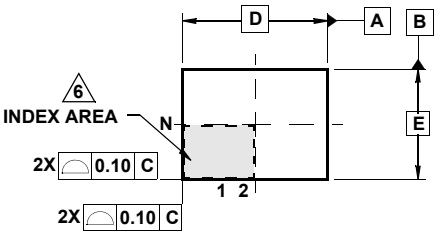


TYPICAL RECOMMENDED LAND PATTERN

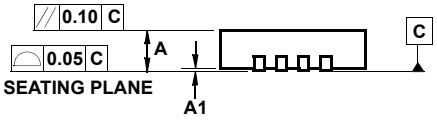
NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

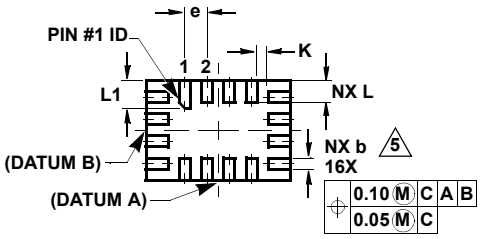
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



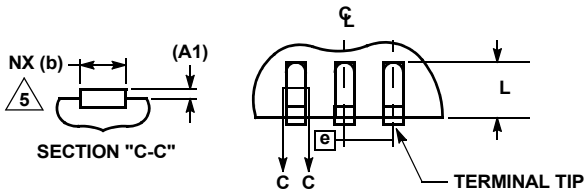
TOP VIEW

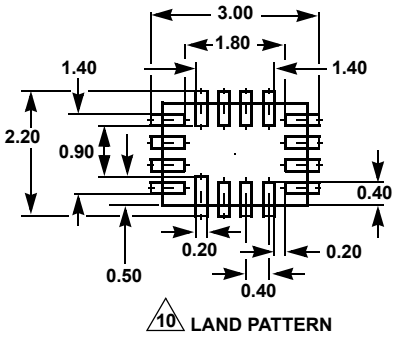


SIDE VIEW



BOTTOM VIEW





L16.2.6x1.8A

16 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.55	2.60	2.65	-
E	1.75	1.80	1.85	-
e		0.40 BSC		-
K	0.15	-	-	-
L	0.35	0.40	0.45	-
L1	0.45	0.50	0.55	-
N		16		2
Nd		4		3
Ne		4		3
θ	0	-	12	4

Rev. 6 1/14

NOTES:

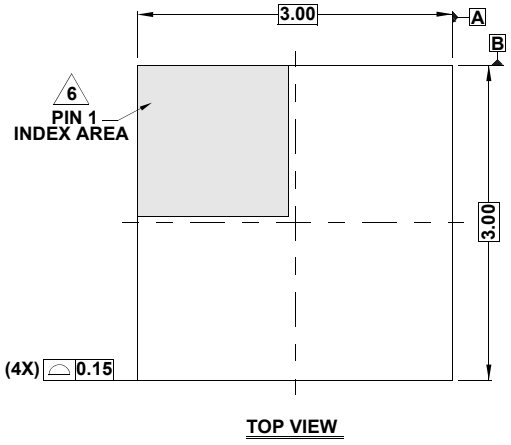
1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

Package Outline Drawing

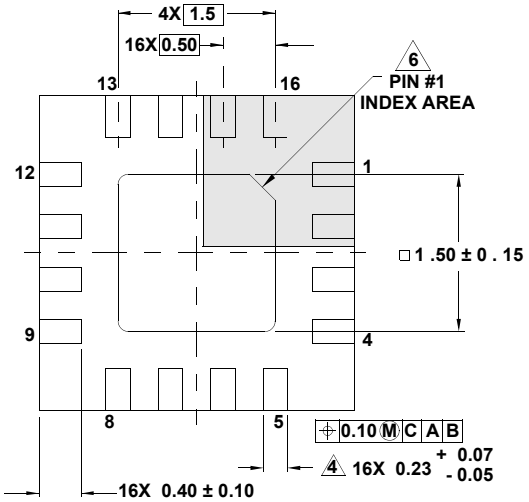
L16.3x3A

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

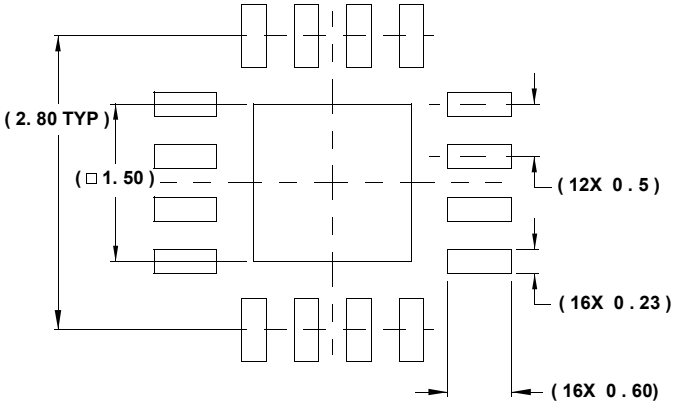
Rev 1, 7/11



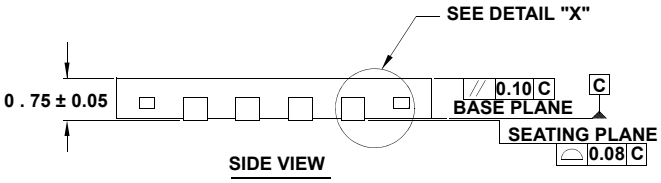
TOP VIEW



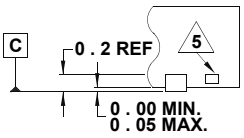
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.