# HMU16, HMU17

January 1994

## 16 x 16-Bit CMOS Parallel Multipliers



### Features

- 16 x 16-Bit Parallel Multiplier with Full 32-Bit Product
- High-Speed (35ns) Clocked Multiply Time
- Low Power Operation:
  - $I_{CCSB}$ = 500µA Maximum
  - $I_{CCOP}$ = 7.0mA Maximum at 1MHz
- Supports Two's Complement, Unsigned Magnitude and Mixed Mode Multiplication
- HMU16 is Compatible with the AM29516, LMU16, IDT7216 and the CY7C516
- HMU17 is Compatible with the AM29517, LMU17, IDT7217 and the CY7C517
- TTL Compatible Inputs/Outputs
- Three-State Outputs

### Applications

- Fast Fourier Transform Analysis
- Digital Filtering
- Graphic Display Systems
- Image Processing
- Radar and Sonar
- Speech Synthesis and Recognition

### Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| HMU16JC-35 | 0°C to +70°C | 68 Lead PLCC |
| HMU16JC-45 | 0°C to +70°C | 68 Lead PLCC |
| HMU16GC-35 | 0°C to +70°C | 68 Lead PGA |
| HMU16GC-45 | 0°C to +70°C | 68 Lead PGA |
| HMU17JC-35 | 0°C to +70°C | 68 Lead PLCC |
| HMU17JC-45 | 0°C to +70°C | 68 Lead PLCC |
| HMU17GC-35 | 0°C to +70°C | 68 Lead PGA |
| HMU17GC-45 | 0°C to +70°C | 68 Lead PGA |

### Description

The HMU16 and HMU17 are high speed, low power CMOS 16 x 16-bit multipliers ideal for fast, real time digital signal processing applications.

The X and Y operands along with their mode controls (TCX and TCY) have 17-bit input registers. The mode controls independently specify the operands as either two's complement or unsigned magnitude format, thereby allowing mixed mode multiplication operations.

Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP). For asynchronous output these registers may be made transparent through the use of the feedthrough control (FT).

Additional inputs are provided for format adjustment and rounding. The format adjust control (FA) allows the user to select either a left shifted 31-bit product or a full 32-bit product, whereas the round control (RND) provides the capability of rounding the most significant portion of the result.

The HMU16 has independent clocks (CLKX, CLKY, CLKL, CLKM) associated with each of these registers to maximize throughput and simplify bus interfacing. The HMU17 has only a single clock input (CLK), but makes use of three register enables ($\overline{ENX}$, $\overline{ENY}$ and $\overline{ENP}$). The $\overline{ENX}$ and $\overline{ENY}$ inputs control the X and Y input registers, while $\overline{ENP}$ controls both the MSP and LSP output registers. This configuration facilitates the use of the HMU17 for microprogrammed systems.

The two halves of the product may be routed to a single 16-bit three-state output port via a multiplexer, and in addition, the LSP is connected to the Y-input port through a separate three-state buffer.

All outputs of the HMU16 and HMU17 multipliers also offer three-state control for multiplexing results onto multiuse busses.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.



File Number **2803.2**

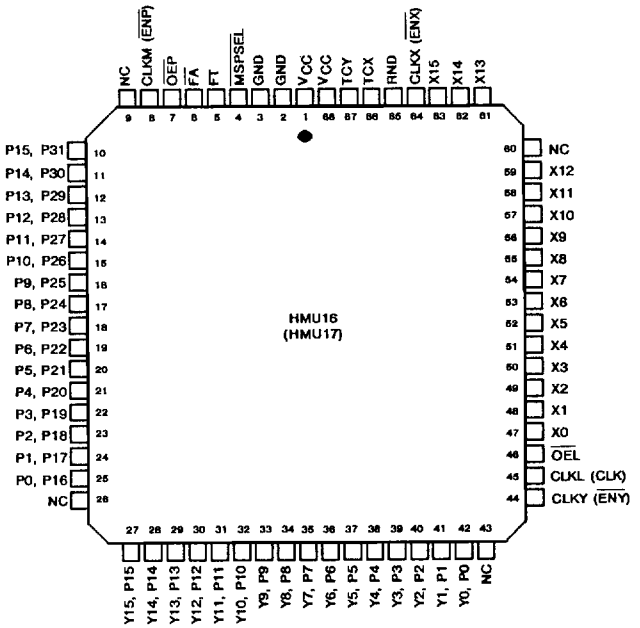
## Package Pinouts

**CERAMIC 68 PIN GRID ARRAY (PGA)**
TOP VIEW

| | A | B | C | D | E | F | G | H | J | K | L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 11 | | N/C | X13 | X15 | RND | TCY | $V_{CC}$ | GND | FT | $\overline{OEP}$ | |
| 10 | X11 | X12 | X14 | CLKX ($\overline{ENX}$) | TCX | $V_{CC}$ | GND | $\overline{MSPSEL}$ | $\overline{FA}$ | CLKM ($\overline{ENP}$) | N/C |
| 9 | X9 | X10 | | | | | | | | P30/ P14 | P31/ P15 |
| 8 | X7 | X8 | | | | | | | | P28/ P12 | P29/ P13 |
| 7 | X5 | X6 | | | | | | | | P26/ P10 | P27/ P11 |
| 6 | X3 | X4 | | | | | | | | P24/ P8 | P25/ P9 |
| 5 | X1 | X2 | | | | | | | | P22/ P6 | P23/ P7 |
| 4 | $\overline{OEL}$ | X0 | | | | | | | | P20/ P4 | P21/ P5 |
| 3 | CLKY ($\overline{ENY}$) | CLKL (CLK) | | | | | | | | P18/ P2 | P19/ P3 |
| 2 | N/C | Y0/ P0 | Y2/ P2 | Y4/ P4 | Y6/ P6 | Y8/ P8 | Y10/ P10 | Y12/ P12 | Y14/ P14 | P16/ P0 | P17/ P1 |
| 1 | | Y1/ P1 | Y3/ P3 | Y5/ P5 | Y7/ P7 | Y9/ P9 | Y11/ P11 | Y13/ P13 | Y15/ P15 | N/C | |

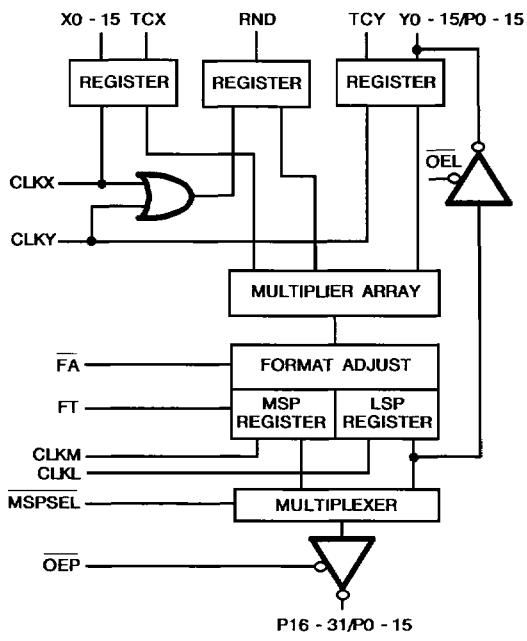
68 LEAD
PIN GRID ARRAY
TOP VIEW

**68 PIN PLASTIC LEADED CHIP CARRIER (PLCC)**
TOP VIEW

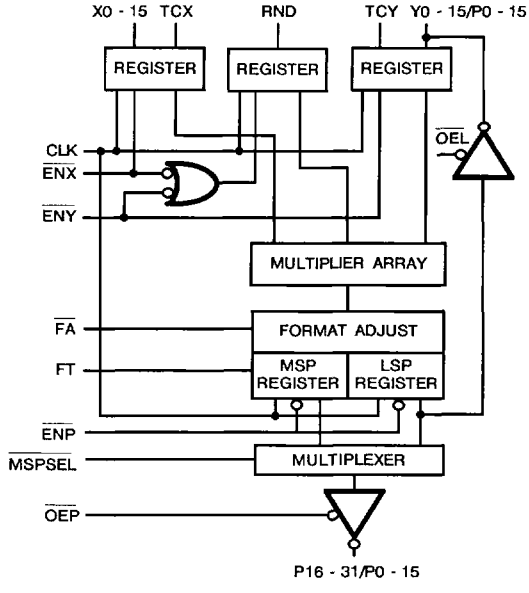


## Functional Block Diagram

HMU16




HMU17



## Pin Description

| SYMBOL | PLCC PIN NUMBER | TYPE | DESCRIPTION |
|---|---|---|---|
| $V_{CC}$ | 1, 68 | | $V_{CC}$. The +5V power supply pins. A 0.1µF capacitor between the $V_{CC}$ and GND pins is recommended. |
| GND | 2, 3 | | GND. The device ground. |
| X0-X15 | 47-59, 61-63 | I | X-Input Data. These 16 data inputs provide the multiplicand which may be in two's complement or unsigned magnitude format. |
| Y0-Y15/ P0-P15 | 27-42 | I/O | Y-Input/LSP Output Data. This 16-Bit port is used to provide the multiplier which may be in two's complement or unsigned magnitude format. It may also be used for output of the Least Significant Product (LSP). |
| P16-P31/ P0-P15 | 10-25 | O | Output Data. This 16-Bit port may provide either the MSP (P16-31) or the LSP (P0-15). |
| TCY, TCX | 66, 67 | I | Two's Complement Control. Input data is interpreted as two's complement when this control is HIGH. A LOW indicates the data is to be interpreted as unsigned magnitude format. |
| FT | 5 | I | Feedthrough Control. When this control is HIGH, both the MSP and LSP registers are transparent. When LOW, the registers are latched by their associated clock signals. |
| FA | 6 | I | Format Adjust Control. A full 32-bit product is selected when this control line is HIGH. A LOW on this control line selects a left shifted 31-bit product with the sign bit replicated in the LSP. This control is normally HIGH except for certain two's complement integer and fractional applications. |
| RND | 65 | I | Round Control. When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the LSP. This position is dependent on the FA control; FA = HIGH indicates RND adds to the 2-15 bit (P15), and FA = LOW indicates RND adds to the $2^{-16}$ bit (P14). |
| $\overline{\text{MSPSEL}}$ | 4 | I | Output Multiplexer Control. When this control is LOW, the MSP is available for output at the dedicated output port, and the LSP is available at the Y-input/LSP output port. When $\overline{\text{MSPSEL}}$ is HIGH, the LSP is available at both ports and the MSP is not available for output. |
| $\overline{\text{OEL}}$ | 46 | I | Y-In/P0-15 Output Port Three-state Control. When $\overline{\text{OEL}}$ is HIGH, the output drivers are in the high impedance state. This state is required for Y-data input. When $\overline{\text{OEL}}$ is LOW, the port is enabled for LSP output. |
| $\overline{\text{OEP}}$ | 7 | I | P16-31/P0-15 Output Port Three-state Control. A LOW on this control line enables the output port. When $\overline{\text{OEP}}$ is HIGH, the output drivers are in the high impedance state. |
| The following Pin Descriptions apply to the HMU16 only. | | | |
| CLKX | 64 | I | X-Register Clock. The rising edge of this clock loads the X-data input register along with the TCX and RND registers. |
| CLKY | 44 | I | Y-Register Clock. The rising edge of this clock loads the Y-data input register along with the TCY and RND registers. |
| CLKM | 8 | I | MSP Register Clock. The rising edge of CLKM loads the most significant product (MSP) register. |
| CLKL | 45 | I | LSP Register Clock. The rising edge of CLKL loads the least significant product (LSP) register. |
| The following Pin Descriptions apply to the HMU17 only. | | | |
| CLK | 45 | I | Clock. The rising edge of this clock will load all enabled registers. |
| $\overline{\text{ENX}}$ | 64 | I | X-Register Enable. When $\overline{\text{ENX}}$ is LOW, the X-register is enabled; X-input data and TCX will be latched at the rising edge of CLK. When $\overline{\text{ENX}}$ is high, the X-register is in a hold mode. |
| $\overline{\text{ENY}}$ | 44 | I | Y-Register Enable. $\overline{\text{ENY}}$ enables the Y-register. (See $\overline{\text{ENX}}$). |
| $\overline{\text{ENP}}$ | 8 | I | Product Register Enable. $\overline{\text{ENP}}$ enables the product register. Both the MSP and LSP sections are enabled by $\overline{\text{ENP}}$. (See $\overline{\text{ENX}}$). |

## Functional Description

The HMU16/HMU17 are high speed 16 X 16-bit multipliers designed to perform very fast multiplication of two 16-bit binary numbers. The two 16-bit operands (X and Y) may be independently specified as either two's complement or unsigned magnitude format by the two's complement controls (TCX and TCY). When either of these control lines is LOW, the respective operand is treated as an unsigned 16-bit value; and when it is HIGH, the operand is treated as a signed value represented in two's complement format. The operands along with their respective controls are latched at the rising edge of the associated clock signal. The HMU16 accomplishes this through the use of independent clock inputs for each of the input registers (CLKX and CLKY), while the HMU17 utilizes a single clock signal (CLK) along with the X and Y register enable inputs ($\overline{ENX}$ and $\overline{ENY}$).

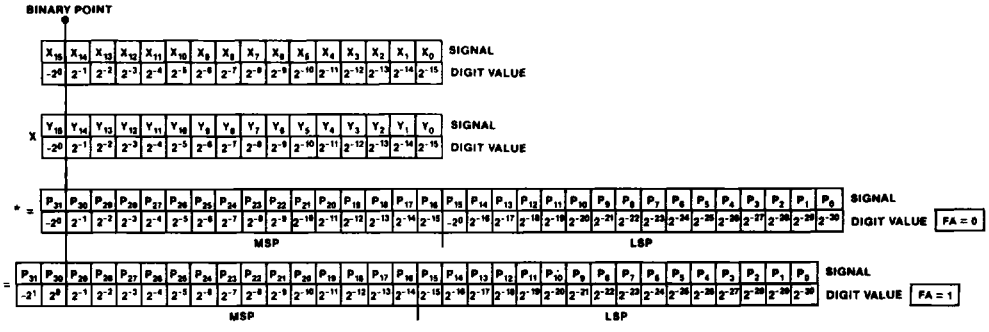
Input controls are also provided for rounding and format adjustment of the 32-bit product. The Round input (RND) is provided to accomodate rounding of the most significant portion of the product by adding one to the Most Significant Bit (MSB) of the LSP register. The position of the MSB is dependent on the state of the Format Adjust Control (See Pin Descriptions and Multiplier Input/Output Format Tables). The Round input is latched into the RND register whenever either of the input registers is clocked. The Format Adjust control ($\overline{FA}$) allows the product output to be formatted. When the $\overline{FA}$ control is HIGH, a full 32-bit product is output; and when $\overline{FA}$ is LOW, a left-shifted 31-bit product is output with the sign bit replicated in bit position 15 of the LSP. The $\overline{FA}$ control must be HIGH for unsigned magnitude, and mixed mode multiplication operations. It may be LOW for certain two's complement integer and fractional operations only (See Multiplier Input/Output Formats Table).

The HMU16/HMU17 multipliers are equipped with two 16-bit output registers (MSP and LSP) which are provided to hold the most and least significant portions of the resultant product respectively. The HMU16 uses independent clocks (CLKM and CLKL) for latching the two output registers, while the HMU17 uses a single clock input (CLK) along with the Product Latch Enable ($\overline{ENP}$). The MSP and LSP registers may also be made transparent for asynchronous output through the use of the Feedthrough control (FT).

There are two output configurations which may be selected when using the HMU16/HMU17 multipliers. The first configuration allows the simultaneous access of the most and least significant halves of the product. When the $\overline{MSPSEL}$ input is LOW, the Most Significant Product will be available at the dedicated output port (P16-31/P0-15). The Least Significant Product is simultaneously available at the bi-directional port shared with the Y-inputs (Y0-15/P0-15) through the use of the LSP output enable ($\overline{OEL}$). The other output configuration involves multiplexing the MSP and LSP registers onto the dedicated output port through the use of the $\overline{MSPSEL}$ control. When the $\overline{MSPSEL}$ control is LOW, the Most Significant Product will be available at the dedicated output port; and when $\overline{MSPSEL}$ is HIGH, the Least Significant Product will be available at this port. This configuration allows access of the entire 32-bit product by a 16-bit wide system bus.

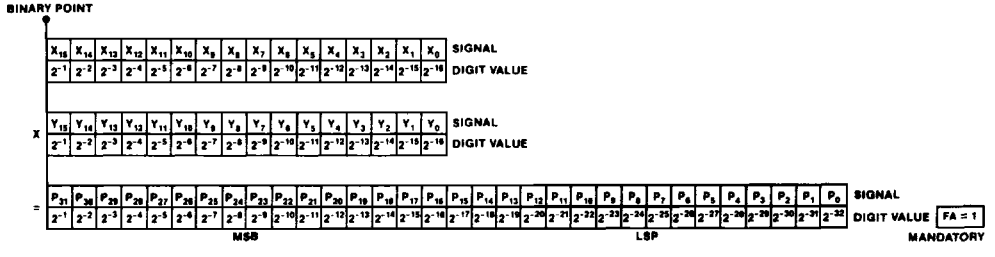
## Multiplier Input/Output Formats Table

### FRACTIONAL TWO'S COMPLEMENT NOTATION

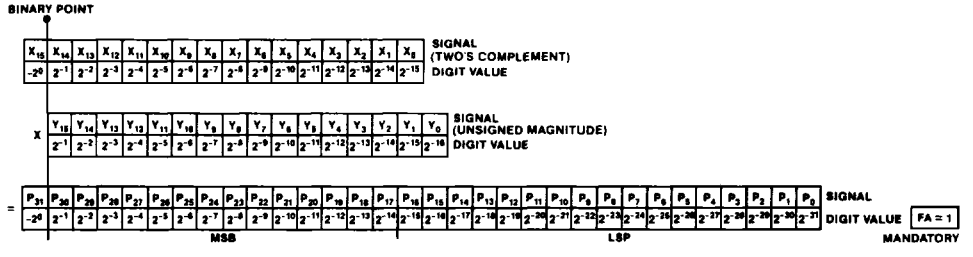



* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000 . . . 0 yielding an erroneous product of -1 in the fraction case and $-2^{30}$ in the integer case.

### FRACTIONAL UNSIGNED MAGNITUDE NOTATION

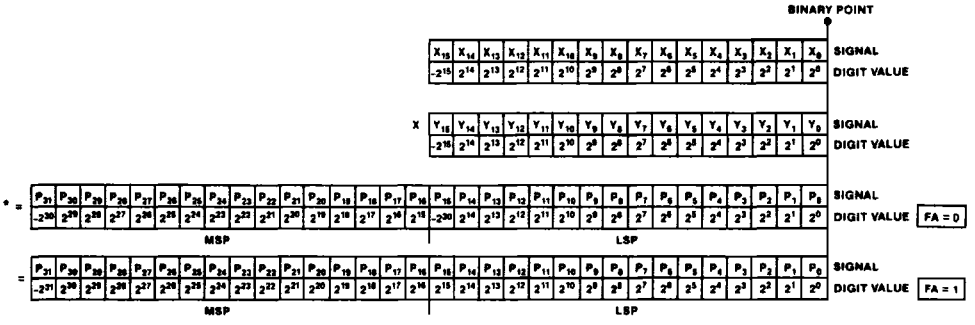



### FRACTIONAL MIXED MODE NOTATION



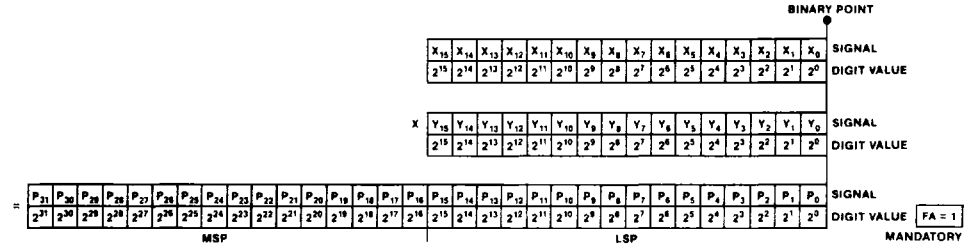
## Multiplier Input/Output Formats Table (Continued)

### INTEGER TWO'S COMPLEMENT NOTATION

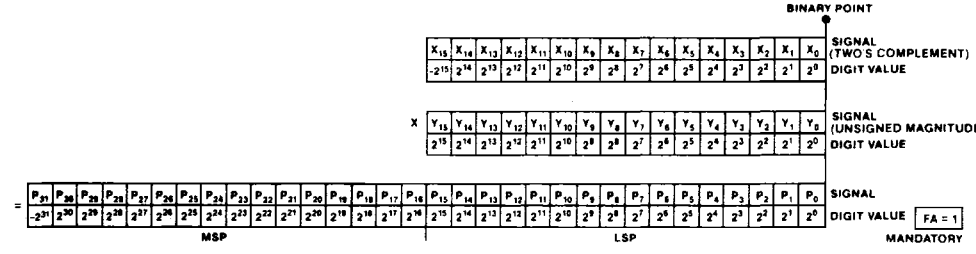



* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000 . . . 0 yielding an erroneous product of −1 in the fraction case and $-2^{30}$ in the integer case.

### INTEGER UNSIGNED MAGNITUDE NOTATION




### INTEGER MIXED MODE NOTATION



## Absolute Maximum Ratings

Supply Voltage ..... +8.0 Volts
Input, Output or I/O Voltage Applied ..... GND-0.5V to $V_{CC}$+0.5V
Storage Temperature Range ..... -65°C to +150°C
Gate Count ..... 4500 Gates
$\theta_{ja}$ ..... 43.2°C/W (PLCC), 42.69°C/W (PGA)
$\theta_{jc}$ ..... 15.1°C/W (PLCC), 10.0°C/W (PGA)
Maximum Package Power Dissipation at 70°C ..... 1.7W (PLCC), 2.46 (PGA)
Junction Temperature ..... +150°C (PLCC), +175°C (PGA)
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

*CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating, and operation at these or any other conditions above those indicated in the operations sections of this specification is not implied.*

## Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... 0°C to +70°C

## D.C. Electrical Specifications ($V_{CC}$ = 5.0V + 5%, $T_A$ = 0°C to +70°C)

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|
| $V_{IH}$ | Logical One Input Voltage | 2.0 | - | V | $V_{CC}$ = 5.25V |
| $V_{IL}$ | Logical Zero Input Voltage | - | 0.8 | V | $V_{CC}$ = 4.75V |
| $V_{OH}$ | Output High Voltage | 2.6 | - | V | $I_{OH}$ = -400µA, $V_{CC}$ = 4.75V |
| $V_{OL}$ | Output Low Voltage | - | 0.4 | V | $I_{OL}$ = +4.0mA, $V_{CC}$ = 4.75V |
| $I_I$ | Input Leakage Current | -10 | 10 | µA | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 5.25V |
| $I_O$ | Output or I/O Leakage Current | -10 | 10 | µA | $V_O$ = $V_{CC}$ or GND, $V_{CC}$ = 5.25V |
| $I_{CCSB}$ | Standby Power Supply Current | - | 500 | µA | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 5.25V Outputs Open |
| $I_{CCOP}$ | Operating Power Supply Current | - | 7.0 | mA | $V_I$ = $V_{CC}$ or GND, $V_{CC}$ = 5.25V f = 1MHz (Note 1) |

## Capacitance ($T_A$ = +25°C, Note 2)

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 15 | pF | Frequency = 1MHz. All measurements referenced to device Ground. |
| $C_{OUT}$ | Output Capacitance | 10 | pF | |
| $C_{I/O}$ | I/O Capacitance | 10 | pF | |

NOTES:

1. Operating Supply Current is proportional to frequency, Typical rating is 5mA/MHz.
2. Not tested, but characterized at initial design and at major process/ design changes.

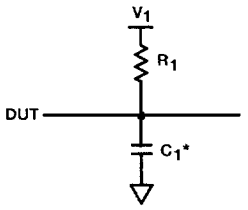
**A.C. Electrical Specifications** ($V_{CC}$ = 5.0V + 5%, $T_A$ = 0°C to +70°C, Note 3)

| SYMBOL | PARAMETER | HMU16/HMU17-35 | | HMU16/HMU17-45 | | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| $T_{MUC}$ | Unclocked Multiply Time | - | 55 | - | 70 | ns | |
| $T_{MC}$ | Clocked Multiply Time | - | 35 | - | 45 | ns | |
| $T_S$ | X, Y, RND Setup Time | 15 | - | 18 | - | ns | |
| $T_H$ | X, Y, RND Hold Time | 2 | - | 2 | - | ns | |
| $T_{PWH}$ | Clock Pulse Width High | 10 | - | 15 | - | ns | |
| $T_{PWL}$ | Clock Pulse Width Low | 10 | - | 15 | - | ns | |
| $T_{PDSEL}$ | $\overline{\text{MSPSEL}}$ to Product Out | - | 22 | - | 25 | ns | |
| $T_{PDP}$ | Output Clock to P | - | 22 | - | 25 | ns | |
| $T_{PDY}$ | Output Clock to Y | - | 22 | - | 25 | ns | |
| $T_{ENA}$ | 3-State Enable Time | - | 22 | - | 25 | ns | Note 1 |
| $T_{DIS}$ | 3-State Disable Time | - | 22 | - | 25 | ns | |
| $T_{SE}$ | Clock Enable Setup Time (HMU17 only) | 15 | - | 15 | - | ns | |
| $T_{HE}$ | Clock Enable Hold Time (HMU17 only) | 2 | - | 2 | - | ns | |
| $T_{HCL}$ | Clock Low Hold Time CLKXY Relative to CLKML (HMU16 only) | 0 | - | 0 | - | ns | Note 2 |
| $T_R$ | Output Rise Time | - | 8 | - | 8 | ns | From 0.8V to 2.0V |
| $T_F$ | Output Fall Time | - | 8 | - | 8 | ns | From 2.0V to 0.8V |

NOTES:

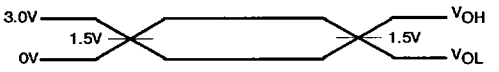
1. Transition is measured at ±200mV from steady state voltage with loading specified in A.C. Test Circuit, $V_1$ = 1.5V, $R_1$ = 500Ω and $C_1$ = 40pF
2. To ensure the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.
3. Refer to A.C. Test Circuit, with $V_1$ = 2.4V, $R_1$ = 500Ω and $C_1$ = 40pF

## A.C. Test Circuit




* Includes Stray and Jig Capacitance

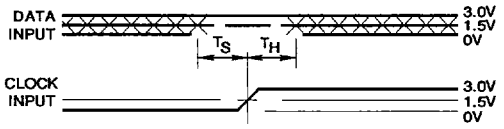
## A.C. Testing Input, Output Waveforms



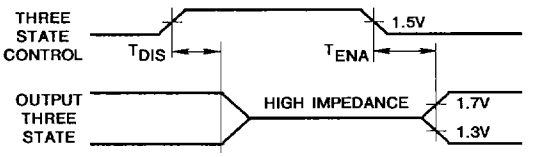

A.C. Testing: All parameters tested as per test circuit. Input rise and fall times are driven at 1ns/V.

## Timing Diagram

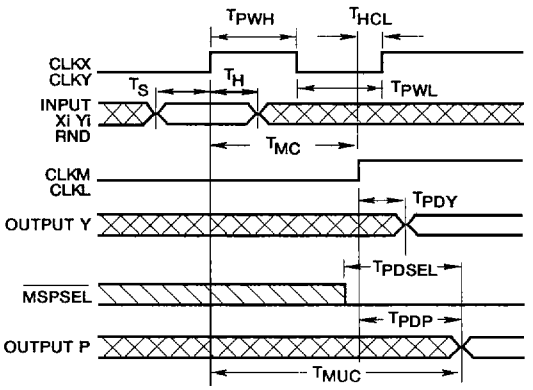
SET-UP AND HOLD TIME




THREE STATE CONTROL




HMU16 TIMING DIAGRAM




HMU17 TIMING DIAGRAM