



# 16×16-Bit CMOS Single Port Multiplier/Accumulator

## ADSP-1110A

### 1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 16×16-bit multiplier/accumulator integrated circuit.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

| Device | Part Number         |
|--------|---------------------|
| -1     | ADSP-1110AS(X)/883B |
| -2     | ADSP-1110AT(X)/883B |

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

| (X) | Package | Description    |
|-----|---------|----------------|
| D   | D-28    | 28-Pin DIP     |
| E   | E-28    | 28-Contact LCC |

### 1.3 Absolute Maximum Ratings.

|                                       |       |                    |
|---------------------------------------|-------|--------------------|
| Supply Voltage                        | ..... | -0.3 V to 7 V      |
| Input Voltage                         | ..... | -0.3 V to $V_{DD}$ |
| Output Voltage                        | ..... | -0.3 V to $V_{DD}$ |
| Operating Temperature Range (Ambient) | ..... | -55°C to +125°C    |
| Storage Temperature Range             | ..... | -65°C to +150°C    |
| Lead Temperature (Soldering 10 sec)   | ..... | +300°C             |

### 1.5 Thermal Characteristics.

Maximum Thermal Resistance  $\theta_{JC}$ : see MIL-M-38510, Appendix C.

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| Test  | Symbol            | Device | Design Limit @ +25°C | Sub Group 1 | Sub Group 2, 3 | Sub Group 9, 10, 11 | Test Condition <sup>1</sup>                             | Units  |
|---|-------------------|--------|----------------------|-------------|----------------|---------------------|---|--------|
| Digital Input High Voltage*                 | V <sub>IH</sub>   | -1, 2  | 2.0                  | 2.2         | 2.2            |                     | V <sub>DD</sub> = max                                   | V min  |
| Digital Input Low Voltage                   | V <sub>IL</sub>   | -1, 2  | 0.8                  | 0.8         | 0.8            |                     | V <sub>DD</sub> = min                                   | V max  |
| Digital Output High Voltage                 | V <sub>OH</sub>   | -1, 2  | 2.4                  | 2.4         | 2.4            |                     | V <sub>DD</sub> = min<br>I <sub>OH</sub> = -1 mA        | V min  |
| Digital Output Low Voltage*                 | V <sub>OL</sub>   | -1, 2  | 0.4                  | 0.6         | 0.6            |                     | V <sub>DD</sub> = min<br>I <sub>OH</sub> = +4 mA        | V max  |
| Digital Input High Current                  | I <sub>IH</sub>   | -1, 2  | 10                   | 10          | 10             |                     | V <sub>DD</sub> = max<br>V <sub>IN</sub> = +5.0 V       | μA max |
| Digital Input Low Current                   | I <sub>IL</sub>   | -1, 2  | 10                   | 10          | 10             |                     | V <sub>DD</sub> = max<br>V <sub>IN</sub> = 0.0 V        | μA max |
| Three-State Leakage*<br>Current Low         | I <sub>OZL</sub>  | -1, 2  | 50                   | 50          | 50             |                     | V <sub>DD</sub> = max<br>V <sub>IL</sub> = 0 V (High Z) | μA max |
| Three-State Leakage<br>Current High         | I <sub>OZH</sub>  | -1, 2  | 50                   | 50          | 50             |                     | V <sub>DD</sub> = max<br>V <sub>IH</sub> = max (High Z) | μA max |
| Supply Current*                             | I <sub>DD1</sub>  | -1, 2  | 70                   | 80          | 80             |                     | V <sub>DD</sub> = max; TTL<br>Inputs; f = max           | mA max |
|   | I <sub>DD2</sub>  | -1, 2  | 35                   | 40          | 40             |                     | V <sub>DD</sub> = max<br>* All V <sub>IN</sub> = 2.4 V  | mA max |
| Clock Pulse Width                           | t <sub>PW</sub>   | -1, 2  | 15                   |             |                | 15                  | Note 2  | ns min |
| Input Control Hold Time                     | t <sub>CH</sub>   | -1, 2  | 5                    |             |                | 6                   | Note 2  | ns min |
| Input Data Setup Time                       | t <sub>DS</sub>   | -1, 2  | 15                   |             |                | 15                  | Note 2  | ns min |
| Clock Period*                               | t <sub>CLK</sub>  | -1     | 50                   |             |                | 60                  | Note 2  | ns min |
|   |                   | -2     | 42.5                 |             |                | 50                  |   |        |
| Input Control Setup Time                    | t <sub>CS</sub>   | -1     | 25                   |             |                | 25                  | Note 2  | ns min |
|   |                   | -2     | 20                   |             |                | 20                  |   |        |
| Input Data Hold Time*                       | t <sub>DH</sub>   | -1, 2  | 3                    |             |                | 4                   | Note 2  | ns min |
| Multiply/Accumulate Time*                   | t <sub>MAC</sub>  | -1     | 100                  |             |                | 120                 | Note 2  | ns max |
|   |                   | -2     | 85                   |             |                | 100                 |   |        |
| Control to Valid Output*                    | t <sub>D</sub>    | -1     | 30                   |             |                | 30                  | Note 2  | ns max |
|   |                   | -2     | 25                   |             |                | 30                  |   |        |
| Control to Valid Output*<br>with Saturation | t <sub>DSAT</sub> | -1     | 35                   |             |                | 40                  | Note 2  | ns max |
|   |                   | -2     | 32                   |             |                | 35                  |   |        |
| Output Driver Disable Time                  | t <sub>DIS</sub>  | -1, 2  | 25                   |             |                | 25                  | Notes 2 and 3   | ns max |
| Control to Overflow Flag*                   | t <sub>O</sub>    | -1     | 30                   |             |                | 35                  | Note 2  | ns max |
|   |                   | -2     | 25                   |             |                | 30                  |   |        |
| Control to Overflow Flag*<br>W/SL           | t <sub>LO</sub>   | -1     | 40                   |             |                | 45                  | Note 2  | ns max |
|   |                   | -2     | 35                   |             |                | 45                  |   |        |

## NOTES

\*Indicates that a limit for this parameter has changed from REV. C.

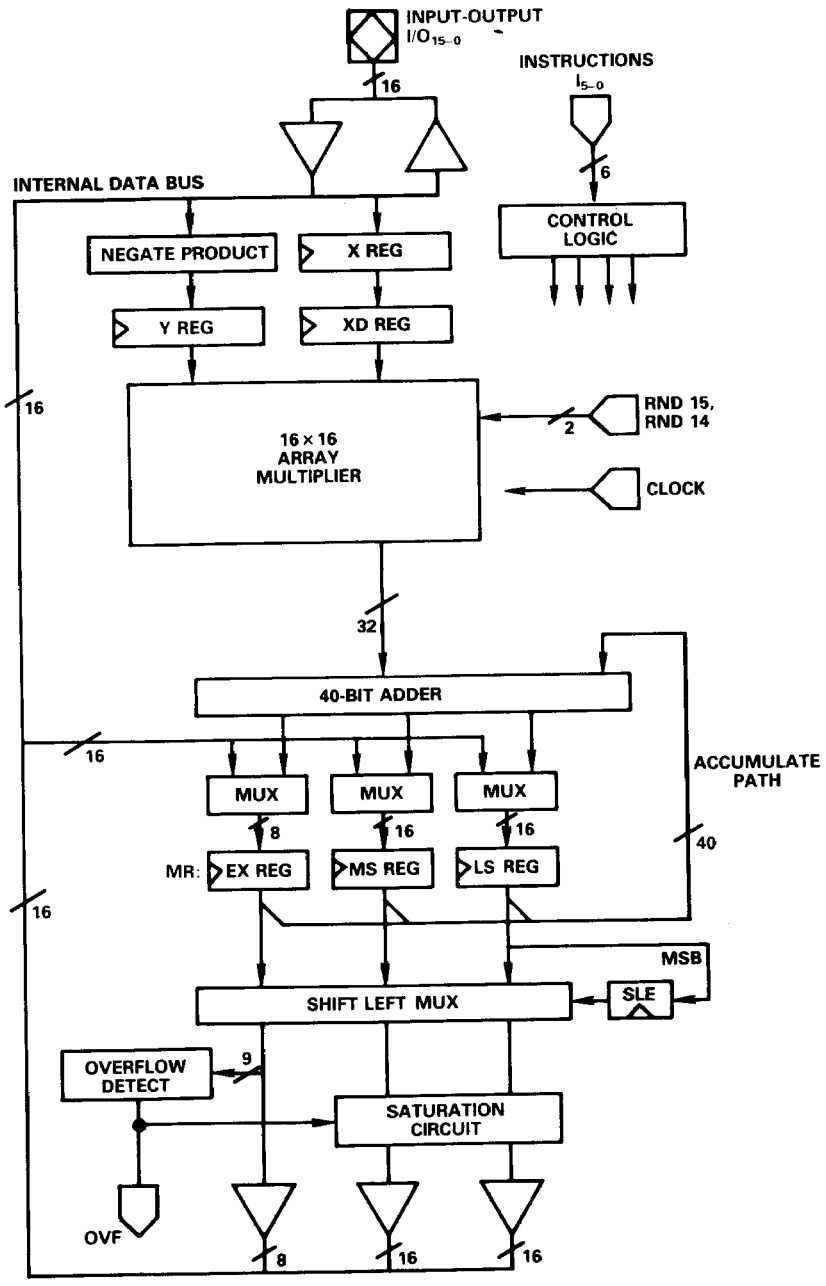
<sup>1</sup>T<sub>A</sub> = +25°C; V<sub>DD</sub> = +4.5 V min to +5.5 V max (unless otherwise noted).

<sup>2</sup>TTL inputs of 0 V and +3.0 V; V<sub>DD</sub> = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).

<sup>3</sup>Transitions measured per Figure 2.

Table 1.

## 3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

| PIN | FUNCTION          | PIN | FUNCTION          |
|-----|-------------------|-----|-------------------|
| 1   | RND15             | 15  | CLK               |
| 2   | RND14             | 16  | I <sub>3</sub>    |
| 3   | I/O <sub>14</sub> | 17  | I <sub>4</sub>    |
| 4   | I/O <sub>12</sub> | 18  | I <sub>5</sub>    |
| 5   | I/O <sub>10</sub> | 19  | OVF               |
| 6   | I/O <sub>8</sub>  | 20  | I/O <sub>1</sub>  |
| 7   | I/O <sub>6</sub>  | 21  | I/O <sub>3</sub>  |
| 8   | I/O <sub>4</sub>  | 22  | I/O <sub>5</sub>  |
| 9   | I/O <sub>2</sub>  | 23  | I/O <sub>7</sub>  |
| 10  | I/O <sub>0</sub>  | 24  | I/O <sub>9</sub>  |
| 11  | I <sub>0</sub>    | 25  | I/O <sub>11</sub> |
| 12  | I <sub>1</sub>    | 26  | I/O <sub>13</sub> |
| 13  | I <sub>2</sub>    | 27  | I/O <sub>15</sub> |
| 14  | GND               | 28  | V <sub>DD</sub>   |

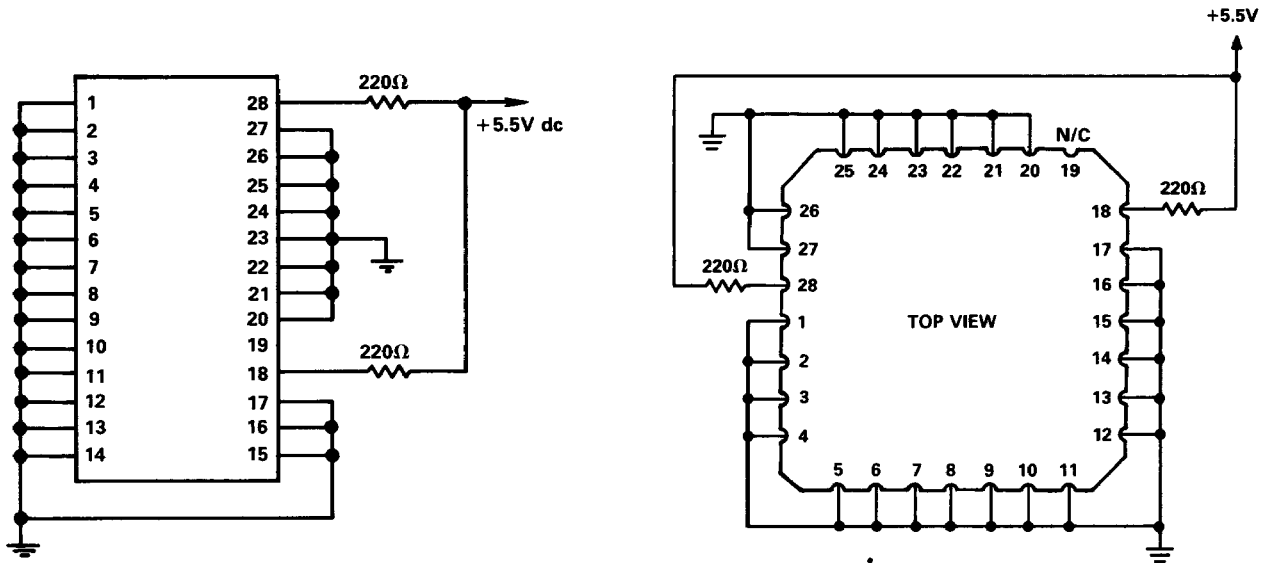
## 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

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## 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1110AD Life Test and Burn-In Circuit

ADSP-1110AE Life Test and Burn-In Circuit

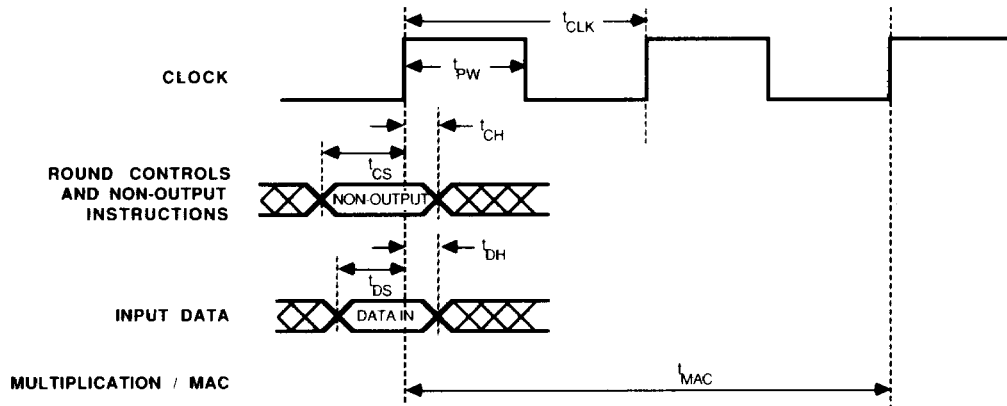


Figure 1. ADSP-1110A Timing: Clocked (Synchronous) Operations All Non-Output Instructions

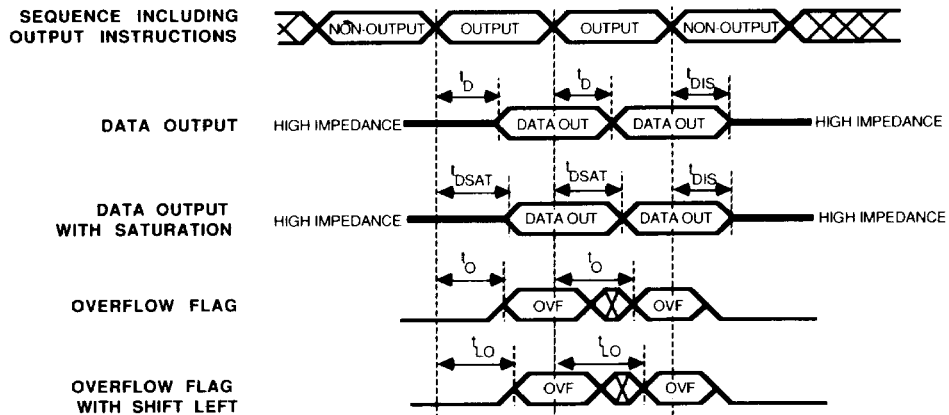


Figure 2. ADSP-1110A Timing: Unlocked (Asynchronous) Operations All Output Instructions

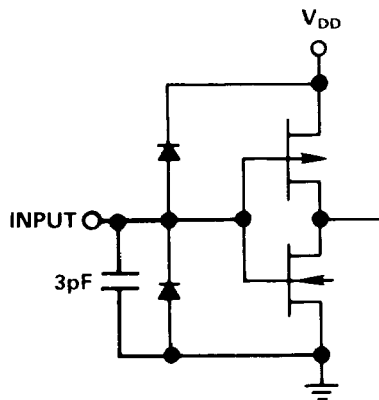


Figure 3. Equivalent Input Circuit

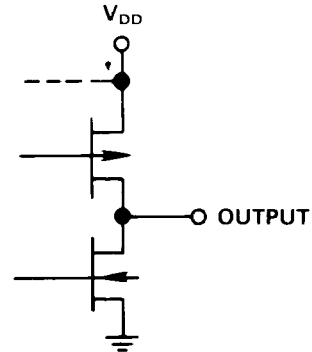


Figure 4. Equivalent Output Circuit

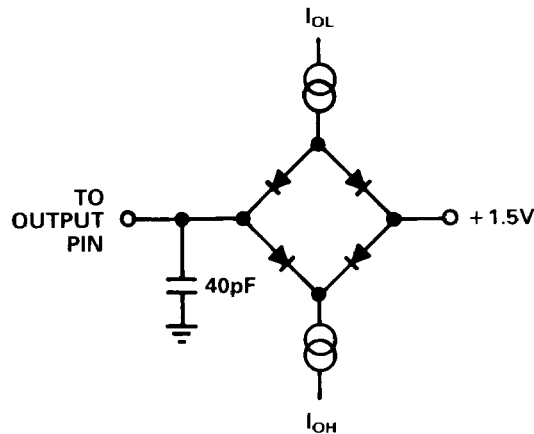


Figure 5. Normal Load Circuit for AC Measurements

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| Instruction Group | Instruction  | Microcode                  | Comments  |
|-------------------|--|----------------------------|---|
|                   |  | Instruction<br>5 4 3 2 1 0 |   |
| Miscellaneous     | NOP  | 0 0 0 0 X X                | No Operation  |
|                   | CKMR   | 0 0 0 1 X X                | Clock MR  |
| Input             | X = BUS  | 0 0 1 0 X X                |   |
| Preload           | LS = BUS   | 0 1 0 0 0 0                |   |
|                   | MS = BUS   | 0 1 0 1 X 0                |   |
|                   | EX = BUS   | 0 1 0 0 1 0                |   |
| Transfer          | LS = MS  | 0 1 0 0 0 1                | Set SLE register  |
|                   | MS = EX  | 0 1 0 1 0 1                |   |
| Sign Extend       | EX = SIGN EXT MS                                     | 0 1 0 0 1 1                |   |
|                   | MS = SIG EXT LS                                      | 0 1 0 1 1 1                |   |
| Output            | BUS = EX   | 0 0 1 1 0 1                | All output instructions are asynchronous<br>I5-I2:<br>0011 = EX<br>0110 = MS<br>0111 = LS<br>I1-I0:<br>01 = to bus<br>00 = to bus shifted<br>10 = to bus shifted w/saturation<br>11 = to bus w/saturation   |
|                   | BUS = EX (sl)  | 0 0 1 1 0 0                |   |
|                   | BUS = MS   | 0 1 1 0 0 1                |   |
|                   | BUS = MS (sl)  | 0 1 1 0 0 0                |   |
|                   | BUS = MS (sat)                                       | 0 1 1 0 1 1                |   |
|                   | BUS = MS (sl, sat)                                   | 0 1 1 0 1 0                |   |
|                   | BUS = LS   | 0 1 1 1 0 1                |   |
|                   | BUS = LS (sl)  | 0 1 1 1 0 0                |   |
|                   | BUS = LS (sat)                                       | 0 1 1 1 1 1                |   |
|                   | BUS = LS (sl, sat)                                   | 0 1 1 1 1 0                |   |
| Multi-Operation   | Y = BUS; CKMR; X <sub>US</sub> *Y <sub>US</sub>      | 1 0 0 X 0 0                | Require two cycles to complete.<br>Other instructions can be executed<br>on the second cycle.<br><br>I5 = Multiply/MAC operation<br>I4 = Y twos complement<br>I3 = X twos complement<br>I2 = Subtract previous result<br>I1 = Add/subtract previous result<br>from product<br>I0 = Negate product |
|                   | Y = BUS; CKMR; -X <sub>US</sub> *Y <sub>US</sub>     | 1 0 0 X 0 1                |   |
|                   | Y = BUS; CKMR; X <sub>US</sub> *Y <sub>US</sub> +MR  | 1 0 0 0 1 0                |   |
|                   | Y = BUS; CKMR; -X <sub>US</sub> *Y <sub>US</sub> +MR | 1 0 0 0 1 1                |   |
|                   | Y = BUS; CKMR; X <sub>US</sub> *Y <sub>US</sub> -MR  | 1 0 0 1 1 0                |   |
|                   | Y = BUS; CKMR; -X <sub>US</sub> *Y <sub>US</sub> -MR | 1 0 0 1 1 1                |   |
|                   | Y = BUS; CKMR; X <sub>TC</sub> *Y <sub>US</sub>      | 1 0 1 X 0 0                |   |
|                   | Y = BUS; CKMR; -X <sub>TC</sub> *Y <sub>US</sub>     | 1 0 1 X 0 1                |   |
|                   | Y = BUS; CKMR; X <sub>TC</sub> *Y <sub>US</sub> +MR  | 1 0 1 0 1 0                |   |
|                   | Y = BUS; CKMR; -X <sub>TC</sub> *Y <sub>US</sub> +MR | 1 0 1 0 1 1                |   |
|                   | Y = BUS; CKMR; X <sub>TC</sub> *Y <sub>US</sub> -MR  | 1 0 1 1 1 0                |   |
|                   | Y = BUS; CKMR; -X <sub>TC</sub> *Y <sub>US</sub> -MR | 1 0 1 1 1 1                |   |
|                   | Y = BUS; CKMR; X <sub>US</sub> *Y <sub>TC</sub>      | 1 1 0 X 0 0                |   |
|                   | Y = BUS; CKMR; -X <sub>US</sub> *Y <sub>TC</sub>     | 1 1 0 X 0 1                |   |
|                   | Y = BUS; CKMR; X <sub>US</sub> *Y <sub>TC</sub> +MR  | 1 1 0 0 1 0                |   |
|                   | Y = BUS; CKMR; -X <sub>US</sub> *Y <sub>TC</sub> +MR | 1 1 0 0 1 1                |   |
|                   | Y = BUS; CKMR; X <sub>US</sub> *Y <sub>TC</sub> -MR  | 1 1 0 1 1 0                |   |
|                   | Y = BUS; CKMR; -X <sub>US</sub> *Y <sub>TC</sub> -MR | 1 1 0 1 1 1                |   |
|                   | Y = BUS; CKMR; X <sub>TC</sub> *Y <sub>TC</sub>      | 1 1 1 X 0 0                |   |
|                   | Y = BUS; CKMR; -X <sub>TC</sub> *Y <sub>TC</sub>     | 1 1 1 X 0 1                |   |
|                   | Y = BUS; CKMR; X <sub>TC</sub> *Y <sub>TC</sub> +MR  | 1 1 1 0 1 0                |   |
|                   | Y = BUS; CKMR; -X <sub>TC</sub> *Y <sub>TC</sub> +MR | 1 1 1 0 1 1                |   |
|                   | Y = BUS; CKMR; X <sub>TC</sub> *Y <sub>TC</sub> -MR  | 1 1 1 1 1 0                |   |
|                   | Y = BUS; CKMR; -X <sub>TC</sub> *Y <sub>TC</sub> -MR | 1 1 1 1 1 1                |   |

## Mnemonic Definitions

|     |   |      |  |
|-----|---|------|--|
| =   | Assign right side to left.                            | sl   | Shift left.  |
| BUS | 16-bit external data bus used for all I/O operations. | sat  | Conditional on overflow, saturate the outputted value. |
| X   | Input register for multiplier.                        | TC   | Twos complement number.                                |
| Y   | Input register for multiplier.                        | US   | Unsigned magnitude number.                             |
| EX  | 8-bit extension register for accumulator.             | SIGN | Sign bit (MSB) of specified register.                  |
| MS  | 16-bit most significant product register.             | CKMR | Clock product into EX, MS and LS.                      |
| LS  | 16-bit least significant product register.            | *    | Multiply   |
| MR  | 40-bit accumulator comprising EX, MS and LS.          | X    | Microcode instruction bit can be either a 0 or 1.      |

Table 2. ADSP-1110A Instruction Set