features

- **10-bit, 21 Mega-Samples Per Second (MSPS), A/D Converter**
- **Single Power Supply Operation, 2.7 V to 3.3 V**
- **Internally Programmable Correlated Double Sampler (CDS) Timing SR and ADCCLK**
- **Very Low Power: 109 mW Typical at 2.7-V, 1.5-mW Power-Down Mode**
- **Full Channel Differential Nonlinearity Error: <±0.5 LSB Typical**
- **Full Channel Integral Nonlinearity Error: <±1.0 LSB Typical**
- **Programmable Optical Black (OB) Level and Offset Calibration**
- **Programmable Gain Amplifier (PGA) With 0-dB to 36-dB Gain Range (0.047 dB/Step) for CCD Mode, 0-dB to 12-dB Gain Range (0.047 dB/Step) for Video Mode**
- **Additional Digital-to-Analog Converters (DACs) for External Analog Setting**
- **Serial Interface for Register Configuration**
- **Internal Reference Voltages**
- **48-Terminal TQFP Package**

applications

- **Digital Still Camera**
- **Digital Camcorder**
- **Digital Video Camera**

description

The VSP10T21 device is a complete charge-coupled device (CCD) and video signal processor/digitizer designed for digital camera and camcorder applications. The VSP10T21 device performs all the analog processing functions necessary to maximize the dynamic range, corrects various errors associated with the CCD sensor, and then digitizes the results with an on-chip high-speed analog-to-digital converter (ADC). One of the key features of this device is an integrated programmable delay generated for the CDS timing control, which eases the AFE timing adjustments for optimum image quality. Other key components of the VSP10T21 device include:

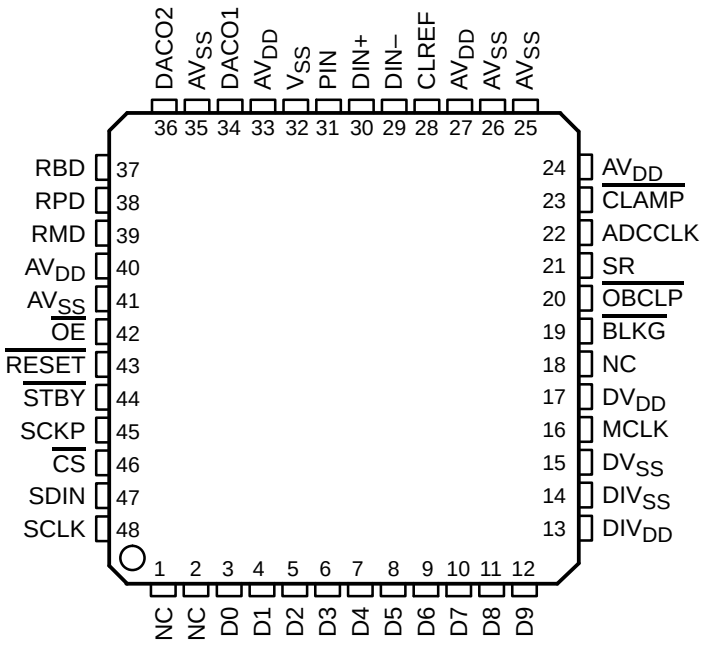
- Input clamp circuitry and a CDS
- Programmable gain amplifier (PGA) with 0-dB to 36-dB gain range (0.047 dB/step) for CCD mode, 0-dB to 12-dB gain range (0.047 dB/step) for video mode
- Internal programmable optical black level and offset calibration
- 10-bit, 21 MSPS pipeline ADC for CCD mode and 28 MSPS ADC for video mode
- Parallel data port for easy microprocessor interface and a serial port for configuring internal control registers
- Two DACs for external system control
- Internal reference voltages

Designed in advanced CMOS process, the VSP10T21 device operates from a single power supply with a normal power consumption of 109 mW at 2.7 V and 21 MSPS and a 1.5-mW power-down mode.

High precision, single 3-V operation, very low power consumption, and fully integrated analog processing circuitry make the VSP10T21 device an ideal CCD signal processing solution for the electronic video camcorder and digital still camera applications.

The part is available in a 48-terminal TQFP package and is specified over an operating temperature range of –20°C to 75°C.

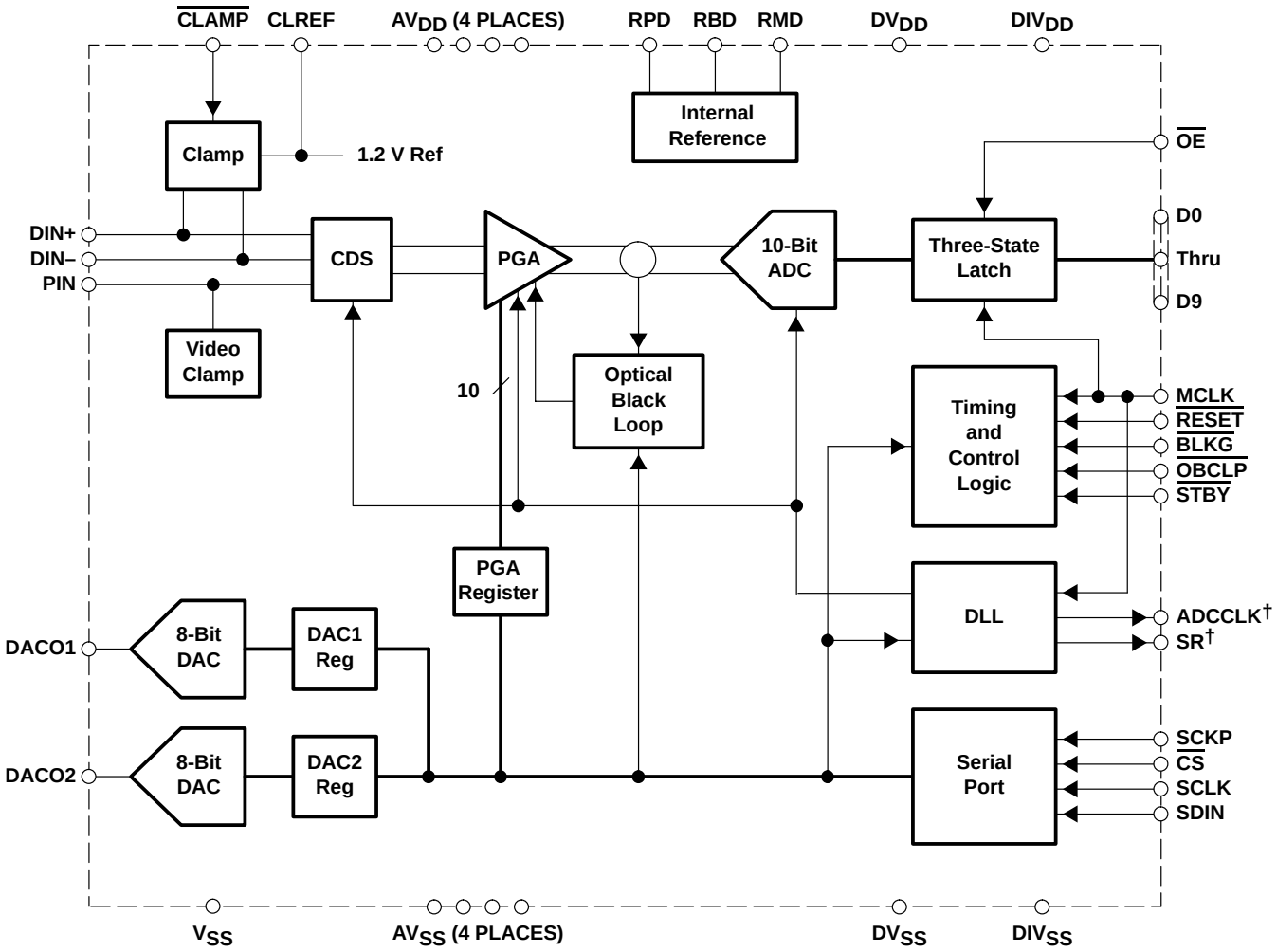
PFB PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE
	TQFP (PFB)
–20°C to 75°C	VSP10T21PFB

functional block diagram



† ADCCLK and SR output signals are only enabled by setting bits D3 (ADEN) and D4 (ROEN) in the clock control register to 1.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADCCLK	22	O	ADCCLK clock output, for probe only
AV_{DD}	24, 27, 33, 40		Analog supply voltage, +3 V
AV_{SS}	25, 26, 35, 41		Analog ground
$\overline{BLKG}$	19	I	Control input. The CDS operation is disabled when $\overline{BLKG}$ is pulled low.
$\overline{CLAMP}$	23	I	CCD signal clamp control input
CLREF	28	O	Clamp reference voltage output
$\overline{CS}$	46	I	Chip select. A logic low on this input enables the VSP10T21 device.
DACO1	34	O	Digital-to-analog converter output 1
DACO2	36	O	Digital-to-analog converter output 2
DIN–	29	I	Differential input signal from CCD
DIN+	30	I	Differential Input signal from CCD
DIV_{DD}	13		Digital interface circuit supply voltage, 1.8 V to 3.6 V
DIV_{SS}	14		Digital interface circuit ground
DV_{DD}	17		Digital supply voltage, +3 V
DV_{SS}	15		Digital ground
D0–D9	3–12	O	10-bit 3-state ADC output data or offset DACs test data
MCLK	16	I	System clock input
NC	1, 2, 18		Not connected
$\overline{OBCLP}$	20	I	Optical black level and offset calibration control input, active low
$\overline{OE}$	42	I	Output data enable, active low
PIN	31	I	Video input signal
RBD	37	O	Internal bandgap reference for external decoupling
$\overline{RESET}$	43	I	Hardware reset input, active low. This signal forces a reset of all internal registers.
RMD	39	O	Ref– output for external decoupling
RPD	38	O	Ref+ output for external decoupling
SCKP	45	I	This terminal selects the polarity of SCLK. 0 = Active low (high when SCLK is not running) 1 = Active high (low when SCLK is not running)
SCLK	48	I	Serial clock input. This clock synchronizes the serial data transfer.
SDIN	47	I	Serial data input to configure the internal registers.
SR	21	O	CCD reference level sample clock output, for probe only
$\overline{STBY}$	44	I	Hardware power-down control input, active low
V_{SS}	32		Analog ground

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AV_{DD}, DV_{DD}, DIV_{DD} . . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital input voltage range . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supplies

PARAMETER		MIN	NOM	MAX	UNIT
AV_{DD}	Analog supply voltage	2.7	3	3.3	V
DV_{DD}	Digital supply voltage	2.7	3	3.3	V
DIV_{DD}	Digital interface supply voltage	1.8		3.6	V

digital inputs

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage	DV_{DD} = 3 V	0.8 DV_{DD}			V
V_{IL}	Low-level input voltage	DV_{DD} = 3 V			0.2 DV_{DD}	V
	Input MCLK frequency	DV_{DD} = 3 V, CCD mode			21	MHz
		DV_{DD} = 3 V, video mode			28	MHz
$t_{w(MCLKH)}$	ADCCLK pulse duration, clock high	DV_{DD} = 3 V	23.8			ns
$t_{w(MCLKL)}$	ADCCLK pulse duration, clock low	DV_{DD} = 3 V	23.8			ns
	Input SCLK frequency	DV_{DD} = 3 V			40	MHz
$t_{w(SCLKH)}$	SCLK pulse duration, clock high	DV_{DD} = 3 V	12.5			ns
$t_{w(SCLKL)}$	SCLK pulse duration, clock low	DV_{DD} = 3 V	12.5			ns

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, AV_{DD} = DV_{DD} = 3 V, MCLK = 21 MHz (unless otherwise noted)

total device

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Device power consumption	AV_{DD} = DV_{DD} = 3 V		130		mW
Device power consumption	AV_{DD} = DV_{DD} = 2.7 V		109		mW
Power consumption in power-down mode			1.5		mW
No missing code			Assured		

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, AV_{DD} = DV_{DD} = 3 V, MCLK = 21 MHz (unless otherwise noted) (continued)

analog-to-digital converter (ADC)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ADC resolution			10 (CCD) 8 (Video)		Bits
INL	Integral nonlinearity	AV_{DD} = DV_{DD} = 2.7 to 3.3 V		±1.0		LSB
DNL	Differential nonlinearity	AV_{DD} = DV_{DD} = 2.7 to 3.3 V		±0.5		LSB
SNR	Input referred signal-to-noise ratio	0 dB gain		60		dB
		36 dB gain		74		

correlated double sampler (CDS) and programmable gain amplifier (PGA)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	CDS and PGA sample rate					21 (CCD) 28 (Video)	MHz
	CDS full scale input span		Single-ended input			1	V
	Input capacitance of CDS				4		pF
	Minimum PGA gain				0	1	dB
	Maximum PGA gain	CCD			36		dB
		Video			12		
	PGA gain resolution				0.047		dB

user digital-to-analog converters (DAC)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC resolution			8		Bits
INL	Integral nonlinearity			±0.5		LSB
DNL	Differential nonlinearity			±0.1		LSB
	Output voltage range		0		AV_{DD}	V
	Output settling time	10-pF external load, settle to 1 mV		4		µs

reference voltages

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal bandgap voltage reference		1.43	1.50	1.58	V
	Temperature coefficient			100		ppm/°C
	ADC Ref+	Externally decoupled		2		V
	ADC Ref–	Externally decoupled		1		V

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, AV_{DD} = DV_{DD} = 3 V, MCLK = 21 MHz (unless otherwise noted) (continued)

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic Inputs						
I_{IH}	High-level input current	DV_{DD} = 3 V	–10		10	µA
I_{IL}	Low-level input current	DV_{DD} = 3 V	–10		10	µA
C_I	Input capacitance			5		pF
Logic Outputs						
V_{OH}	High-level output voltage	I_{OH}= 50 µA, DIV_{DD} = 3 V	DIV_{DD}–0.4			V
V_{OL}	Low-level output voltage	I_{OL}= 50 µA, DIV_{DD} = 3 V		0.4		V
I_{OZ}	High-impedance-state output current			±10		µA
C_o	Output capacitance			5		pF

key timing requirement

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Maximum programming range for SR and ADCCLK timing signals			T†		ns
	SR and ADCCLK programming resolution			T/30		ns
t_{SRW}	SR pulse width	Measured at 50% of pulse height, recommend to use T/4 of ADCCLK cycle	10			ns
t_{SRD}	Delay between the rising edge of external SR test output and the actual sampling instant	Measured at 50% of pulse height			2.4‡	ns
t_{ADCKD}	Delay between the falling edge of external ADCCLK test output and the actual instant of sampling the video signal				1.7§	ns
t_{OD}	The rising edge of MCLK to output data delay			6		ns
t_{CSF}	CS falling edge to SCLK rising edge		0			ns
t_{CSR}	SCLK falling edge to CS rising edge		5			ns

† T is the time period of MCLK.

‡ SR is the internally generated timing. Due to the pad delay on the output SR, the maximum of the SR delay is 2.4 ns. It must not be delayed further on the positive direction unless it crosses a full pixel period (refer to Figure 2). The target for the SR position is to make sure that the rising edge of SR sample the reference level of the CCD signal.

§ ADCCLK is the internally generated timing. Due to the pad delay on the output ADCCLK, the maximum of the ADCCLK delay is 1.7 ns. It must not be delayed further on the positive direction unless it crosses a full pixel period (refer to Figure 2). The target for the SR position is to make sure that the falling edge of ADCCLK sample the video level of the active instant of the CCD signal.

NOTE: The digital output is latched out by MCLK.

TYPICAL CHARACTERISTICS

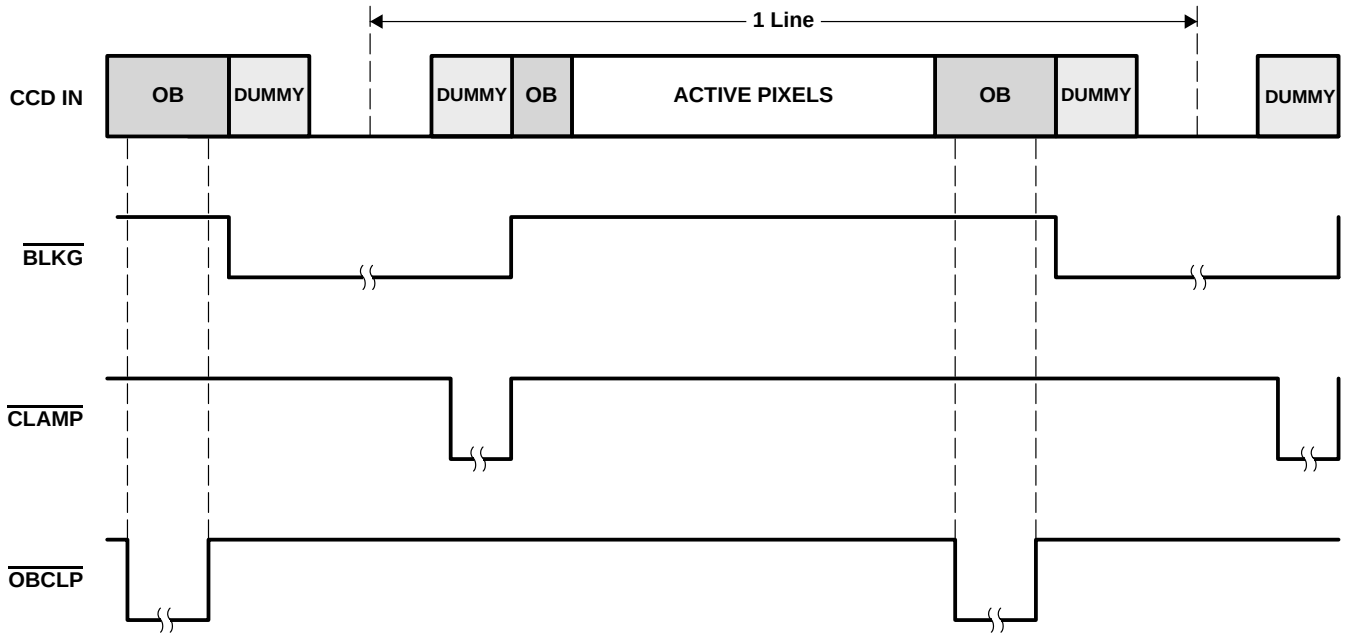
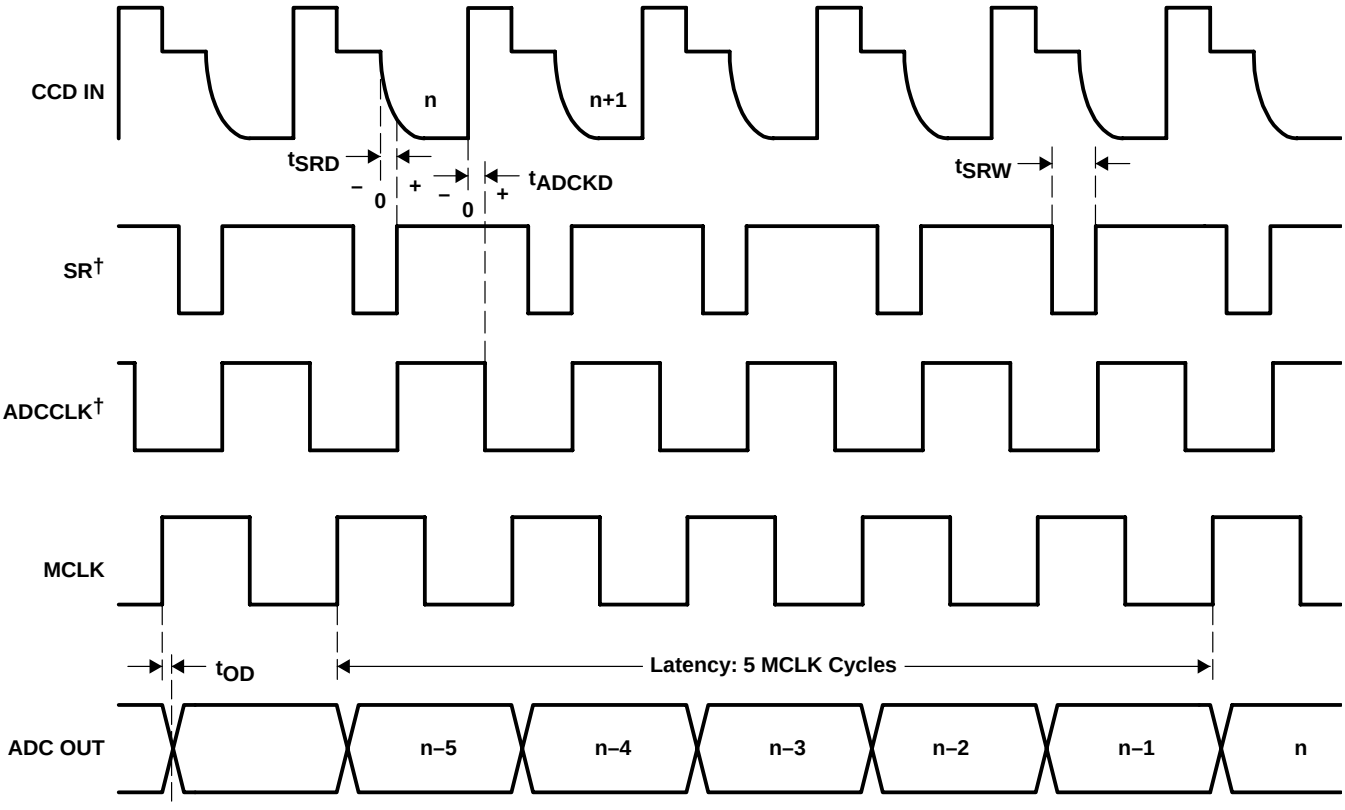


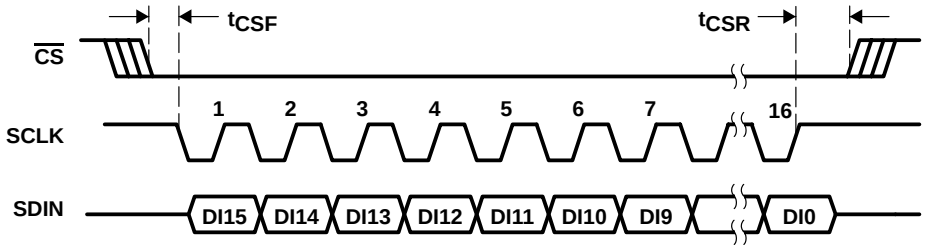
Figure 1. CCD Horizontal Synchronization Timing Diagram



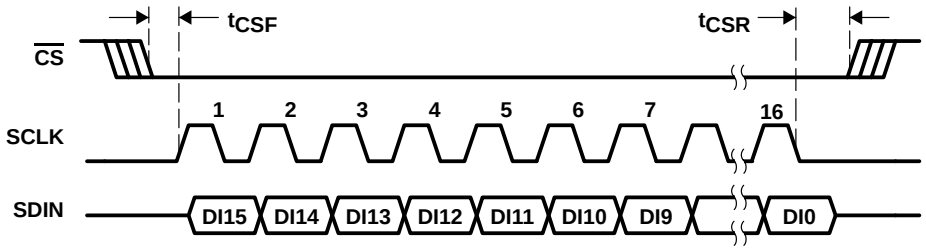
† SR and ADCCLK are external signals.

Figure 2. CCD Pixel Synchronization Timing Diagram

TYPICAL CHARACTERISTICS



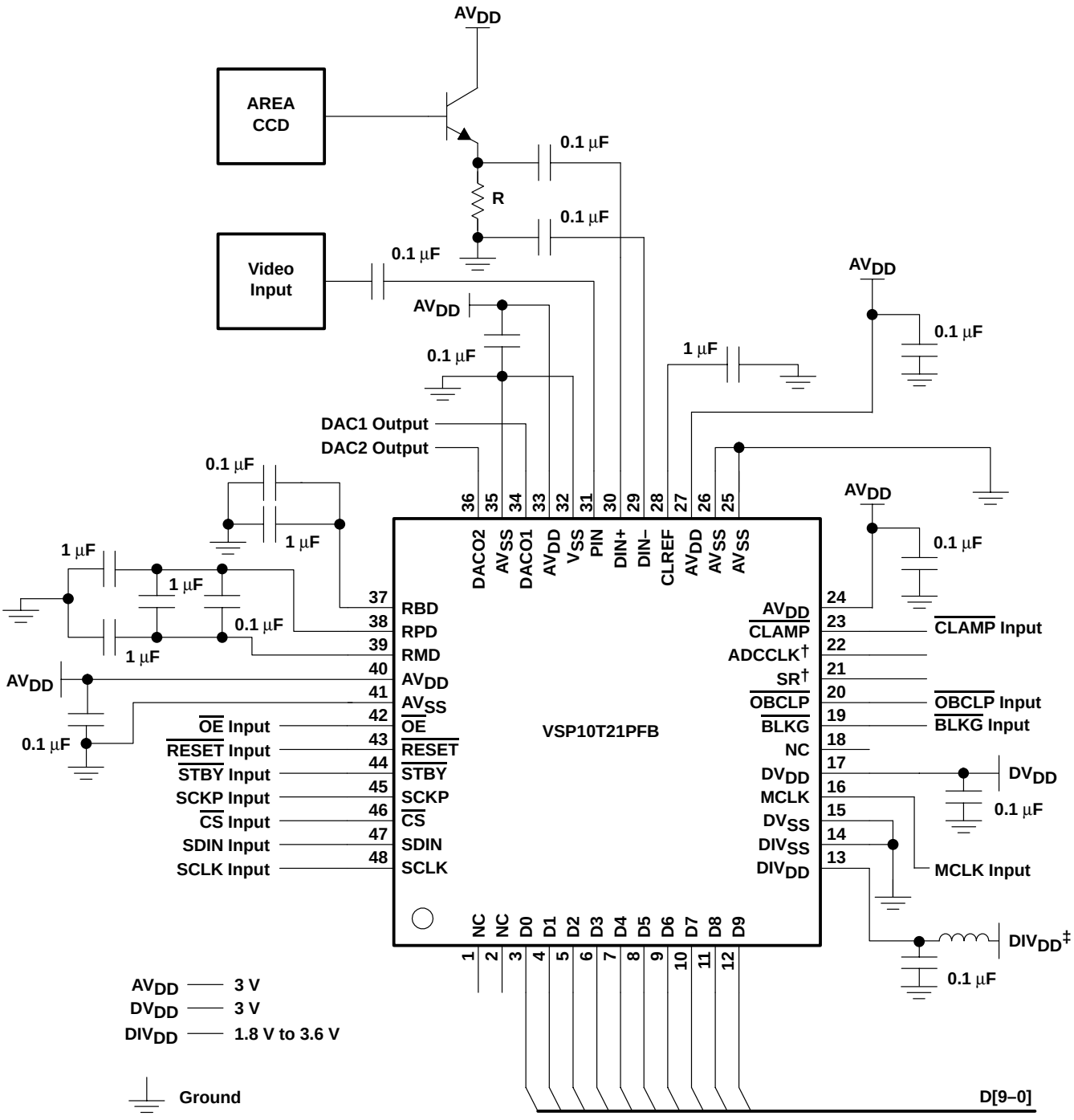
SCKP Terminal is Pulled Low



SCKP Terminal is Pulled High

Figure 3. Serial Interface Timing Diagram

APPLICATION INFORMATION



† ADCCLK and SR are test outputs only.
‡ DIV_{DD} is recommended to have a ferrite bead to filter the power transients.
NOTE: All analog outputs should be buffered if the load is resistive or if the load is capacitive with more than 2 pF loading. The decoupling capacitors for the power supplies must be placed as close as possible to these terminals.

Figure 4. Typical Application Connection

REGISTER DEFINITION

serial input data format

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
X	X	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A3	A2	A1	A0	
0	0	0	0	Control register
0	0	0	1	PGA gain register
0	0	1	0	User DAC1 register
0	0	1	1	User DAC2 register
0	1	0	0	Reserved
0	1	0	1	Optical black Vb setup register
0	1	1	0	Video control register
0	1	1	1	Reserved
1	0	0	0	SR and ADC delay register
1	0	0	1	Clock control register

D9–D10

10-bit data to be written into the selected register

control register format (00H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STBY	PDD1	PDD2	DACD	x	x	x	x	x	RTSY

control register description

BIT	NAME	DESCRIPTION
D9	STBY	Device power down control 1 = Standby 0 = Active (default)
D8	PDD1	Power down the user DAC1 1 = Standby 0 = Active (default)
D7	PDD2	Power down the user DAC2 1 = Standby 0 = Active (default)
D6	DACD	Sustain the user DACs when power down 0 = User DACs are powered down during global power-down (default) 1 = User DACs are not powered down during global power-down
D5	x	Reserved
D4	x	Reserved
D3	x	Reserved
D2	x	Reserved
D1	x	Reserved
D0	RTSY	Writing a 1 to this bit will reset entire system to the default settings (active high).

Default = 00 0000 0000

REGISTER DEFINITION

PGA register format (01H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Default PGA gain = 00 0000 0000 or 0 dB

The gain code range for CCD mode is from 0–767, which covers from 0 to 36 dB with 0.047 dB per step. Users must use this code range. The gain stays at 36 dB when the code is from 768–1023. For the video mode, the gain code range is from 256–512, which covers from 0 to 12 dB with 0.047 dB per step. Users must use a 256–512 code range for the video mode. In video mode, the gain range is from 12 dB to 24 dB for the gain code range of 513 to 767; however, the offset might be too large for this gain range.

user DAC1 and DAC2 registers format (02H and 03H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Default user DAC register value = 00 0000 0000

The DAC1 and DAC2 codes are from 0 to 255, which cover the output voltages at DACO1 and DACO2 output terminals from 0 to AV_{DD} with linear correspondence.

optical black Vb setup register format (05H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	NOB	VB3	VB2	VB1	VB0

optical black Vb setup register description

BIT	NAME	DESCRIPTION
D9–D5	X	Reserved
D4	NOB	This bit controls the OB output 0 = OB output has no affect by the Vb setting, and it is always 0 (default) 1 = OB output corresponds to the Vb setting.
D3–D0	VB3–VB0	**VB3 VB2 VB1 VB0 OB output** 0 0 0 0 20 LSB (default) 0 0 0 1 21 ⋮ 1 1 1 1 35

Default optical black Vb setup register value = 00 0000 0000

If NOB (D4) is set to 0, VB3–VB0 (D3–D0) has no effect. The output OB is 0.
If NOB is set to 1, the output OB is defined by VB3–VB0 from 20 LSB to 35 LSB, typically.

REGISTER DEFINITION

video control register (06H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	MOD	X

video control register description

BIT	NAME	DESCRIPTION
D9–D2	X	Reserved
D1	MOD	This bit defines the mode of the input 0 = CCD mode (default) 1 = Video mode
D0	X	Reserved. Always program this bit to 0.

Default register value= 00 0000 0000

SR and ADCCLK internal delay register format (08H)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCL4	ADCL3	ADCL2	ADCL1	ADCL0	SRL4	SRL3	SRL2	SRL1	SRL0

SR and ADCCLK internal delay register description

BIT	NAME	DESCRIPTION
D9–D5	ADCL4–ADCL0	These five bits set the internal ADCCLK delay. T is the period of the MCLK.

ADCL4	ADCL3	ADCL2	ADCL1	ADCL0	Typical internal delay
0	0	0	0	0	0
0	0	0	0	1	T/30
		:			
0	0	1	1	1	7T/30 (default)
		:			
1	1	1	0	1	29T/30

D4–D0	SRL4–SRL0	These five bits set the internal SR delay. T is the period of the MCLK.

SRL4	SRL3	SRL2	SRL1	SRL0	Typical internal delay
0	0	0	0	0	0
0	0	0	0	1	T/30
		:			
0	1	0	0	1	9T/30 (default)
		:			
1	1	1	0	1	29T/30

Default register value= 0 01110 1001
NOTE: Do not program SR and ADCCLK internal delays above 29T/30.

REGISTER DEFINITION

clock control register format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	ROEN	ADEN	CKIP	SRW1	SRW0

clock control register description

BIT	NAME	DESCRIPTION
D9–D5†	X	Reserved
D4	ROEN	This bit controls the SR output 1 = Disables SR output (default) 0 = Enables SR output
D3	ADEN	This bit controls the ADCCLK output 1 = Disables ADCCLK output (default) 0 = Enables ADCCLK output
D2	CKIP‡	This bit controls the input clock (MCLK) polarity 1 = Falling edge of the MCLK latches the ADC output 0 = Rising edge of the MCLK latches the ADC output (default)
D1–D0	SRW1, SRW0	These bits control the width of the SR pulse **SRW1 SRW0 Typical width** 0 0 4T/20 0 1 5T/20 (default) 1 0 6T/20 1 1 7T/20

Default register value= 00 00111001

† Bit D5 is recommended to be set to 1.

‡ This bit controls the polarity of the MCLK inside the VSP10T21 device which latches the ADC data output. Corresponding with this change, the user needs to read the data with different edge of the MCLK. By switching this bit from 0 to 1 also introduces an additional half pixel clock cycle delay.

PRINCIPLES OF OPERATION

CDS/PGA signal processor

In a CCD imaging system, the output from the CCD sensor is first fed to the CDS of the VSP10T21 device. The CCD signal is sampled and held during the reset reference interval and the video signal interval. By subtracting two resulting voltage levels, the CDS removes low frequency noise from the output of the CCD sensor and obtains the voltage difference between the CCD reference level and the video level of each pixel. Only the MCLK is required to feed into the AFE. Two clocks are generated internally based on the MCLK to perform the CDS function. One is SR for sampling the reference level of the CCD signal. The other clock is ADCCLK which samples the video level of the CCD signal on the falling edge. The ADCCLK is also used for the A/D conversion. These two clocks are output on the pad for the verification purpose. The user must not use these two terminals to drive any circuits. The digital ADC outputs are internally latched out by MCLK.

The CCD output is capacitively coupled to the VSP10T21 input. The $\overline{\text{CLAMP}}$ input clamps the ac-coupling capacitor to establish proper dc bias during the dummy pixel interval. The bias at the input to the VSP10T21 device is set to 1.2 V. Normally, the $\overline{\text{CLAMP}}$ is applied at sensor's line rate. A capacitor, with a value 10 times larger than that of the input ac-coupling capacitor, must be connected between terminals 28 (CLREF) and 25 (AV_{SS}).

The signal is sent to the PGA after the CDS function is complete. The PGA gain can be adjusted from 0 dB to 36 dB by programming the internal gain register via the serial port. The PGA is digitally controlled with 10-bit resolution on a linear dB scale, resulting a 0.047 dB gain step. The gain can be expressed by the following equation:

$$\text{Gain} = \text{PGA code} \times 0.047 \text{ dB}$$

where PGA code has a range of 0 to 767.

For example, if PGA code = 128, then the PGA Gain = 6 dB (or gain of 2).

In CCD mode, users must use the 0 to 767 range for PGA gain code. The gain stays at 36 dB when the code is from 768 to 1023.

video mode operation

The VSP10T21 device also provides an analog video-processing channel that consists of an input clamp, a PGA, and an ADC. Setting the MOD bit to 1 in video control register enables the video channel. The video signal must be connected to terminal 31 (PIN) via a 0.1-µF capacitor as shown in Figure 4.

The video clamp circuit automatically clamps the lowest level of the video input signal, which is usually the sync tip, to around 60 LSB.

The PGA gain in the video mode can be adjusted from 0 to 12 dB by programming the internal gain register via the serial port. The PGA is digitally controlled with 10-bit resolution on a linear dB scale, resulting a 0.047 dB gain step. The gain can be expressed by the following equation:

$$\text{Gain} = (\text{PGA code} - 256) \times 0.047 \text{ dB}$$

where PGA code has a range of 256 to 512.

For the video mode, users must use the 256 to 512 range for the PGA gain code. The gain code 0–255 must not be used, and the gain range is from 12 dB to 24 dB for the gain code range of 513 to 767; however, the offset might be too large for this gain range.

PRINCIPLES OF OPERATION

internal timing

As previously explained, the SR and ADCCLK clocks are required to operate the CDS. Users need to synchronize the SR and ADCCLK clocks with the CCD signal waveform. The output from the ADC is read out to external circuitry by the MCLK signal that is the external signal used to generate the SR and ADCCLK clocks internally. The user can use the SR and ADCCLK internal delay register to program the delay of these clocks based on Figure 2 in order to achieve the optimal performance. Terminals 21 (SR) and 22 (ADCCLK) are used to monitor these two internal signals. By changing bit D2 (CKIP) in the clock control register, the AFE digital output is latched at either the rising edge or the falling edge of the MCLK pulse.

The $\overline{\text{CLAMP}}$ signal activates the clamping circuit for the input signal. The $\overline{\text{OBCLP}}$ signal activates the optical black calibration and the active portion (the low pulse) of this signal must be within the optical black period of the CCD (see Figure 1).

ADC

The ADC employs a pipelined architecture to achieve high throughput and low power consumption. Fully differential implementation and digital error correction ensure 10-bit resolution.

The latency of the ADC data output is the default 5 MCLK cycles as shown in Figure 2. Pulling terminal 42 ($\overline{\text{OE}}$) high puts the ADC output in high impedance.

automatic optical black calibration

In the VSP10T21 device, the optical black and the system channel offset corrections are performed by an auto analog feedback loop. During the optical black calibration interval ($\overline{\text{OBCLP}}$ = low) of each line, the optical black pixels plus the channel offset are sampled and compared with the desired black level specified in the optical black Vb setup register. The difference is then integrated and added to incoming pixel data at PGA input. This analog feedback loop calibrates the PGA output to the desired black pixel level, which can be programmed either to 0 or from 20 LSB to 35 LSB at 1 LSB/step resolution typically via the serial port. The OB calibration settles within about 1000 OB pixels.

input blanking function

During blanking period of CCD operation, large input transients may occur at the VSP10T21 device's input, making the ADC output unpredictable. Activating $\overline{\text{BLKG}}$ pulse during this period ensures the digital code is zero at the ADC output.

user DACs

The VSP10T21 device includes two user DACs that can be used for external analog settings. These are resistor string DACs. They must be used only to drive capacitor or buffer loads, not resistor loads. The output voltage of each DAC can be independently set and has a range of 0 V to the supply voltage with 8-bit resolution. When the user DACs are not used in a camera system, they can be put in the standby mode by programming control bits in the control register 1. The status of the user DACs is defined in the following table.

PRINCIPLES OF OPERATION

SOFTWARE/HARDWARE GLOBAL STANDBY	PDD1/PDD2	DACD	STATUS OF DAC1/DAC2
Active	0	x	Active
Active	1	x	Standby
Standby	0	0	Standby
Standby	0	1	Active
Standby	1	x	Standby

NOTE: The hardware global standby is set by pulling down terminal 44 ($\overline{\text{STBY}}$) of the VSP10T21 device. The software global standby is controlled by setting bit D9 (STBY) in the control register to 1.

3-wire serial interface

A simple 3-wire (terminals 48 (SCLK), 47 (SDIN), and 46 ($\overline{\text{CS}}$)) serial interface is provided to allow writing to the internal registers of the VSP10T21 device. The serial clock SCLK can be run at a maximum speed of 40 MHz. The serial data SDIN is 16 bits long. After two leading null bits, there are four address bits for which internal register is to be updated, the following 10 bits are the data to be written to the register. To enable the serial port, $\overline{\text{CS}}$ must be held low. The data transfer is initiated by the incoming SCLK after $\overline{\text{CS}}$ falls. Figure 3 shows the detailed timing for the serial interface.

The SCLK polarity is selectable by pulling terminal 45 (SCKP) either high or low.

device reset

The device is not under the default configuration when powered on. The registers are set to the default value by a reset. When terminal 43 ($\overline{\text{RESET}}$) is pulled low, all internal registers are set to their default values. In addition, the VSP10T21 device has a software-reset function that resets the device when writing to a control bit in the control register.

See *REGISTER DEFINITION* for the register default values.

power-down mode (standby)

The VSP10T21 device implements both hardware and software power-down modes. Pulling terminal 44 ($\overline{\text{STBY}}$) low puts the device in the low-power standby mode. The total power drops to about 1.5 mW. Setting bit D9 (STBY) in the control register can also activate the power-down mode. Users can still program all internal registers during the power-down mode.

power supply

The VSP10T21 device has several power supply terminals. Each major internal analog block has a dedicated AV_{DD} supply terminal. All internal digital circuitry is powered by the DV_{DD}. Both AV_{DD} and DV_{DD} are 3 V nominal.

The DIV_{DD} and DIV_{SS} terminals supply power to the output digital driver (D9–D0). The DIV_{DD} is independent of the DV_{DD} and can be operated from 1.8 V to 3.6 V. This allows the outputs to interface with digital ASICs requiring different supply voltages.

PRINCIPLES OF OPERATION

grounding and decoupling

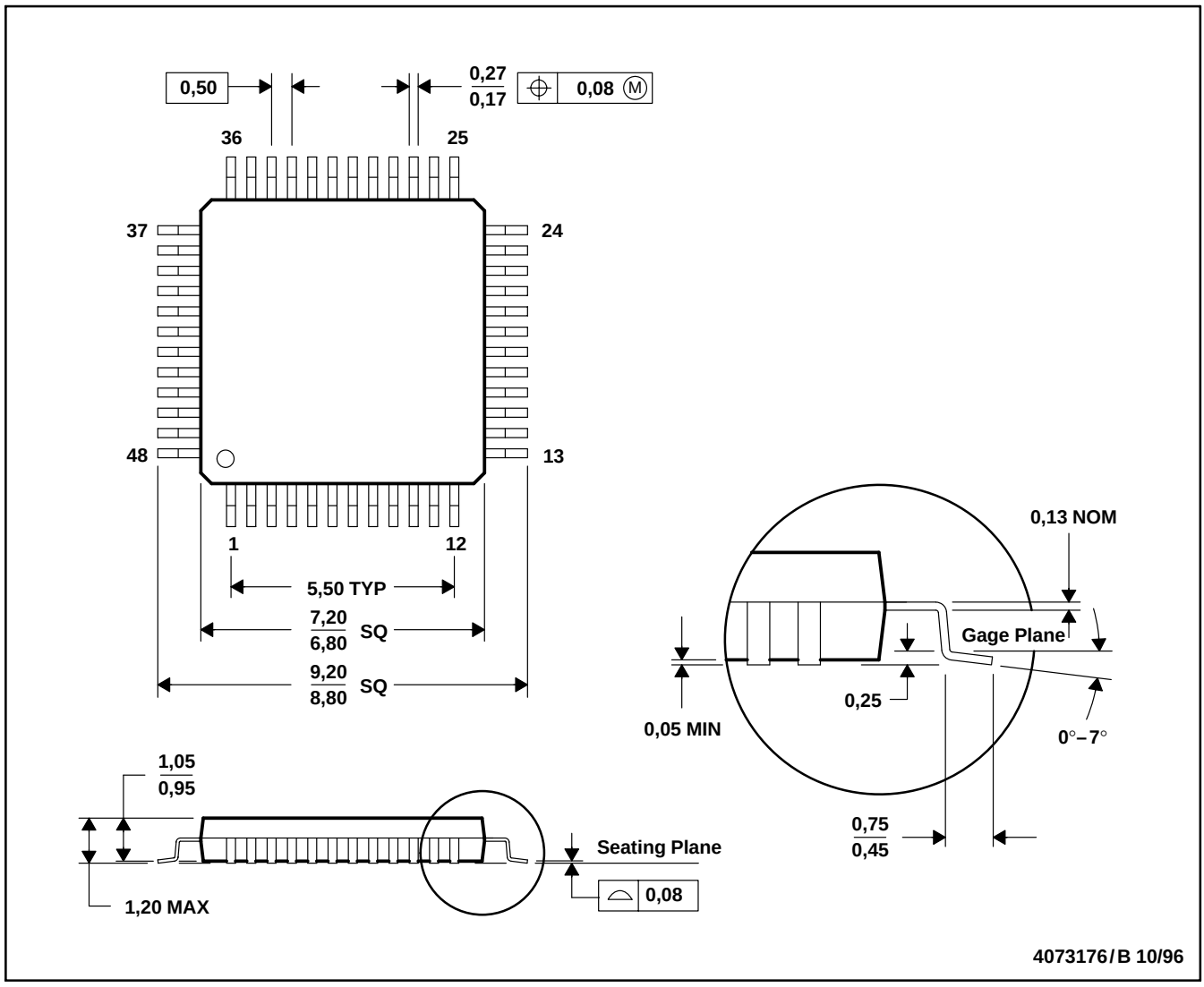
General practices must apply to the printed-circuit board (PCB) design to limit high frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference terminals be sufficiently bypassed. In the case of power supply decoupling, 0.1-μF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Recommended external decoupling for the three voltage reference terminals is shown in Figure 4. Since the effectiveness of the decoupling capacitors depends largely on the proximity to the individual supply terminal, all decoupling capacitors must be placed as close as possible to the supply terminals. An inductor is recommended for the DIV_{DD} power supply (see Figure 4). Common ground is also recommended.

voltage references

An internal precision voltage reference of 1.5 V nominal is provided. This reference voltage generates the ADC Ref– voltage of 1 V and Ref+ of 2 V. It also sets the clamp voltage. All internally generated voltages are fixed values and cannot be adjusted. Terminals 37 (RBD), 38 (RPD), and 39 (RMD) must not be used to drive any loads.

MECHANICAL DATA

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
VSP10T21PFB	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
VSP10T21PFBG4	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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