Burr-Brown Products from Texas Instruments

AFE1302

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ADSL ANALOG FRONT-END

FEATURES

- NOISE FLOOR: –144dBm/Hz
- MULTIRATE COMPATIBLE
- VCXO CIRCUITRY AND DAC
- 8.8M TO 1.1MWords/s WORD RATE
- FIVE GENERAL-PURPOSE OUTPUTS
- 570mW POWER DISSIPATION
- TQFP-48 PACKAGE

DESCRIPTION

Burr-Brown's Analog Front-End from Texas Instruments reduces the size and cost of an ADSL-compliant system by providing the active analog circuitry needed to connect an ADSL Digital Signal Processor (DSP) to an external line driver, receiver, TX/RX filters, hybrid, transformer, and POTS filter. The AFE1302 is designed for downstream data rates of 4Mbps and higher, and operation at a clock rate of 35.328MHz, with an output word rate of up to 8.832MWords/s.

Functionally, this unit consists of a transmit (TX) channel, a receive (RX) channel, a VCXO (Voltage Controlled Crystal Oscillator) control Digital-to-Analog Converter (DAC), and VCXO active circuitry. The TX section converts, filters, and buffers outgoing Discrete Multi Tone (DMT) data from the ADSL DSP. The receive section amplifies, filters, and digitizes the DMT data received on the twisted pair line.

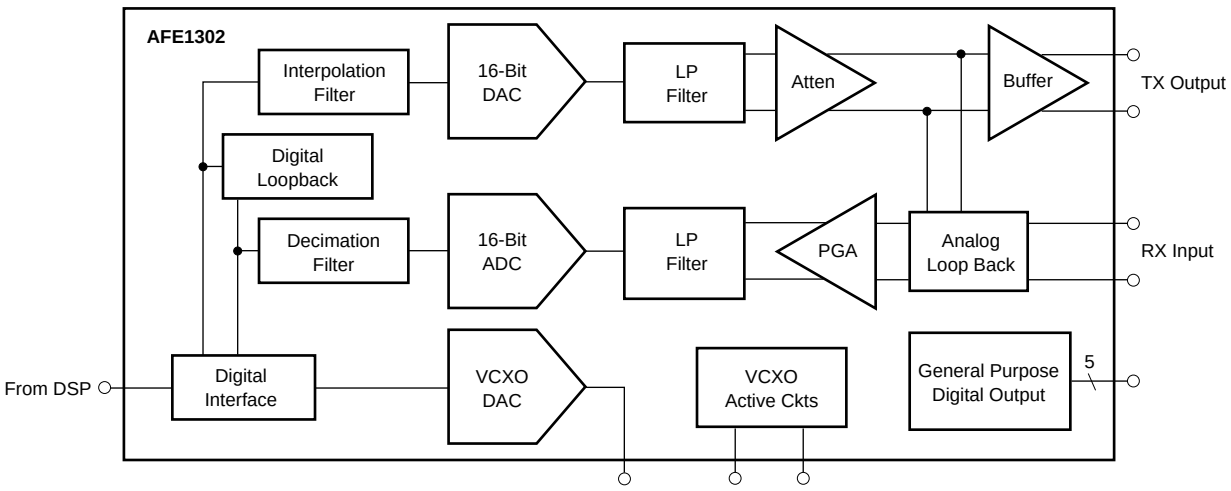
This IC operates on a single 5V supply. The digital circuitry in the unit can be connected to a supply voltage ranging from 3.3V to 5V. The chip uses only 570mW.

The AFE1302 is designed to be used with external amplifiers and filters for noise reduction and dynamic-range improvement.

The RX channel consists of a low-noise PGA, a switched capacitor low-pass filter, and fourth-order delta-sigma Analog-to-Digital Converter (ADC). The delta-sigma modulator operating at a 32X oversampling ratio produces a 16-bit output at word rates up to 8832kHz.

The TX channel consists of a fourth-order delta-sigma DAC, switched-capacitor low-pass filter, programmable attenuator, and buffer. The buffer drives off-chip into a low-noise line driver configured as a 3-pole active filter to produce an overall low-noise high-drive TX output signal on a twisted pair line.

Patents Pending



TEXAS INSTRUMENTS

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SPECIFICATIONS

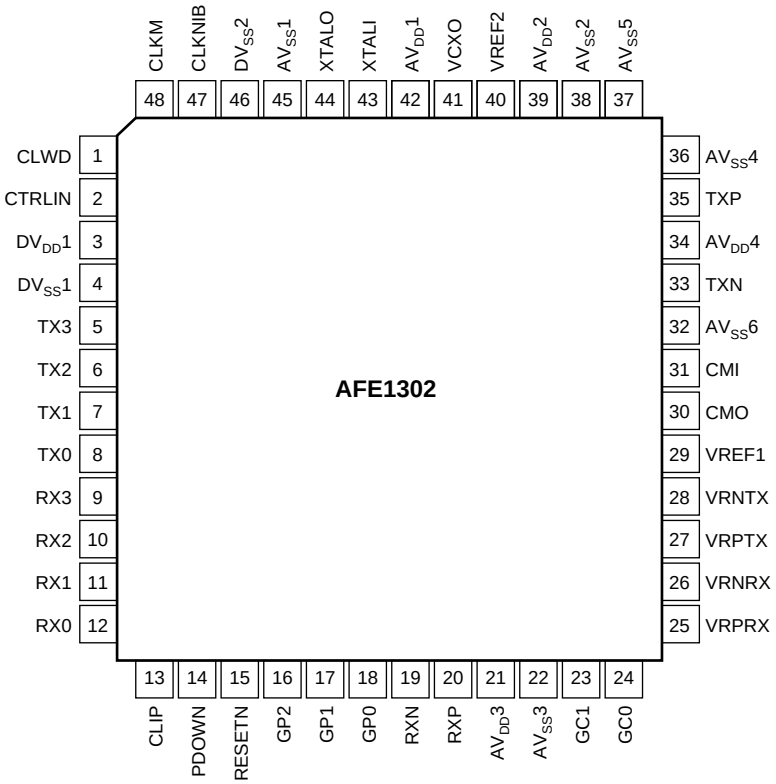
Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, f_{CLK} = 35.328MHz, TX output and RX input measured differentially, unless otherwise specified.

PARAMETER	CONDITIONS	AFE1302Y MIN	AFE1302Y TYP	AFE1302Y MAX	UNITS
RECEIVE CHANNEL					
Input Signal (CMV = AV_{DD}/2)	Differential, G = –6dB	9.0	9.6		Vp-p
Common-Mode Voltage			AV_{DD}/2		V
Input Impedance	Pin-to-AV_{DD}		2.8		kΩ
Input Capacitance			30		pF
Programmable Amplifier Range		–6		40	dB
Gain Step Size	Monotonicity Guaranteed		1		dB
Input Noise	PGA = +40dB(1)		–148	–144	dBm/Hz
Output Word Rate		1.104		8.832	MWords/s
Output Word Resolution	(15 Bits + 1 Sign Bit) or (14 Bits + 2 Sign Bits)			16	Bits
ADC Sampling Rate		35.328			MSamples/s
Low-Pass Frequency Corner	One Pole Analog Filter		1.1		MHz
Passband Droop	At 550kHz		1		dB
SINAD	PGA Gain = 40dB, Input Referred		100		dB
	PGA Gain = 0dB	68			dB
THD	Single Tone, PGA = 0dB	75	84		dB
MTPR (MultiTone Power Ratio)			75		dB
TRANSMIT CHANNEL					
Input Word Rate		1.104		8.832	MWords/s
Input Word Resolution	(15 Bits + 1 Sign Bit) or (14 Bits + 2 Sign Bits)			16	Bits
Peak Signal Amplitude	Differential, G = 0dB	4.4	4.8		Vp-p
Common-Mode Voltage			AV_{DD}/2		
Load Resistance	Differential		400		Ω
Load Capacitance	Differential		10		pF
Programmable Attenuator Range		–31		0	dB
Attenuator Step Size	Monotonicity Guaranteed		1.0		dB
Attenuator Step Accuracy			0.5		dB
Low-Pass Filter Corner Frequency	Fourth-Order, 0.1dB Programmable		127		kHz
Passband Ripple			–0.1		dB
Group Delay Variation				10	µs
Output Noise	Measured at 50kHz		–110		dBm/Hz
	Measured at 200kHz		–116		dBm/Hz
THD Distortion	FS Output 0dB		65		dBc
	FS Output –6dB		73		dBc
SFDR in RX Band (20 Tone Test)	See Note (2)		–98		dBVrms
MTPR			70		dB
VCXO WITH EXTERNAL CIRCUITRY	Sensitive to PCB Layout				
Frequency			35.328		MHz
Tuning Range			±100		ppm
DAC Resolution	Monotonicity Guaranteed		10		Bits
DIGITAL INTERFACE					
Logic Levels					
V_{IH}	$\|I_{IH}\|$ < 10µA	DV_{DD} – 1	DV_{DD}	DV_{DD} + 0.3	V
V_{IL}	$\|I_{IL}\|$ < 10µA	–0.3	0	0.8	V
V_{OH}	I_{OH} = –20µA	DV_{DD} – 0.5			V
V_{OL}	I_{OL} = 20µA			0.4	V
CONTROL INTERFACE (GC0, GC1, GP0, GP1, GP2)					
Logic Levels					
V_{OH}	I_{OH} = 1mA	DV_{DD} – 0.5			V
V_{OL}	I_{OL} = 1mA			0.4	V
POWER					
Analog Power Supply Voltage	AV_{DD}	4.75	5	5.25	V
Analog Dissipated Power			470		mW
Digital Power Supply Voltage	DV_{DD}	3.0	3.3	5.5	V
Digital Dissipated Power	V_{DD} = 3.3V		100		mW
TEMPERATURE RANGE					
Operation		0		70	°C
Thermal Resistance, θ_{JA}			56.5		°C/W

NOTES: (1) With TX in operation, no RX data, referred to 100Ω. (2) With TX reverb multitone signal (25.875kHz to 138kHz at a 4.3125kHz step), measured signal level beyond 150kHz at TXP, TXN.

PIN CONFIGURATION

Top View **TQFP**



ABSOLUTE MAXIMUM RATINGS

Analog Inputs: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	AGND –0.3V to AV_{DD} +0.3V
Analog Outputs Short Circuit to Ground (+25°C)	Continuous
AV_{DD} to AGND	–0.3V to 6V
DV_{DD} to DGND	–0.3V to 6V
Digital Input Voltage to DGND	–0.3V to DV_{DD} +0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} +0.3V
AGND, DGND, Differential Voltage	0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 3s)	+260°C
Power Dissipation	700mW

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
AFE1302Y	TQFP-48	355	0°C to +70°C	AFE1302Y	AFE1302Y/250	Tape and Reel
"	"	"	"	"	AFE1302Y/2K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of “AFE1302Y/2K” will get a single 2000-piece Tape and Reel.

PIN DESCRIPTIONS

Number	Type	Pin Name	Description	External Connection
Analog Interface				
23	Output	GC0	External Gain Control Output LSB	Optional Swap Amp
24	Output	GC1	External Gain Control Output MSB	Optional Swap Amp
19	Input	RXN	Analog Receive Negative Input	Line Interface
20	Input	RXP	Analog Receive Positive Input	Line Interface
25	Output	VRPRX	RX Reference Positive Output	0.1uF,1µF to $AV_{SS}3$
26	Output	VRNRX	RX Reference Negative Output	0.1uF,1µF to $AV_{SS}3$
30	Output	CMO	Output Common-Mode voltage	0.1uF,1µF to $AV_{SS}3$
27	Output	VRPTX	TX Reference Positive Output	0.1uF,1µF to $AV_{SS}3$
28	Output	VRNTX	TX Reference Negative Output	0.1uF,1µF to $AV_{SS}3$
29	Output	VREF1	Unbuffered Bandgap Reference	0.1uF,1µF to $AV_{SS}3$
31	Output	CMI	Unbuffered Common-Mode Voltage	0.1uF,1µF to $AV_{SS}3$
35	Output	TXP	TX Positive Output	Line Interface
33	Output	TXN	TX Negative Output	Line Interface
40	Output	VREF2	DAC Reference Voltage	XTAL Interface
41	Output	VCXO	VXCO Control Voltage DAC Output	XTAL Interface
43	—	XTALI	XTAL Oscillator Input	XTAL
44	—	XTALO	XTAL Oscillator Output	XTAL
Digital Interface				
48	Output	CLKM	Master Clock Output, f = 35.328MHz	DSP
47	Output	CLKNIB	Nibble Clock Output	DSP
1	Output	CLWD	Word Clock Output	DSP
2	Input	CTRLIN	Serial Data Input	DSP
5	Input	TX3	Digital Transmit Input	DSP
6	Input	TX2	Digital Transmit Input	DSP
7	Input	TX1	Digital Transmit Input	DSP
8	Input	TX0	Digital Transmit Input	DSP
9	Output	RX3	Digital Receive Output	DSP
10	Output	RX2	Digital Receive Output	DSP
11	Output	RX1	Digital Receive Output	DSP
12	Output	RX0	Digital Receive Output	DSP
13	Output	CLIP	Clipping Detection Output	DSP
14	Input	PDOWN	Power-Down Select, “1” = Power Down	DSP
15	Input	RESETN	Reset Pin (Active LOW)	DSP
16	Output	GP2	General-Purpose Output 2	—
17	Output	GP1	General-Purpose Output 1	—
18	Output	GP0	General-Purpose Output 0	—
Supply voltages				
46	—	$DV_{SS}2$	Digital Ground 2	DGND Plane
3	3V or 5V	$DV_{DD}1$	Digital Power	0.1uF,1µF to $DV_{SS}1$
4	—	$DV_{SS}1$	Digital Ground 1	DGND Plane
21	5V	$AV_{DD}3$	Analog Power (Main)	0.1uF,1µF to $AV_{SS}3$
22	—	$AV_{SS}3$	Analog Ground (Main)	AGND Plane
32	—	$AV_{SS}6$	Analog Ground for TX Output	AGND Plane
34	5V	$AV_{DD}4$	Analog Power for TX Output	0.1uF,1µF to $AV_{SS}4$
36	—	$AV_{SS}4$	Analog Ground for TX Output	AGND Plane
37	—	$AV_{SS}5$	Analog Clock Ground	AGND Plane
38	—	$AV_{SS}2$	Analog Clock Ground	AGND Plane
39	5V	$AV_{DD}2$	Analog Clock Power	0.1uF,1µF to $AV_{SS}2$
42	5V	$AV_{DD}1$	XTAL Power	0.1uF,1µF to $AV_{SS}1$
45	—	$AV_{SS}1$	XTAL Ground	AGND Plane

THEORY OF OPERATION

The AFE1302 consists of a transmit (TX) channel, a receive (RX) channel, and a digital interface to connect to an ADSL DSP. In addition, VCXO circuitry and a VCXO control DAC are included for precise clock generation.

The TX channel receives digital data at the nominal rate of 1.104MWords/s to 8.832MWords/s. These TX data words are interpolated up to the AFE1302 clock rate of 35.328MHz. The data is converted to analog form with a 16-bit delta-sigma DAC and bandwidth limited with a fourth-order, switched-capacitor low-pass filter. The filter output is buffered and drives off-chip to an external Burr-Brown line-driver circuit from Texas Instruments. This line driver is configured as an LC passive filter to provide additional out-of-band noise and distortion attenuation (see System section). Transmit power can be reduced with a combination of digital and analog attenuation to ensure compliance with the G.992.2 “politeness” rule.

In the RX channel, the analog receive signal is input to a PGA. The output of the first-order, switched capacitor filter is digitized with a 16-bit delta-sigma ADC. A decimation filter ensures a compliant word rate (1.104MWords/s to 8.832MWords/s) to the ADSL digital chip.

Precise phase alignment is required to ensure proper operation of the ADSL modem. The active circuitry required to create a VCXO is included on the AFE1302. This includes the gain element as well as a 10-bit, monotonic DAC. The only external components required are a varactor, load capacitor, and crystal.

TX DISTORTION AND NOISE REQUIREMENTS

The TX output is a DMT signal generated by the AFE1302. This output contains the desired DMT signal in the TX frequency band as well as unwanted noise and distortion in both the TX and RX frequency bands. The inband TX distortion and noise is specified by the MultiTone Power Ratio (MTPR) test. Since MTPR is better than 70 dB, full-rate ADSL performance is guaranteed for TX upstream signals.

However, TX distortion and noise can also limit downstream RX performance. TX noise and distortion can degrade RX signal quality since the TX output is connected to the RX input through filters, line driver, and hybrid. Three tests show out-of-band TX performance as used in the ADSL system. Total harmonic distortion (THD) shows the overall linearity of the TX signals. The next test uses a typical ADSL DMT TX signal and measures the largest distortion tone in the RX band. The largest distortion tone in the RX band is –98 dBVrms or –124 dBm/Hz as measured in a 4.3125 kHz bandwidth. In the last test, TX noise is measured by transmitting no signal. Noise as shaped by the TX filter is lower than –116dBm/Hz in the RX band.

To insure that TX distortion and noise do not degrade the RX downstream performance, external filtering and trans-hybrid loss of greater than 30dB is required. Refer to Figure 6 for an external circuit and contract TI for a detailed reference design document.

DIGITAL DATA TRANSMISSION

Data is transmitted to the AFE1302 from the DSP on the TX[0:3] lines, as shown in Figure 1. The Data TX[0:3] changes during the rising edge of CLKM within the DSP, and the Data are valid on the falling edge of CLKM for the AFE to read. The minimum setup and hold time are 5ns (see Figure 2); the start of a new sample is indicated by CLWD being HIGH.

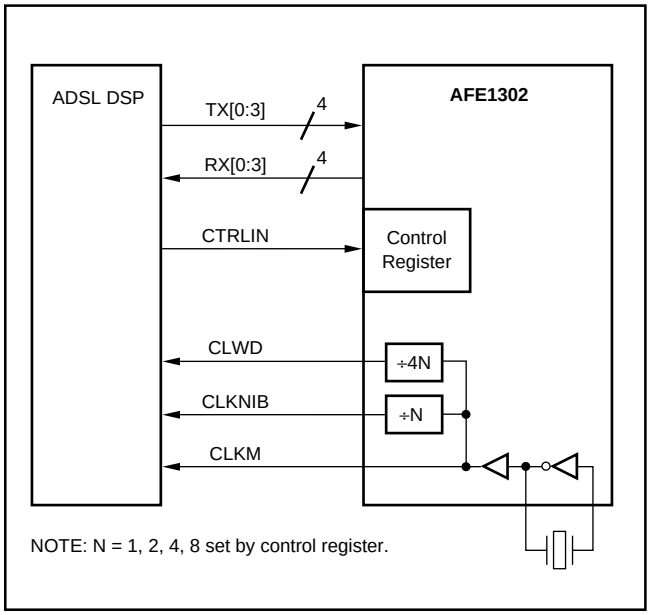


FIGURE 1. AFE1302/DSP Interface.

Data is transmitted to the DSP from the AFE1302 on the RX[0:3] lines, as shown in Figure 1. The Data RX[0:3] changes during the rising edge of CLKM within the AFE, and the Data are valid on the falling edge of CLKM for the DSP to read. The minimum setup and hold time are 5ns (see Figure 2); the start of a new sample is indicated by CLWD being HIGH.

During normal operation, a 16-bit TX data word is generated by the DSP. This TX data is sent from the DSP to the AFE via four serial lines TX[0:3]. Each serial line is clocked by CLKM at 35.328MHz or by CLKNIB at 35.328MHz divided by N. CLKNIB and CLWD can be changed by programming N via the control register.

The RX word output rate and TX word input rate can be changed by programming N in the control register for values of 1, 2, 4, or 8. For instance, setting N = 1 sets the TX and RX data word rate to 8.832Mwords/s.

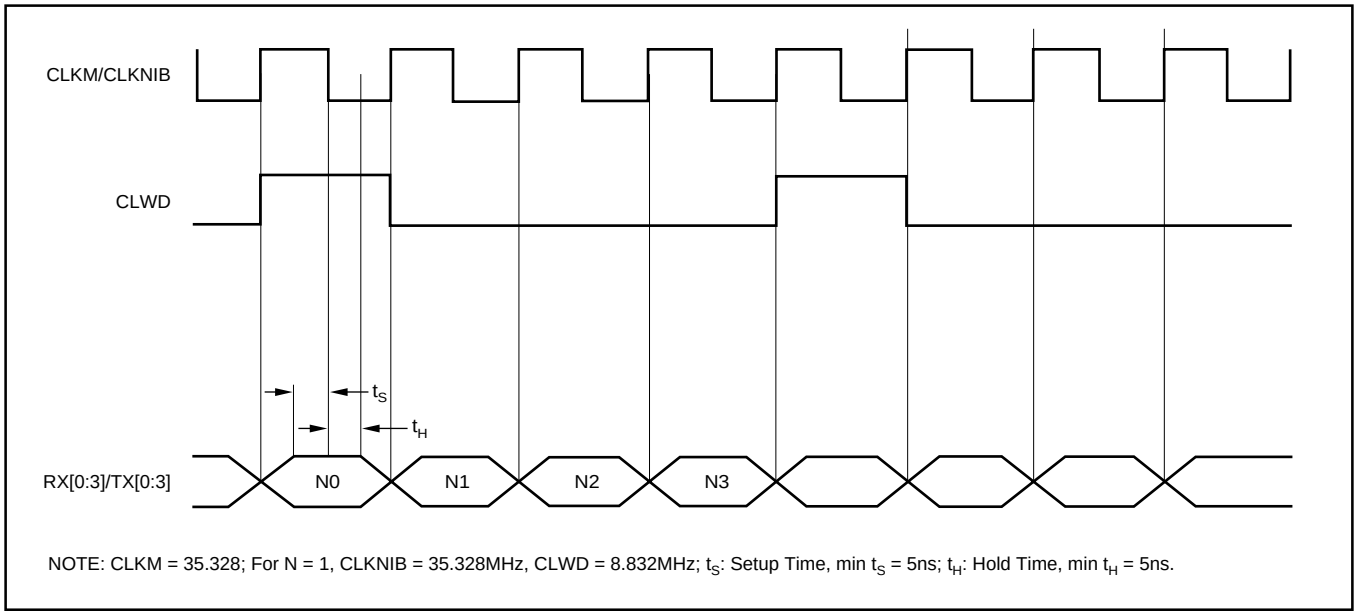


FIGURE 2. AFE1302 Transmit/Receive Timing Diagram.

TRANSMIT DATA

Transmit data TX[0:3] passed to the AFE1302 will be Binary Two's Complement with one or two sign bits depending on bit 9 in the AFE1302 control register at address 001 (see Table V). Bit 9 = 0 is two sign bits and bit 9 = 1 is one sign bit. Please refer to Tables I and II.

BIT MAP\NIBBLE	N0	N1	N2	N3
TX0	data bit 0 (LSB)	data bit 4	data bit 8	data bit 12
TX1	data bit 1	data bit 5	data bit 9	data bit 13
TX2	data bit 2	data bit 6	data bit 10	data sign
TX3	data bit 3	data bit 7	data bit 11	data sign

TABLE I. AFE1302 TX Data Format, Address 001, Bit 9 = 0.

This corresponds to the internal data structure as follows (sign bit is repeated):

INTERNAL DATA BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTERNAL DATA BIT	Sign	Sign	13	12	11	10	9	8	7	6	5	4	3	2	1	0

BIT MAP\NIBBLE	N0	N1	N2	N3
TX0	data bit 0 (LSB)	data bit 4	data bit 8	data bit 12
TX1	data bit 1	data bit 5	data bit 9	data bit 13
TX2	data bit 2	data bit 6	data bit 10	data bit 14
TX3	data bit 3	data bit 7	data bit 11	data sign

TABLE II. AFE1302 TX Data Format, Address 001, Bit 9 = 1.

This corresponds to the internal data structure as follows:

INTERNAL DATA BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTERNAL DATA BIT	Sign	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

RECEIVE DATA

Data RX[0:3] received from the AFE1302 will be in the format shown in Tables III and IV:

BIT MAP\NIBBLE	N0	N1	N2	N3
RX0	data bit 0 (LSB)	data bit 4	data bit 8	data bit 12
RX1	data bit 1	data bit 5	data bit 9	data bit 13
RX2	data bit 2	data bit 6	data bit 10	data sign
RX3	data bit 3	data bit 7	data bit 11	data sign

TABLE III. AFE1302 RX Data Format, Address 001, Bit 9 = 0.

This corresponds to the internal data structure as follows (sign bit is repeated):

INTERNAL DATA BIT	Sign	Sign	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTERNAL DATA BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

BIT MAP\NIBBLE	N0	N1	N2	N3
RX0	data bit 0 (LSB)	data bit 4	data bit 8	data bit 12
RX1	data bit 1	data bit 5	data bit 9	data bit 13
RX2	data bit 2	data bit 6	data bit 10	data bit 14
RX3	data bit 3	data bit 7	data bit 11	data sign

TABLE IV. AFE1302 RX Data Format, Address 001, Bit 9 = 1.

This corresponds to the internal data structure as follows:

INTERNAL DATA BIT	Sign	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTERNAL DATA BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

CLIP EVENT

Receive data (AFEG_RX) is generated in the AFE1302 with additional headroom. For the one sign-bit case, if AFEG_RX data is greater than 7FFF, it will be clipped to 7FFF. If AFEG_RX data is less than 8000, it will be clipped to 8000. For the two sign-bit case, if AFEG_RX data is greater than 3FFF, it will be clipped to 3FFF. If AFEG_RX data is less than C000, it will be clipped to C000. During clip, pin CLIP will be asserted HIGH for monitoring purposes. Pin CLIP will remain HIGH until 0 is written to address = 010, bit 3 in AFE1302 control register.

PROGRAMMING THE AFE1302

The internal AFE control register, as shown in Table V, is used to set the programmable features of the AFE1302 and to set the VCXO frequency. Serial data is sent from the DSP to the AFE control register on the CTRLIN pin in 16-bit blocks. This data is clocked into the AFE1302 on the falling edge of CLWD. AFEREG data is valid when followed by at least 16 stop bits (HIGH). The timing is shown in Figure 3. During programming, all AFE1302 functions are active. Data ID code 0 through 5 must be configured for normal operation; data ID code 6 and 7 are reserved for future use.

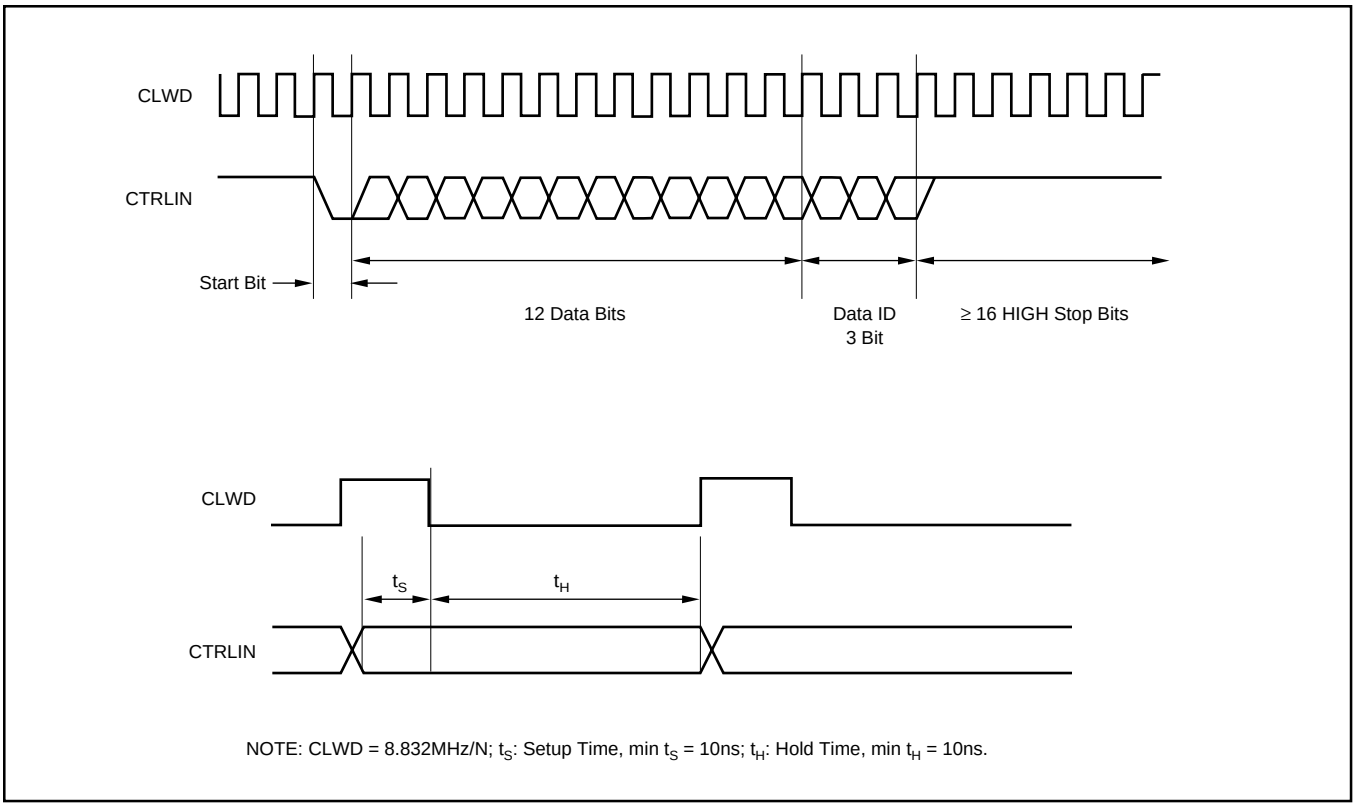


FIGURE 3. AFE1302 Program Timing.

START BIT	DATA BITS												DATA ID			
MSB															LSB	REGISTER DESCRIPTIONS
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	***RX REGISTER***
0	X												0	0	0	External Gain Control GC1 (1 Bit)
0		X											0	0	0	External Gain Control GC0 (1 Bit)
0			0	0	0	0	0	0					0	0	0	AGC RX Gain Setting –6dB (6 Bits)
0			0	0	0	0	0	1					0	0	0	AGC RX Gain Setting –5dB (6 Bits)
0			X	X	X	X	X	X					0	0	0	AGC RX Gain Setting X dB (6 Bits)
0			1	0	1	1	1	0					0	0	0	AGC RX Gain Setting 40dB (6 Bits)
0												X	0	0	0	X = 1, Filter Setting 1.1MWords/s; X = 0, Filter Setting 8.8MWords/s
0									0	0	0		0	0	0	Reserved, Must Be Set As Shown
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	***TX REGISTER***
0	0	0	0	0	0								0	0	1	Transmit Attenuator Setting = 0dB (5 Bits)
0	0	0	0	0	1								0	0	1	Transmit Attenuator Setting = –1dB (5 Bits)
0	X	X	X	X	X								0	0	1	Transmit Attenuator Setting = X dB (5 Bits)
0	1	1	1	1	1								0	0	1	Transmit Attenuator Setting = –31dB (5 Bits)
0										X			0	0	1	GP2 (General-Purpose Output 2)
0											X		0	0	1	GP1 (General-Purpose Output 1)
0												X	0	0	1	GP0 (General-Purpose Output 0)
0						X							0	0	1	X = 1, RX and TX Data Format Has 1 Sign Bit and 15 Data Bits X = 0, RX and TX Data Format Has 2 Sign Bits and 14 Data Bits
0							0	0	1				0	0	1	Reserved, Must Be Set As Shown
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	***AFE REGISTER***
0	X												0	1	0	Digital Loopback TX to RX Through Digital Section (1 Bit) X = 1, Loopback Mode; X = 0, Normal Operation Mode
0		X											0	1	0	Analog Loopback TX to RX Through Analog Section (1 Bit) X = 1, Loopback Mode; X = 0, Normal Operation Mode
0			X										0	1	0	X = 1, RX Enable Mode
0				X	X								0	1	0	Data Word Clock Divider (2 Bits)
0				0	0								0	1	0	Data Word Clock = 8.832MHz (2 Bits)
0				0	1								0	1	0	Data Word Clock = 4.416MHz (2 Bits)
0				1	0								0	1	0	Data Word Clock = 2.208MHz (2 Bits)
0				1	1								0	1	0	Data Word Clock = 1.104MHz (2 Bits)
0												X	0	1	0	Clear CLIP Signal: X = 1, RX is Clipping; X = 0, CLIP Cleared
0						0	0	1	0	0	1		0	1	0	Reserved, Must Be Set As Shown
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	***VCXO DAC VALUE REGISTER***
0	X	X	X	X	X	X	X	X	X	X			0	1	1	VCXO DAC Input Word (10 Bits)
0	0	0	0	0	0	0	0	0	0	0			0	1	1	VCXO DAC Input Word = 0 (10 Bits)
0	1	1	1	1	1	1	1	1	1	1			0	1	1	VCXO DAC Input Word = +FS (10 Bits)
0											0	0	0	1	1	Reserved, Must Be Set As Shown
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	***INTERFACE REGISTER***
0	X	X	X	X	X	X	X	X					1	0	0	Reserved
0									X				1	0	0	X = 0, TX[3:0] Should Be Latched On Falling CLKNIB X = 1, TX[3:0] Should Be Latched On Rising CLKNIB
0										X			1	0	0	X = 0, RX[3:0] Should Be Latched On Falling CLKNIB X = 1, RX[3:0] Should Be Latched On Rising CLKNIB
0											X		1	0	0	Digital Loopback RX Into TX: X = 1 Loopback Mode; X = 0 Normal Mode
0												0	1	0	0	Reserved, Must Be Set As Shown
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	***RESERVED***
0	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	Reserved, Must Be Set As Shown
0	X	X	X	X	X	X	X	X	X	X	X	X	1	1	0	Reserved, Data ID 6
0	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	Reserved, Data ID 7

NOTE: All registers are initially set to zero.

TABLE V. AFE1302 Control Register.

DIGITAL-TO-ANALOG CONVERTER

The Digital-to-Analog Converter (DAC) data for the TX channel is deserialized and written in four 4-bit registers and coded in two's complement, as shown in Table VI.

ANALOG I/O	DAC/ADC HEXDATA 1 SIGN BIT
Positive Full-Scale	7FFF
Mid-Scale	0000
Negative Full-Scale	8000

TABLE VI. One Sign Bit.

ANALOG-TO-DIGITAL CONVERTER

The Analog-to-Digital Converter (ADC) data from the RX channel is stored in four 4-bit registers and coded in two's complement, as shown in Table VII.

ANALOG I/O	DAC/ADC HEXDATA 2 SIGN BITS
Positive Full-Scale	3FFF
Mid-Scale	0000
Negative Full-Scale	C000

TABLE VII. Two Sign Bits.

SCALABLE TIMING

The AFE1302 scales operation with the clock frequency. All internal filters change frequency with the clock speed so that the unit can be used at different frequencies just by changing the clock speed.

For the RX channel, the digital filtering of the delta-sigma converter scales directly with the clock speed. For the TX channel, the power spectral density scales directly with the clock rate. The transformer and external filter need to be changed for different frequency requirements.

LAYOUT

The analog front-end of an ADSL system has a number of conflicting requirements. It must accept and deliver digital outputs at fairly high rates of speed, and convert the line input to a high precision (14-bit) digital output. Thus, there are two sections of the AFE1302: the digital section, and the analog section. The recommended VCXO circuit layout is shown in Figure 4.

DIGITAL LAYOUT

The power supply for the digital section of the AFE1302 can range from 3.3V to 5V. This supply should be decoupled to digital ground with a ceramic 0.1µF capacitor placed as close as possible to digital ground (DV_{SS}) and digital power (DV_{DD}). Ideally, both a digital power-supply plane and a digital ground plane should run to and underneath the digital pins of the AFE1302. However, DV_{DD} may be supplied by a wide printed circuit board trace. A digital ground plane underneath all digital pins is strongly recommended.

ANALOG LAYOUT

The remaining portion of the AFE1302 should be considered analog. Note that AV_{DD} must be in the 4.75V to 5.25V range. All AV_{SS} pins should be connected directly to a common analog ground plane and all AV_{DD} pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to the power supply. The analog power-supply pins should be decoupled to analog ground with both a 10µF tantalum capacitor and a 0.1µF ceramic capacitor. The ceramic capacitors should be placed as close to the AFE1302 as possible. The placement of the tantalum capacitor is not as critical, but should be close to the pin. In each case, the capacitor should be connected between AV_{DD} and AV_{SS}.

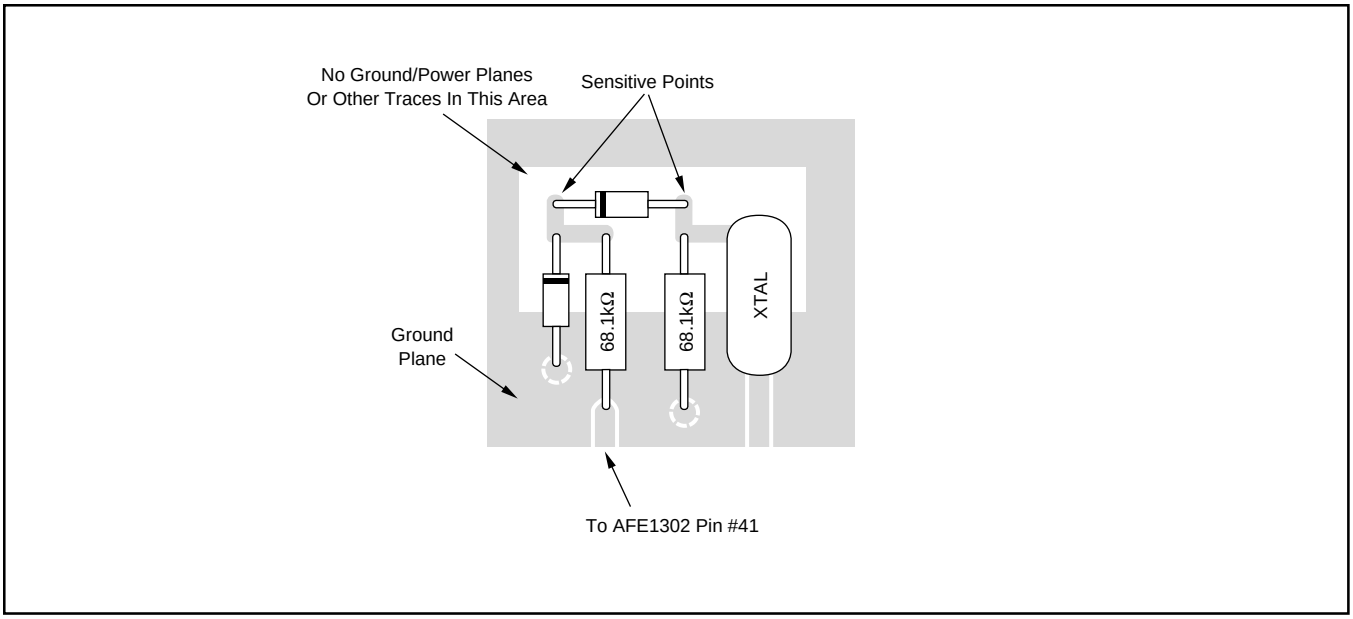


FIGURE 4. VCXO Circuit Layout, Approximately Two Times Actual Size.

SYSTEM

This analog front-end will give the best performance only when included in an optimized system. This section describes external components that will work best with the AFE1302. See Figure 5 for the basic connection diagram.

TRANSMIT

The key noise specification for an ADSL analog front-end is the noise that is added to the RX channel. It is essential to reduce the transmit noise that reaches the receiver for proper system operation. An on-chip fourth-order low-pass transmit filter has been included on the AFE1302 to reduce transmit noise in the receive bandwidth. However, external filtering, as shown in the reference design in Figure 6, is required on the transmitter output to optimize the receive path noise mask. The reference design circuit not only implements extra filtering for the transmit noise, but also includes the drivers necessary to achieve the G.992.2 specified +13dBm output power on the line, thus achieving a minimum component solution.

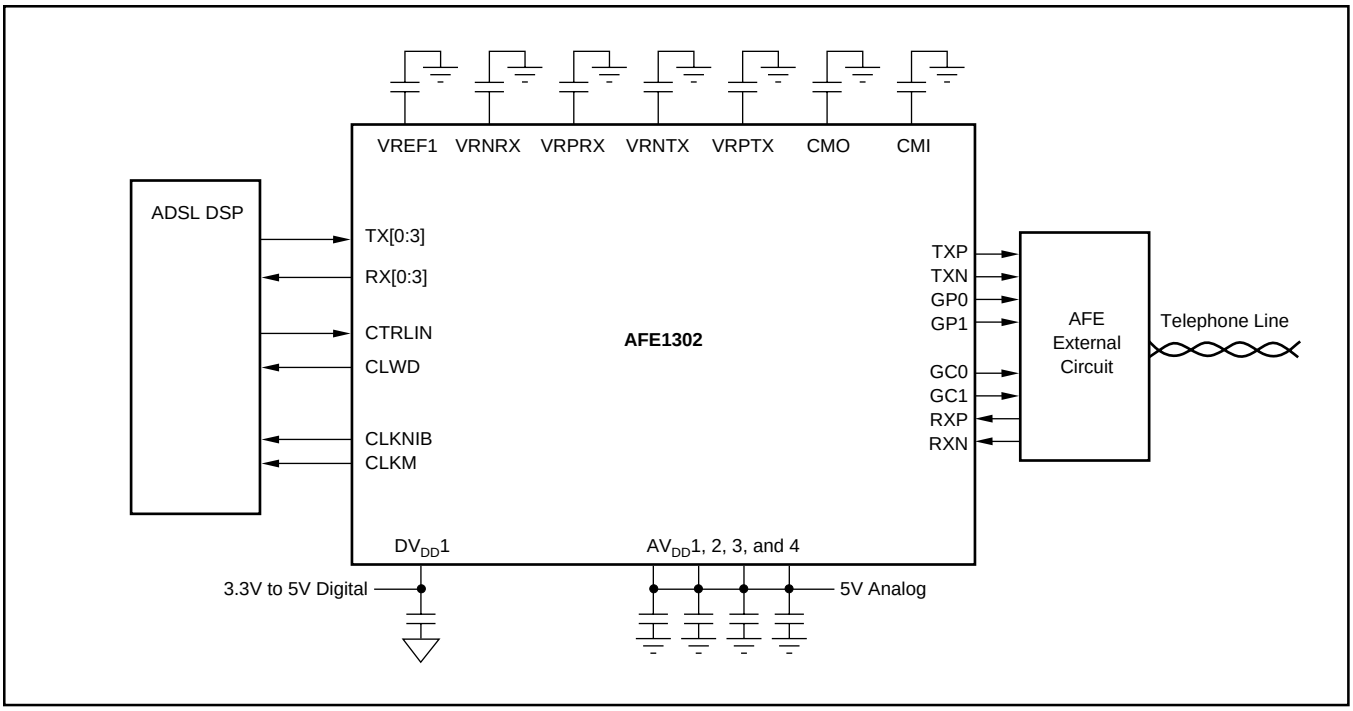


FIGURE 5. Basic Connection Diagram.

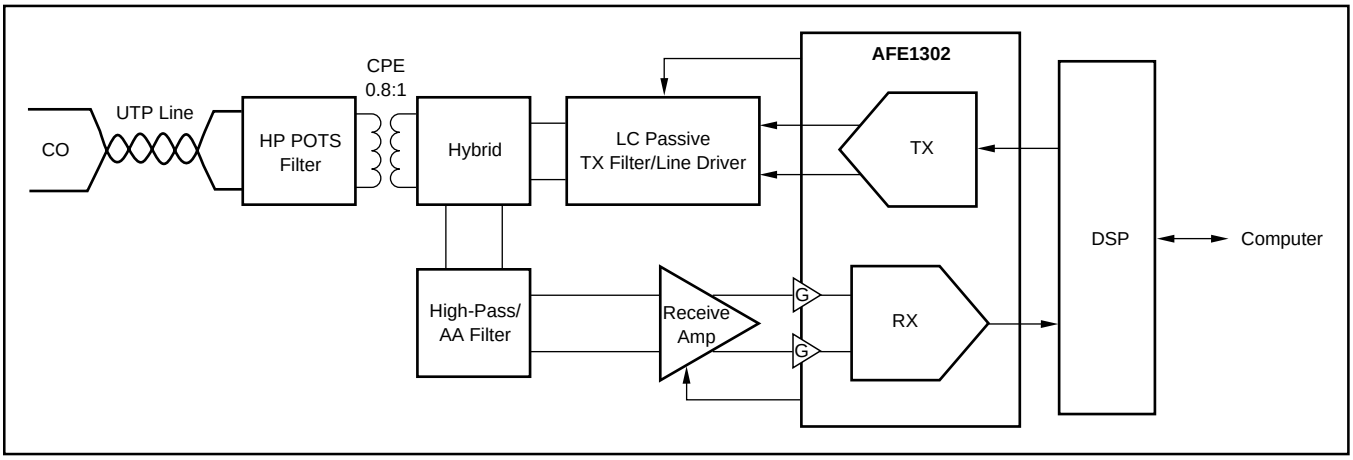


FIGURE 6. CPE Block Diagram (contact factory for detatiled reference design).

The specifications for the complete system solution are given in Table VIII. The numbers include the effects of both the AFE1302 and the surrounding external components, including a Burr-Brown TX line driver from Texas Instruments.

RECEIVE

Receive channel external components include a hybrid, receive amplifier, fifth-order high-pass passive filter, and first-order, low-pass, anti-alias filter. The ADSL system is frequency division multiplexed on a single twisted pair. Filters are used to separate the transmit and receive signals. When the AFE1302 drives long twisted-pair loops, the transmit signal is much larger than the receive signal. The hybrid will ideally eliminate all of the transmit signal at the receive input. However, for poorly matched lines, the actual reduction may be quite small. Without external filtering between the transmit output and the receive input, the transmit signal will clip the receive input before the on-chip receive filter can reduce the transmit signal. Therefore, external receive filters are required to eliminate transmit noise. Refer to Figure 6 for an external circuit and contact the factory for a detailed reference design document.

ADSL FRONT-END SYSTEM PERFORMANCE			
PARAMETER	**CONDITIONS**	**VALUE**	**UNITS**
TX PATH			
Peak Signal Amplitude to Telephone Line		12	Vp-p
Load Impedance		100	Ω
Output Power	To Line (100Ω Match)	13	dBm
Low-Pass Filter Corner Frequency		127	kHz
Passband Ripple		3	dB
Group Delay Variation		15	ms
Output Noise, Out of Band	See Note (2)	–142	dBm/Hz
RX PATH			
RX Input		12.5	Vp-p
MTPR		70	dB
Noise Floor	PGA = 40dB	–142	dBm/Hz
External High-Pass Filter Corner Frequency		157	kHz
Anti-Alias Filter Corner Frequency		1.1	MHz
Passband Ripple		3	dB
NOTE: (1) dBm referenced from average tone power and spread over 4kHz receive tone bins. (2) Measured at 200kHz with typical ADSL multitone transmission signal.			

TABLE VIII. ADSL Front-End System Performance when using the AFE1302 in a Texas Instruments Reference Design Evaluation Board. Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, f_{CLK} = 35.328MHz, TX output and RX input measured at line side.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
AFE1302Y/250	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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