19-0528; Rev 0; 5/06

EVALUATION KIT AVAILABLE

10-Bit, 22Msps, Full-Duplex Analog Front-End

General Description

The MAX19712 is an ultra-low-power, highly integrated mixed-signal analog front-end (AFE) ideal for wideband communication applications operating in full-duplex (FD) mode. Optimized for high dynamic performance and ultra-low power, the device integrates a dual 10-bit, 22Msps receive (Rx) ADC; dual 10-bit, 22Msps transmit (Tx) DAC; three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control; and a 10-bit, 333ksps housekeeping aux-ADC. The typical operating power in FD mode is 50.4mW at a 22MHz clock frequency.

The Rx ADCs feature 54.7dB SINAD and 75.6dBc SFDR at 5.5MHz input frequency with a 22MHz clock frequency. The analog I/Q input amplifiers are fully differential and accept 1.024V_{P-P} full-scale signals. Typical I/Q channel matching is ±0.01° phase and ±0.01dB gain.

The Tx DACs feature 72.9dBc SFDR at f_{OUT} = 2.2MHz and f_{CLK} = 22MHz. The analog I-Q full-scale output voltage range is ±400mV differential. The output DC common-mode voltage is from 0.89V to 1.36V. The I/Q channel offset is adjustable to optimize radio lineup sideband/carrier suppression. Typical I-Q channel matching is ±0.01dB gain and ±0.1° phase.

Two independent 10-bit parallel, high-speed digital buses used by the Rx ADC and Tx DAC allow full-duplex operation for frequency-division duplex applications. The Rx ADC and Tx DAC can be disabled independently to optimize power management. A 3-wire serial interface controls power-management modes, the aux-DAC channels, and the aux-ADC channels.

The MAX19712 operates on a single 2.7V to 3.3V analog supply and 1.8V to 3.3V digital I/O supply. The MAX19712 is specified for the extended (-40°C to +85°C) temperature range and is available in a 56-pin, thin QFN package. The *Selector Guide* at the end of the data sheet lists other pin-compatible versions in this AFE family. For time-division duplex (TDD) applications, refer to the MAX19705–MAX19708 AFE family of products.

Applications

WCDMA Handsets	VoIP Terminals
801.11a/b/g WLAN	Portable Communication Equipment
RFID Readers	

Ordering Information

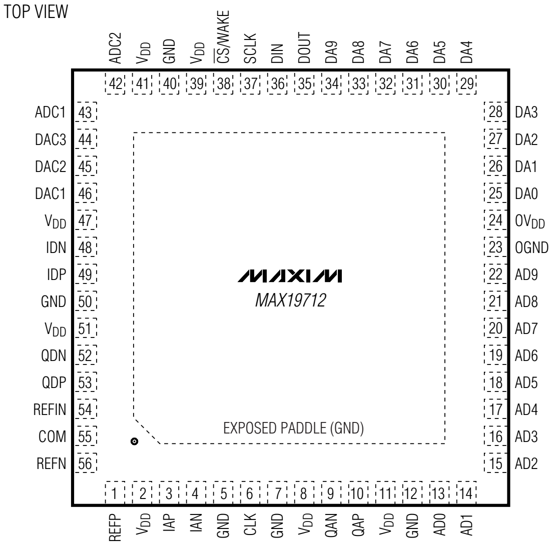
PART*	PIN-PACKAGE	PKG CODE
MAX19712ETN	56 Thin QFN-EP**	T5677-1
MAX19712ETN+	56 Thin QFN-EP**	T5677-1

**All devices are specified over the -40°C to +85°C operating range.*
***EP = Exposed paddle. +Denotes lead-free package.*

Features

- ♦ **Dual 10-Bit, 22Msps Rx ADC and Dual 10-Bit, 22Msps Tx DAC**
- ♦ **Ultra-Low Power**
  - **50.4mW at f_{CLK} = 22MHz, FD Mode**
  - **39.9mW at f_{CLK} = 22MHz, Slow Rx Mode**
  - **33.9mW at f_{CLK} = 22MHz, Slow Tx Mode**
  - **Low-Current Standby and Shutdown Modes**
- ♦ **Programmable Tx DAC Common-Mode DC Level and I/Q Offset Trim**
- ♦ **Excellent Dynamic Performance**
  - **SNR = 54.8dB at f_{IN} = 5.5MHz (Rx ADC)**
  - **SFDR = 72.9dBc at f_{OUT} = 2.2MHz (Tx DAC)**
- ♦ **Three 12-Bit, 1μs Aux-DACs**
- ♦ **10-Bit, 333ksps Aux-ADC with 4:1 Input Mux and Data Averaging**
- ♦ **Excellent Gain/Phase Match**
  - **±0.01° Phase, ±0.01dB Gain (Rx ADC) at f_{IN} = 5.5MHz**
- ♦ **Multiplexed Parallel Digital I/O**
- ♦ **Serial-Interface Control**
- ♦ **Versatile Power-Control Circuits**
  - **Shutdown, Standby, Idle, Tx/Rx Disable**
- ♦ **Miniature 56-Pin Thin QFN Package (7mm x 7mm x 0.8mm)**

Pin Configuration



THIN QFN

NOTE: THE PIN 1 INDICATOR IS "+" FOR LEAD-FREE DEVICES.

Functional Diagram and Selector Guide appear at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND, OV_{DD} to OGND ....-0.3V to +3.6V
GND to OGND...-0.3V to +0.3V
IAP, IAN, QAP, QAN, IDP, IDN, QDP,
QDN, DAC1, DAC2, DAC3 to GND ....-0.3V to V_{DD}
ADC1, ADC2 to GND................................-0.3V to (V_{DD} + 0.3V)
REFP, REFN, REFIN, COM to GND ....-0.3V to (V_{DD} + 0.3V)
AD0–AD9, DA0–DA9, SCLK, DIN, $\overline{CS}$/WAKE,
CLK, DOUT to OGND ....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
56-Pin Thin QFN-EP (derate 27.8mW/°C above +70°C) 2.22W
Thermal Resistance θ_{JA} ....36°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF, C_L < 5pF on all aux-DAC outputs, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		2.7	3.0	3.3	V
Output Supply Voltage	OV_{DD}		1.8		V_{DD}	V
V_{DD} Supply Current		FD mode: f_{CLK} = 22MHz, f_{OUT} = 2.2MHz on both DAC channels; f_{IN} = 5.5MHz on both ADC channels; aux-DACs ON and at midscale, aux-ADC ON		16.8	19	mA
		FD mode: f_{CLK} = 15.36MHz, f_{OUT} = 2.2MHz on both DAC channels; f_{IN} = 5.5MHz on both ADC channels; aux-DACs ON and at midscale, aux-ADC ON		13.4		
		SPI2-Tx mode: f_{CLK} = 22MHz, f_{OUT} = 2.2MHz on both DAC channels; Rx ADC OFF; aux-DACs ON and at midscale, aux-ADC ON		11.3	13	
		SPI1-Rx mode: f_{CLK} = 22MHz, f_{IN} = 5.5MHz on both ADC channels; Tx DAC OFF (Tx DAC outputs at 0V); aux-DACs ON and at midscale, aux-ADC ON		13.3	16	
		SPI4-Tx mode: f_{CLK} = 22MHz, f_{OUT} = 2.2MHz on both DAC channels; Rx ADC ON (output tri-stated); aux-DACs ON and at midscale, aux-ADC ON		16.4	19	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Supply Current		SPI3-Rx mode: f_{CLK} = 22MHz, f_{IN} = 5.5MHz on both channels; Tx DAC ON (Tx DAC outputs at midscale); aux-DACs ON and at midscale, aux-ADC ON		15.8	19	mA
		Standby mode: CLK = 0 or OV_{DD}; aux-DACs ON and at midscale, aux-ADC ON		2.7	4	
		Idle mode: f_{CLK} = 22MHz; aux-DACs ON and at midscale, aux-ADC ON		7.8	10	
		Shutdown mode: CLK = 0 or OV_{DD}, or aux-ADC OFF		0.5	5	µA
OV_{DD} Supply Current		FD mode: f_{CLK} = 22MHz, f_{OUT} = 2.2MHz on both DAC channels; f_{IN} = 5.5MHz on both ADC channels; aux-DACs ON and at midscale, aux-ADC ON		2.3		mA
		SPI1-Rx and SPI3-Rx modes: f_{CLK} = 22MHz, f_{IN} = 5.5MHz on both ADC channels; DAC input bus tri-stated; aux-DACs ON and at midscale, aux-ADC ON		2.2		
		SPI2-Tx and SPI4-Tx modes: f_{CLK} = 22MHz, f_{OUT} = 2.2MHz on both DAC channels; ADC output bus tri-stated; aux-DACs ON and at midscale, aux-ADC ON		160		µA
		Standby mode: CLK = 0 or OV_{DD}; aux-DACs ON and at midscale, aux-ADC ON		0.1		
		Idle mode: f_{CLK} = 22MHz; aux-DACs ON and at midscale, aux-ADC ON		37		
		Shutdown mode: CLK = 0 or OV_{DD}, or aux-ADC OFF		0.1		
Rx ADC DC ACCURACY						
Resolution	N		10			Bits
Integral Nonlinearity	INL			±0.6		LSB
Differential Nonlinearity	DNL			±0.45		LSB
Offset Error		Residual DC offset error	-5	±0.13	+5	%FS
Gain Error		Includes reference error	-5	±0.8	+5	%FS
DC Gain Matching			-0.15	±0.04	+0.15	dB
Offset Matching				±9		LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Temperature Coefficient				±30		ppm/°C
Power-Supply Rejection	PSRR	Offset (V_{DD} ±5%)		±0.1		LSB
		Gain (V_{DD} ±5%)		±0.05		
Rx ADC ANALOG INPUT						
Input Differential Range	V_{ID}	Differential or single-ended inputs		±0.512		V
Input Common-Mode Voltage Range	V_{CM}			V_{DD} / 2		V
Input Impedance	R_{IN}	Switched capacitor load		245		kΩ
	C_{IN}			5		pF
Rx ADC CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}	(Note 2)			22	MHz
Data Latency		Channel IA		5		Clock Cycles
		Channel QA		5.5		
Rx ADC DYNAMIC CHARACTERISTICS (Note 3)						
Signal-to-Noise Ratio	SNR	f_{IN} = 5.5MHz	53	54.8		dB
		f_{IN} = 12.5MHz		54.7		
Signal-to-Noise and Distortion	SINAD	f_{IN} = 5.5MHz	52.9	54.7		dB
		f_{IN} = 12.5MHz		54.6		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 5.5MHz	65.9	75.6		dBc
		f_{IN} = 12.5MHz		76.3		
Total Harmonic Distortion	THD	f_{IN} = 5.5MHz		-72.8	-64.3	dBc
		f_{IN} = 12.5MHz		-71.3		
Third-Harmonic Distortion	HD3	f_{IN} = 5.5MHz		-78.9		dBc
		f_{IN} = 12.5MHz		-76.7		
Intermodulation Distortion	IMD	f_{IN1} = 1MHz, A_{IN1} = -7dBFS; f_{IN2} = 1.8MHz, A_{IN2} = -7dBFS		-71		dBc
Third-Order Intermodulation Distortion	IM3	f_{IN1} = 1MHz, A_{IN1} = -7dBFS; f_{IN2} = 1.8MHz, A_{IN2} = -7dBFS		-78		dBc
Aperture Delay				3.5		ns
Aperture Jitter				2		ps_{RMS}
Overdrive Recovery Time		1.5x full-scale input		2		ns
Rx ADC INTERCHANNEL CHARACTERISTICS						
Crosstalk Rejection		$f_{INX,Y}$ = 5.5MHz, $A_{INX,Y}$ = -0.5dBFS, $f_{INY,X}$ = 1MHz, $A_{INY,X}$ = -0.5dBFS (Note 4)		-91		dB
Amplitude Matching		f_{IN} = 5.5MHz, A_{IN} = -0.5dBFS (Note 5)		±0.01		dB
Phase Matching		f_{IN} = 5.5MHz, A_{IN} = -0.5dBFS (Note 5)		±0.01		Degrees

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF, C_L < 5pF on all aux-DAC outputs, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tx DAC DC ACCURACY						
Resolution	N		10			Bits
Integral Nonlinearity	INL			±0.3		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 6)	-0.75	±0.2	+0.75	LSB
Residual DC Offset	V_{OS}		-4	±0.03	+4	mV
Full-Scale Gain Error			-40	±0.8	+40	mV
Tx DAC DYNAMIC PERFORMANCE						
DAC Conversion Rate	f_{CLK}	(Note 2)			22	MHz
In-Band Noise Density	N_D	f_{OUT} = 2.2MHz		-129		dBFS/Hz
Third-Order Intermodulation Distortion	IM3	f_{OUT1} = 2MHz, f_{OUT2} = 2.2MHz		-70		dBc
Glitch Impulse				10		pV•s
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{OUT} = 2.2MHz	61	72.9		dBc
Total Harmonic Distortion to Nyquist	THD	f_{OUT} = 2.2MHz		-71	-60.5	dBc
Signal-to-Noise Ratio to Nyquist	SNR	f_{OUT} = 2.2MHz		59.3		dB
Tx DAC INTERCHANNEL CHARACTERISTICS						
I-to-Q Output Isolation		$f_{OUTX,Y}$ = 2MHz, $f_{OUTY,X}$ = 2.2MHz		88		dB
Gain Mismatch Between I and Q Channels		Measured at DC	-0.4	±0.01	+0.4	dB
Phase Mismatch Between I and Q Channels		f_{OUT} = 2.2MHz		±0.1		Degrees
Differential Output Impedance				800		Ω
Tx DAC ANALOG OUTPUT						
Full-Scale Output Voltage	V_{FS}			±400		mV
Output Common-Mode Voltage	V_{COMD}	Bits CM1 = 0, CM0 = 0 (default)	1.29	1.36	1.42	V
		Bits CM1 = 0, CM0 = 1	1.14	1.2	1.27	
		Bits CM1 = 1, CM0 = 0	0.96	1.05	1.15	
		Bits CM1 = 1, CM0 = 1	0.78	0.89	1.03	
Rx ADC–Tx DAC INTERCHANNEL CHARACTERISTICS						
Receive Transmit Isolation		ADC $f_{INI} = f_{INQ}$ = 5.5MHz, DAC $f_{OUTI} = f_{OUTQ}$ = 2.2MHz		85		dB
AUXILIARY ADCs (ADC1, ADC2)						
Resolution	N		10			Bits
Full-Scale Reference	V_{REF}	AD1 = 0 (default)		2.048		V
		AD1 = 1		V_{DD}		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input Range				0 to V_{REF}		V
Analog Input Impedance		Measured at DC		500		kΩ
Input-Leakage Current		Measured at unselected input from 0 to V_{REF}		±0.1		µA
Gain Error	GE	Includes reference error, AD1 = 0	-5		+5	%FS
Zero-Code Error	ZE			±2		mV
Differential Nonlinearity	DNL			±0.6		LSB
Integral Nonlinearity	INL			±0.6		LSB
Supply Current				210		µA
AUXILIARY DACs (DAC1, DAC2, DAC3)						
Resolution	N		12			Bits
Integral Nonlinearity	INL	From code 100 to code 4000		±1.25		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic over code 100 to code 4000 (Note 6)	-1.0	±0.65	+1.2	LSB
Output-Voltage Low	V_{OL}	R_L > 200kΩ			0.2	V
Output-Voltage High	V_{OH}	R_L > 200kΩ	2.57			V
DC Output Impedance		DC output at midscale		4		Ω
Settling Time		From code 1024 to code 3072, within ±10 LSB		1		µs
Glitch Impulse		From code 0 to code 4095		24		nV•s
Rx ADC–Tx DAC TIMING CHARACTERISTICS						
CLK Rise to Channel-I Output Data Valid	t_{DOI}	Figure 3 (Note 6)	5.5	8.2	11.5	ns
CLK Fall to Channel-Q Output Data Valid	t_{DOQ}	Figure 3 (Note 6)	6.5	9.5	13.0	ns
I-DAC DATA to CLK Fall Setup Time	t_{DSI}	Figure 5 (Note 6)	10			ns
Q-DAC DATA to CLK Rise Setup Time	t_{DSQ}	Figure 5 (Note 6)	10			ns
CLK Fall to I-DAC Data Hold Time	t_{DHI}	Figure 5 (Note 6)	0			ns
CLK Rise to Q-DAC Data Hold Time	t_{DHQ}	Figure 5 (Note 6)	0			ns
CLK Duty Cycle				50		%
CLK Duty-Cycle Variation				±15		%
Digital Output Rise/Fall Time		20% to 80%		2.4		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF, C_L < 5pF on all aux-DAC outputs, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL-INTERFACE TIMING CHARACTERISTICS (Figures 6 and 8, Note 2)						
Falling Edge of $\overline{\text{CS}}$/WAKE to Rising Edge of First SCLK Time	t_{CSS}		10			ns
DIN to SCLK Setup Time	t_{DS}		10			ns
DIN to SCLK Hold Time	t_{DH}		0			ns
SCLK Pulse-Width High	t_{CH}		25			ns
SCLK Pulse-Width Low	t_{CL}		25			ns
SCLK Period	t_{CP}		50			ns
SCLK to $\overline{\text{CS}}$/WAKE Setup Time	t_{CS}		10			ns
$\overline{\text{CS}}$/WAKE High Pulse Width	t_{CSW}		80			ns
$\overline{\text{CS}}$/WAKE High to DOUT Active High	t_{CSD}	Bit AD0 set		200		ns
$\overline{\text{CS}}$/WAKE High to DOUT Low (Aux-ADC Conversion Time)	t_{CONV}	Bit AD0 set, no averaging, f_{CLK} = 22MHz, CLK divider = 8		4.3		µs
DOUT Low to $\overline{\text{CS}}$/WAKE Setup Time	t_{DCS}	Bit AD0, AD10 set		200		ns
SCLK Low to DOUT Data Out	t_{CD}	Bit AD0, AD10 set			14.5	ns
$\overline{\text{CS}}$/WAKE High to DOUT High Impedance	t_{CHZ}	Bit AD0, AD10 set		200		ns
MODE-RECOVERY TIMING CHARACTERISTICS (Figure 7)						
Shutdown Wake-Up Time (With CLK)	$t_{WAKE,SD}$	From shutdown to Rx mode, ADC settles to within 1dB SINAD		500		µs
		From shutdown to Tx mode, DAC settles to within 10 LSB error		26.2		
		From aux-ADC enable to aux-ADC start conversion		10		
		From shutdown to aux-DAC output valid		28		
		From shutdown to FD mode, ADC settles to within 1dB SINAD, DAC settles to within 10 LSB error		500		
Idle Wake-Up Time (With CLK)	$t_{WAKE,ST0}$	From idle to Rx mode, ADC settles to within 1dB SINAD		7.2		µs
		From idle to Tx mode, DAC settles to 10 LSB error		5.1		
		From idle to FD mode, ADC settles to within 1dB SINAD, DAC settles to within 10 LSB error		7.2		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Wake-Up Time (With CLK)	$t_{WAKE,ST1}$	From standby to Rx mode, ADC settles to within 1dB SINAD		7.1		µs
		From standby to Tx mode, DAC settles to 10 LSB error		22.8		
		From standby to FD mode, ADC settles to within 1dB SINAD, DAC settles to within 10 LSB error		22.8		
Enable Time from Tx to Rx, Fast Mode	$t_{ENABLE,RX}$	ADC settles to within 1dB SINAD		0.1		µs
Enable Time from Rx to Tx, Fast Mode	$t_{ENABLE,TX}$	DAC settles to within 10 LSB error		0.1		µs
Enable Time from Tx to Rx, Slow Mode	$t_{ENABLE,RX}$	ADC settles to within 1dB SINAD		7.5		µs
Enable Time from Rx to Tx, Slow Mode	$t_{ENABLE,TX}$	DAC settles to within 10 LSB error		5.1		µs
INTERNAL REFERENCE (V_{REFIN} = V_{DD}; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Positive Reference		V_{REFP} - V_{COM}		0.256		V
Negative Reference		V_{REFN} - V_{COM}		-0.256		V
Common-Mode Output Voltage	V_{COM}		V_{DD} / 2 - 0.15	V_{DD} / 2	V_{DD} / 2 + 0.15	V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
Differential Reference Output	V_{REF}	V_{REFP} - V_{REFN}	+0.490	+0.512	+0.534	V
Differential Reference Temperature Coefficient	REFTC			±30		ppm/°C
BUFFERED EXTERNAL REFERENCE (external V_{REFIN} = 1.024V applied; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Reference Input Voltage	V_{REFIN}			1.024		V
Differential Reference Output	V_{DIFF}	V_{REFP} - V_{REFN}		0.512		V
Common-Mode Output Voltage	V_{COM}			V_{DD} / 2		V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
REFIN Input Current				-0.7		µA
REFIN Input Resistance				500		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF, C_L < 5pF on all aux-DAC outputs, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (CLK, SCLK, DIN, $\overline{\text{CS}}$/WAKE, DA9–DA0)						
Input High Threshold	V_{INH}		0.7 x OV_{DD}			V
Input Low Threshold	V_{INL}				0.3 x OV_{DD}	V
Input Leakage	DI_{IN}	CLK, SCLK, DIN, $\overline{\text{CS}}$/WAKE = OGND or OV_{DD}	-1		+1	µA
		DA9–DA0 = OV_{DD}	-1		+1	
		DA9–DA0 = OGND	-5		+5	
Input Capacitance	DC_{IN}			5		pF
DIGITAL OUTPUTS (AD9–AD0, DOUT)						
Output-Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2 x OV_{DD}	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 200µA	0.8 x OV_{DD}			V
Tri-State Leakage Current	I_{LEAK}		-1		+1	µA
Tri-State Output Capacitance	C_{OUT}			5		pF

Note 1: Specifications from T_A = +25°C to +85°C guaranteed by production tests. Specifications at T_A < +25°C guaranteed by design and characterization.

Note 2: The minimum clock frequency (f_{CLK}) for the MAX19712 is 2MHz (typ). The minimum aux-ADC sample rate clock frequency (A_{CLK}) is determined by f_{CLK} and the chosen aux-ADC clock-divider value. The minimum aux-ADC A_{CLK} > 2MHz / 128 = 15.6kHz. The aux-ADC conversion time does not include the time to clock the serial data out of DOUT. The maximum conversion time (for no averaging, NAVG = 1) will be t_{CONV} (max) = (12 x 1 x 128) / 2MHz = 768µs.

Note 3: SNR, SINAD, SFDR, HD3, and THD are based on a differential analog input voltage of -0.5dBFS referenced to the amplitude of the digital outputs. SINAD and THD are calculated using HD2 through HD6.

Note 4: Crosstalk rejection is measured by applying a high-frequency test tone to one channel and a low-frequency tone to the second channel. FFTs are performed on each channel. The parameter is specified as the power ratio of the first and second channel FFT test tones.

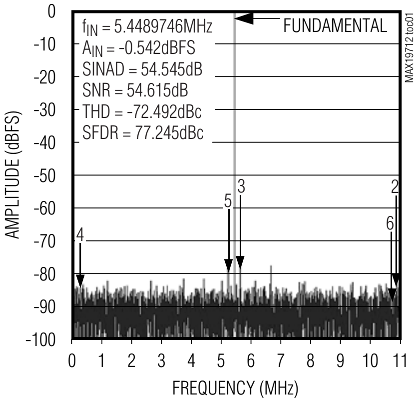
Note 5: Amplitude and phase matching are measured by applying the same signal to each channel, and comparing the two output signals using a sine-wave fit.

Note 6: Guaranteed by design and characterization.

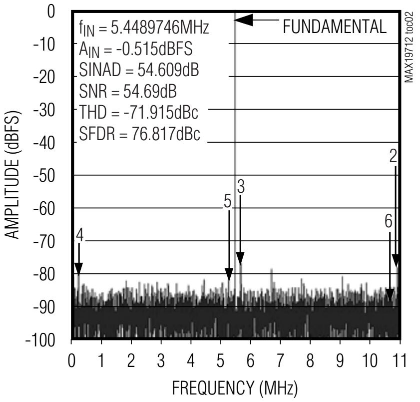
Typical Operating Characteristics

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

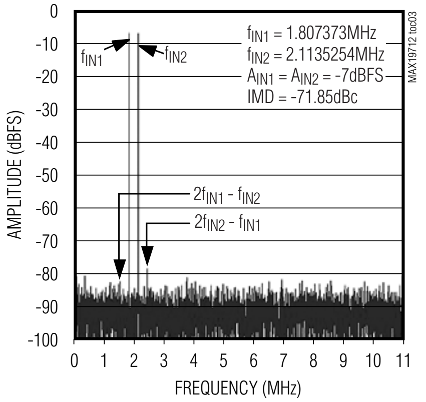
Rx ADC CHANNEL-IA FFT PLOT (8192 SAMPLES)



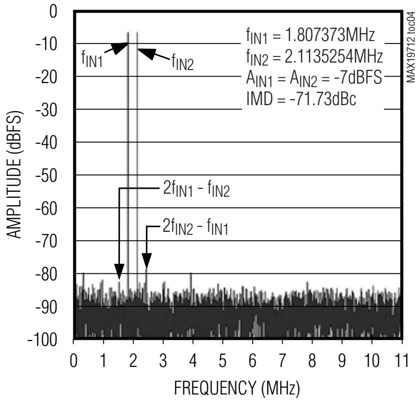
Rx ADC CHANNEL-QA FFT PLOT (8192 SAMPLES)



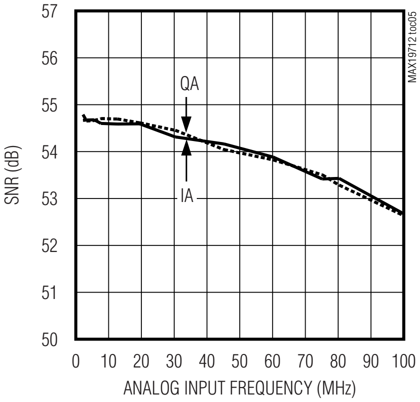
Rx ADC CHANNEL-IA TWO-TONE FFT PLOT (8192 SAMPLES)



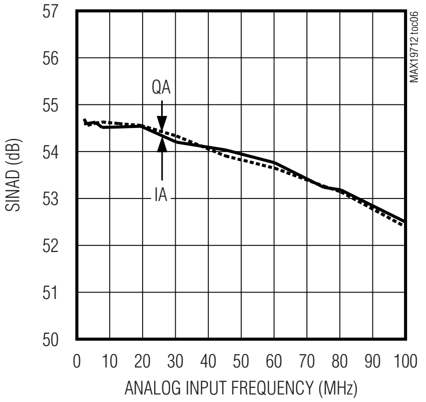
Rx ADC CHANNEL-QA TWO-TONE FFT PLOT (8192 SAMPLES)



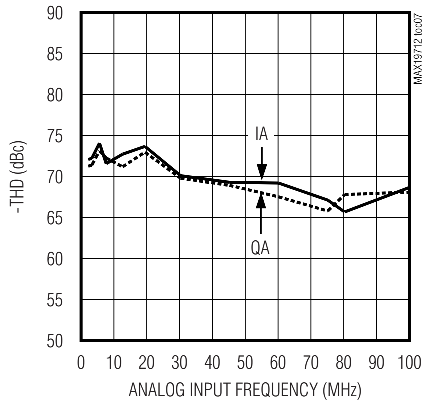
Rx ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



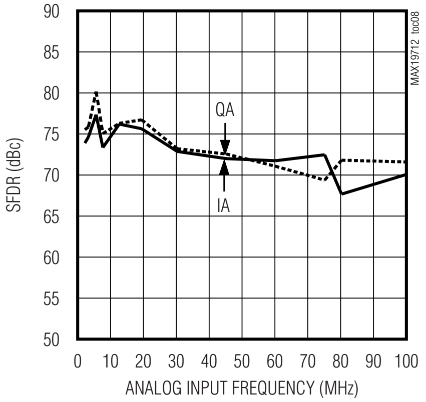
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT FREQUENCY



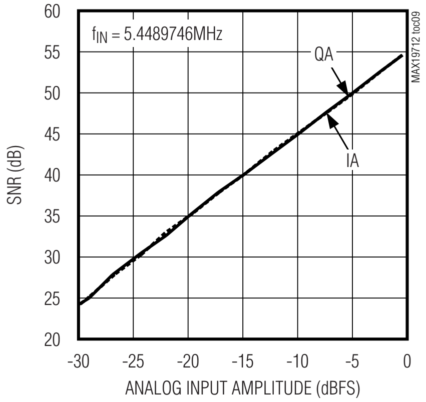
Rx ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



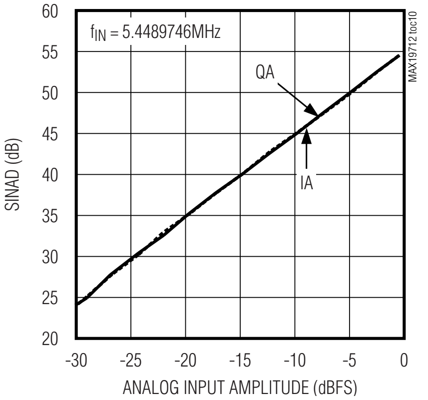
Rx ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT AMPLITUDE



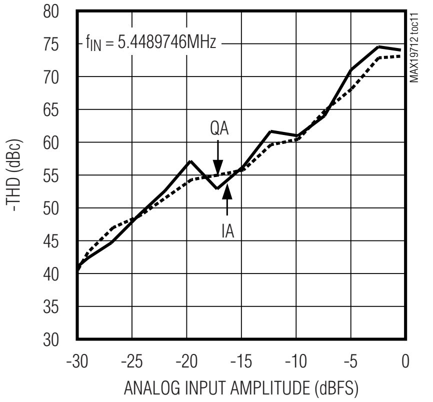
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

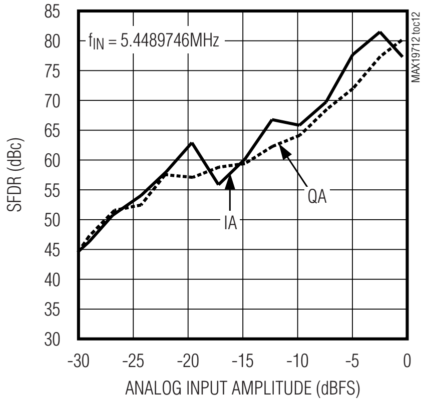
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT AMPLITUDE



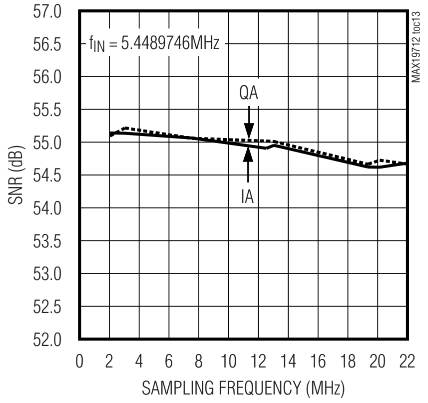
Rx ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT AMPLITUDE



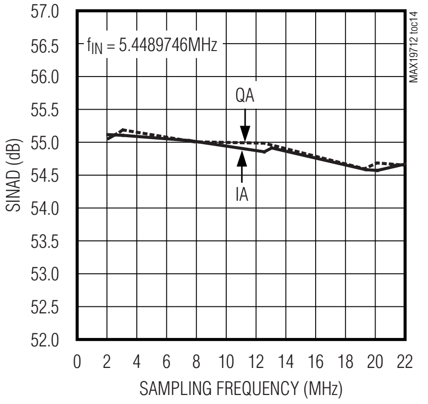
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT AMPLITUDE



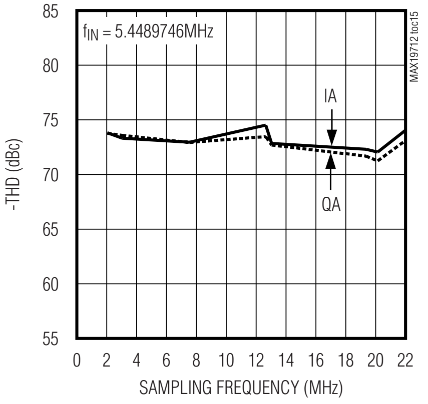
Rx ADC SIGNAL-TO-NOISE RATIO vs. SAMPLING FREQUENCY



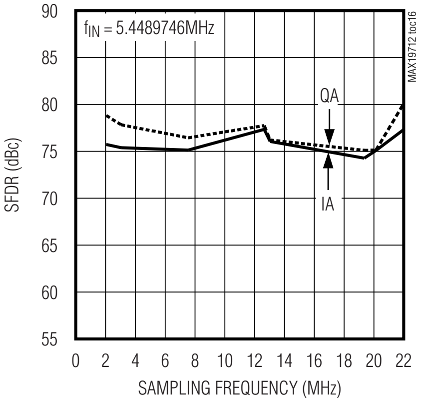
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. SAMPLING FREQUENCY



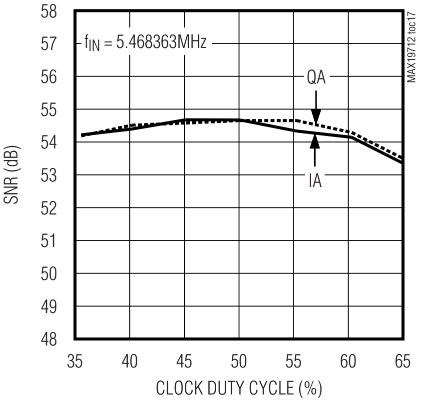
Rx ADC TOTAL HARMONIC DISTORTION vs. SAMPLING RATE



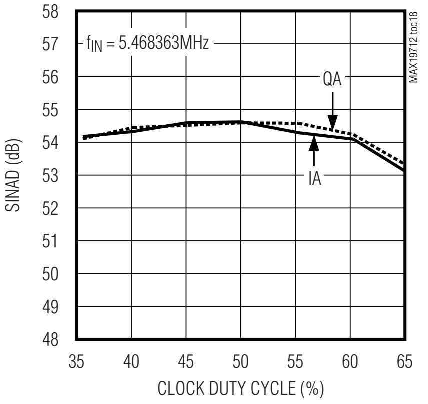
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING FREQUENCY



Rx ADC SIGNAL-TO-NOISE RATIO vs. CLOCK DUTY CYCLE



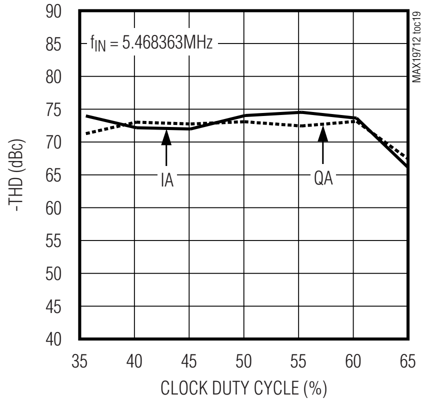
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. CLOCK DUTY CYCLE



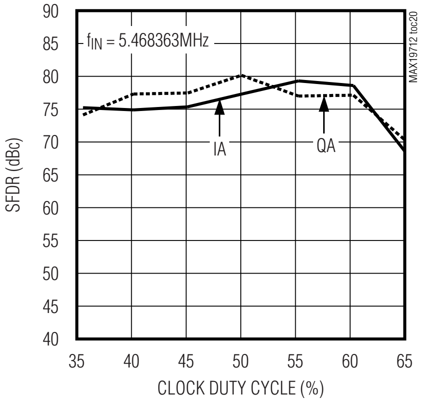
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF, T_A = +25°C, unless otherwise noted.)

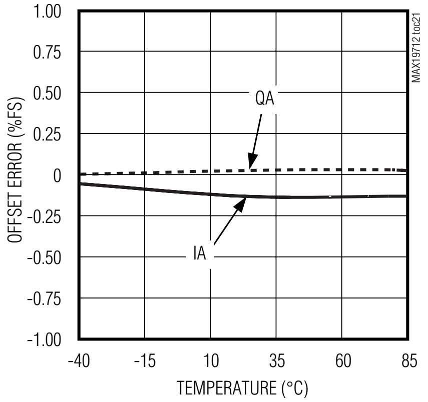
Rx ADC TOTAL HARMONIC DISTORTION vs. CLOCK DUTY CYCLE



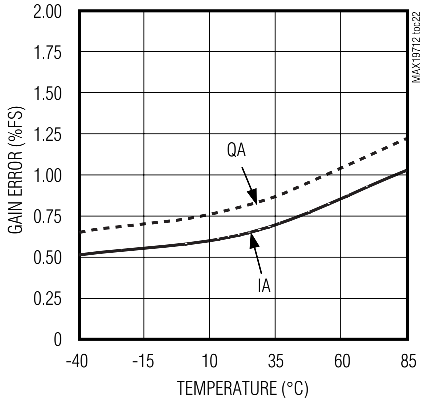
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK DUTY CYCLE



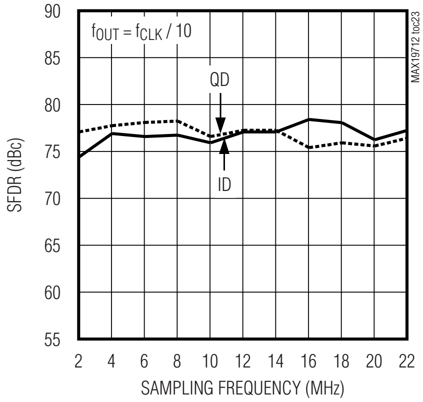
Rx ADC OFFSET ERROR vs. TEMPERATURE



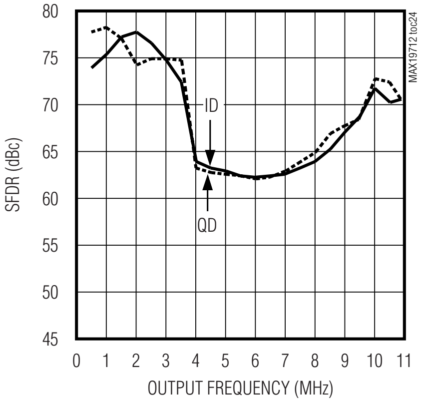
Rx ADC GAIN ERROR vs. TEMPERATURE



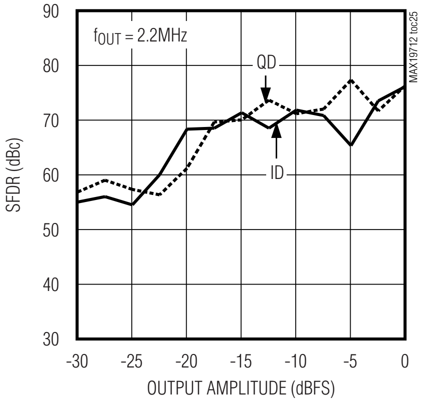
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING FREQUENCY



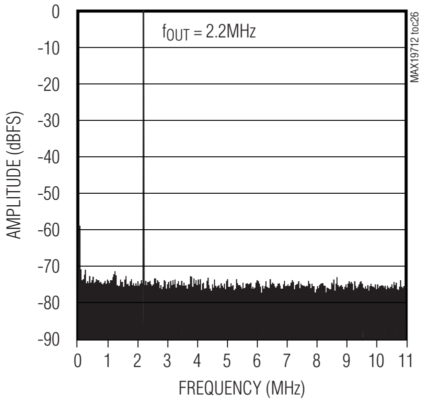
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY



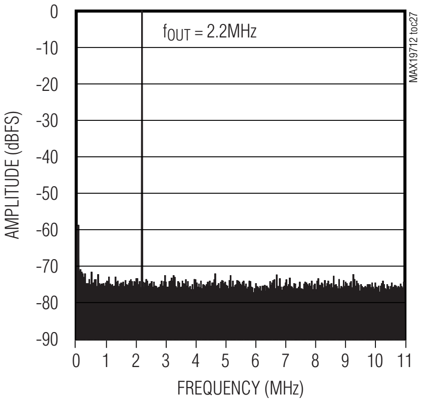
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT AMPLITUDE



Tx DAC CHANNEL-ID SPECTRAL PLOT



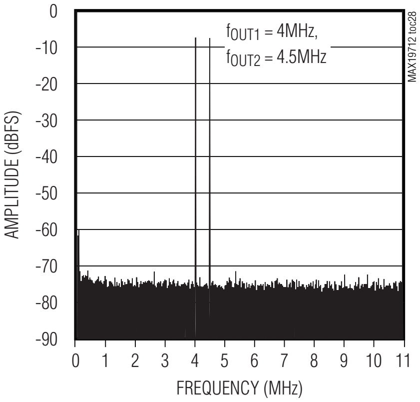
Tx DAC CHANNEL-QD SPECTRAL PLOT



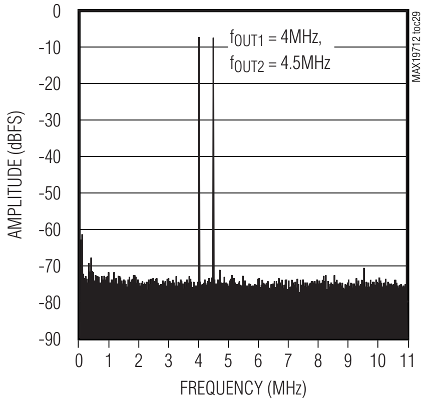
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

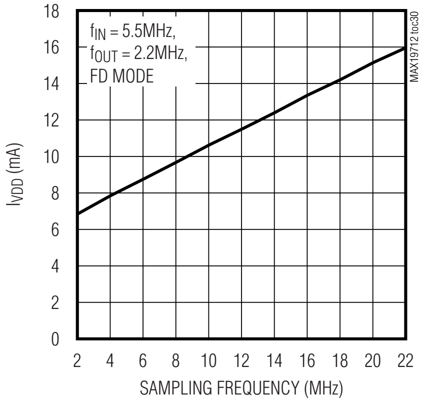
Tx DAC CHANNEL-ID TWO-TONE SPECTAL PLOT



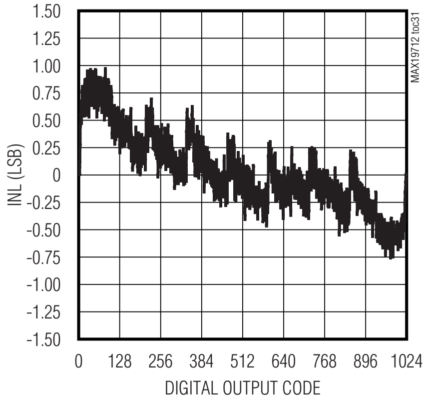
Tx DAC CHANNEL-QD TWO-TONE SPECTAL PLOT



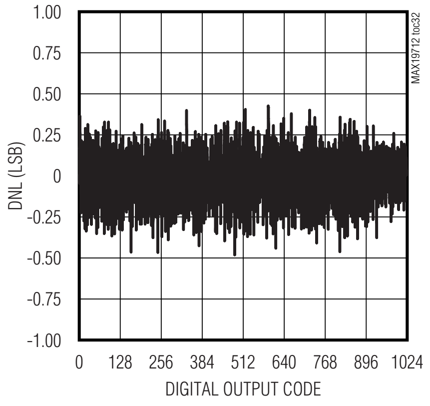
SUPPLY CURRENT vs. SAMPLING FREQUENCY



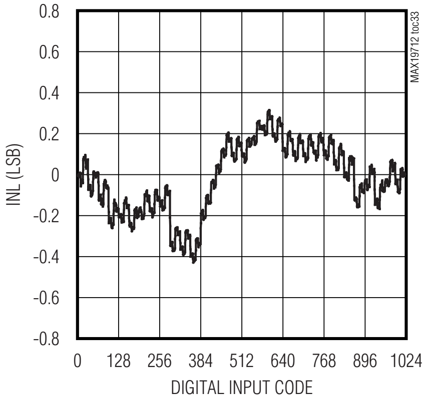
Rx ADC INTEGRAL NONLINEARITY



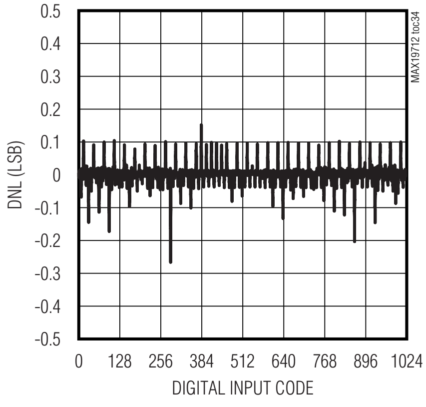
Rx ADC DIFFERENTIAL NONLINEARITY



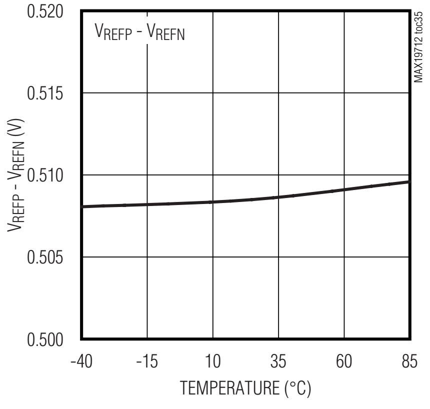
Tx DAC INTEGRAL NONLINEARITY



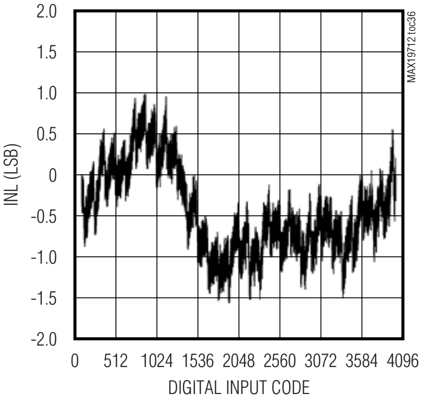
Tx DAC DIFFERENTIAL NONLINEARITY



REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE

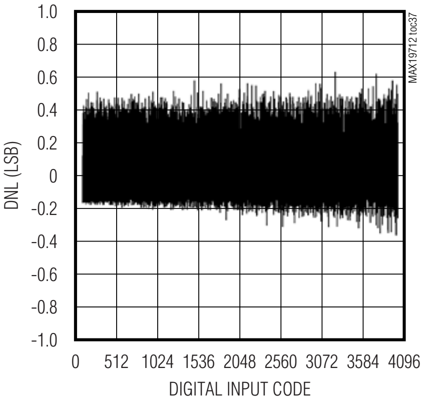


AUX-DAC INTEGRAL NONLINEARITY

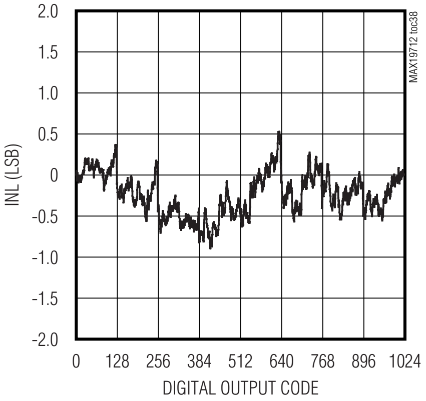


Typical Operating Characteristics (continued)

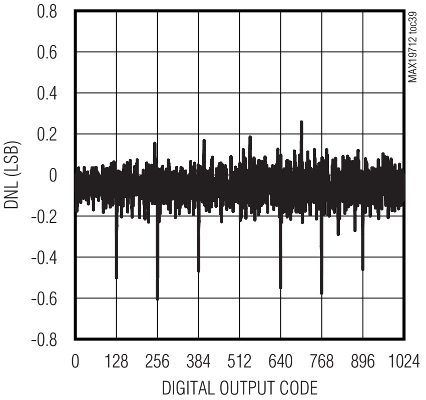
(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 22MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)



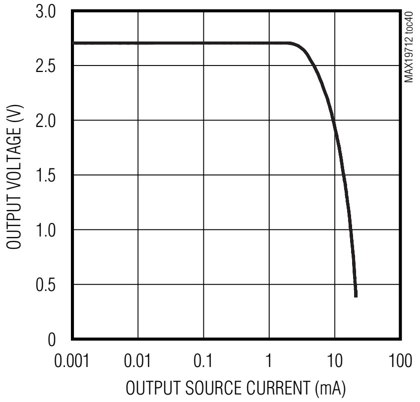
AUX-DAC DIFFERENTIAL NONLINEARITY



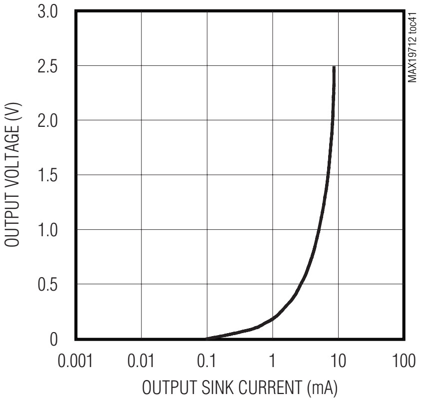
AUX-ADC INTEGRAL NONLINEARITY



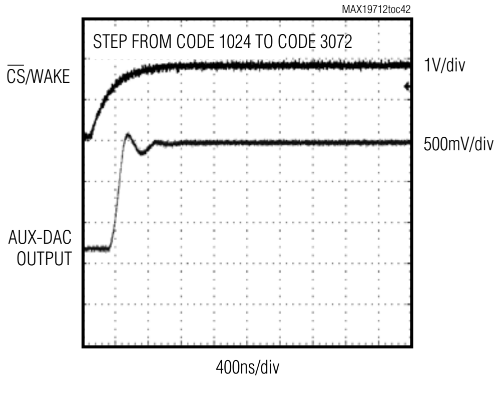
AUX-ADC DIFFERENTIAL NONLINEARITY



AUX-DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



AUX-DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



AUX-DAC SETTLING TIME

Pin Description

PIN	NAME	FUNCTION
1	REFP	Positive Reference Voltage Input Terminal. Bypass with a 0.33µF capacitor to GND as close to REFP as possible.
2, 8, 11, 39, 41, 47, 51	V_{DD}	Analog Supply Voltage. Bypass V_{DD} to GND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
3	IAP	Channel-IA Positive Analog Input. For single-ended operation, connect signal source to IAP.
4	IAN	Channel-IA Negative Analog Input. For single-ended operation, connect IAN to COM.
5, 7, 12, 40, 50	GND	Analog Ground. Connect all GND pins to ground plane.
6	CLK	Conversion Clock Input. Clock signal for both receive ADCs and transmit DACs.
9	QAN	Channel-QA Negative Analog Input. For single-ended operation, connect QAN to COM.
10	QAP	Channel-QA Positive Analog Input. For single-ended operation, connect signal source to QAP.
13–22	AD0–AD9	Receive ADC Digital Outputs. AD9 is the most significant bit (MSB) and AD0 is the least significant bit (LSB).
23	OGND	Output-Driver Ground
24	OV_{DD}	Output-Driver Power Supply. Supply range from +1.8V to V_{DD}. Bypass OV_{DD} to OGND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
25–34	DA0–DA9	Transmit DAC Digital Inputs. DA9 is the most significant bit (MSB) and DA0 is the least significant bit (LSB). DA0–DA9 are internally pulled up to OV_{DD}.
35	DOUT	Aux-ADC Digital Output
36	DIN	3-Wire Serial-Interface Data Input. Data is latched on the rising edge of SCLK.
37	SCLK	3-Wire Serial-Interface Clock Input
38	$\overline{CS}$/WAKE	3-Wire Serial-Interface Chip-Select/WAKE Input. When the MAX19712 is in shutdown, $\overline{CS}$/WAKE controls the wake-up function. See the *Wake-Up Function* section.
42	ADC2	Selectable Auxiliary ADC Analog Input 2
43	ADC1	Selectable Auxiliary ADC Analog Input 1
44	DAC3	Auxiliary DAC3 Analog Output (V_{OUT} = 0 at Power-Up)
45	DAC2	Auxiliary DAC2 Analog Output (V_{OUT} = 0 at Power-Up)
46	DAC1	Auxiliary DAC1 Analog Output (AFC DAC, V_{OUT} = 1.1V at Power-Up)
48	IDN	Tx DAC Channel-ID Differential Negative Output
49	IDP	Tx DAC Channel-ID Differential Positive Output
52	QDN	Tx DAC Channel-QD Differential Negative Output
53	QDP	Tx DAC Channel-QD Differential Positive Output
54	REFIN	Reference Input. Connect to V_{DD} for internal reference.
55	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 0.33µF capacitor.
56	REFN	Negative Reference Voltage Input Terminal. Rx ADC conversion range is ±(V_{REFP} - V_{REFN}). Bypass REFN to GND with a 0.33µF capacitor.
—	EP	Exposed Paddle. Exposed paddle is internally connected to GND. Connect EP to the GND plane.

Detailed Description

The MAX19712 integrates a dual, 10-bit Rx ADC and a dual, 10-bit Tx DAC while providing ultra-low power and high dynamic performance at 22Msps conversion rate. The Rx ADC analog input amplifiers are fully differential and accept 1.024V_{P-P} full-scale signals. The Tx DAC analog outputs are fully differential with ±400mV full-scale output, selectable common-mode DC level, and adjustable channel ID–QD offset trim.

The MAX19712 integrates three 12-bit auxiliary DACs (aux-DACs) and a 10-bit, 333ksps auxiliary ADC (aux-ADC) with 4:1 input multiplexer. The aux-DAC channels feature 1µs settling time for fast AGC, VGA, and AFC level setting. The aux-ADC features data averaging to reduce processor overhead and a selectable clock-divider to program the conversion rate.

The MAX19712 includes a 3-wire serial interface to control operating modes and power management. The serial interface is SPI™ and MICROWIRE™ compatible. The MAX19712 serial interface selects shutdown, idle, standby, FD, transmit (Tx), and receive (Rx) modes, as well as controls aux-DAC and aux-ADC channels.

The MAX19712 features two independent, high-speed, 10-bit buses for the Rx ADC and Tx DAC, which allow full-duplex (FD) operation for frequency-division duplex applications. Each bus can be disabled to optimize power management through the 3-wire interface. The MAX19712 operates from a single 2.7V to 3.3V analog supply and a 1.8V to 3.3V digital supply.

Dual 10-Bit Rx ADC

The ADC uses a seven-stage, fully differential, pipelined architecture that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for channel IA and 5.5 clock cycles for channel QA. The ADC full-scale analog input range is $\pm V_{REF}$ with a V_{DD} / 2 (±0.8V) common-mode input range. V_{REF} is the difference between V_{REFP} and V_{REFN}. See the *Reference Configurations* section for details.

Input Track-and-Hold (T/H) Circuits

Figure 1 displays a simplified diagram of the Rx ADC input track-and-hold (T/H) circuitry. Both ADC inputs (IAP, QAP, IAN, and QAN) can be driven either differen-

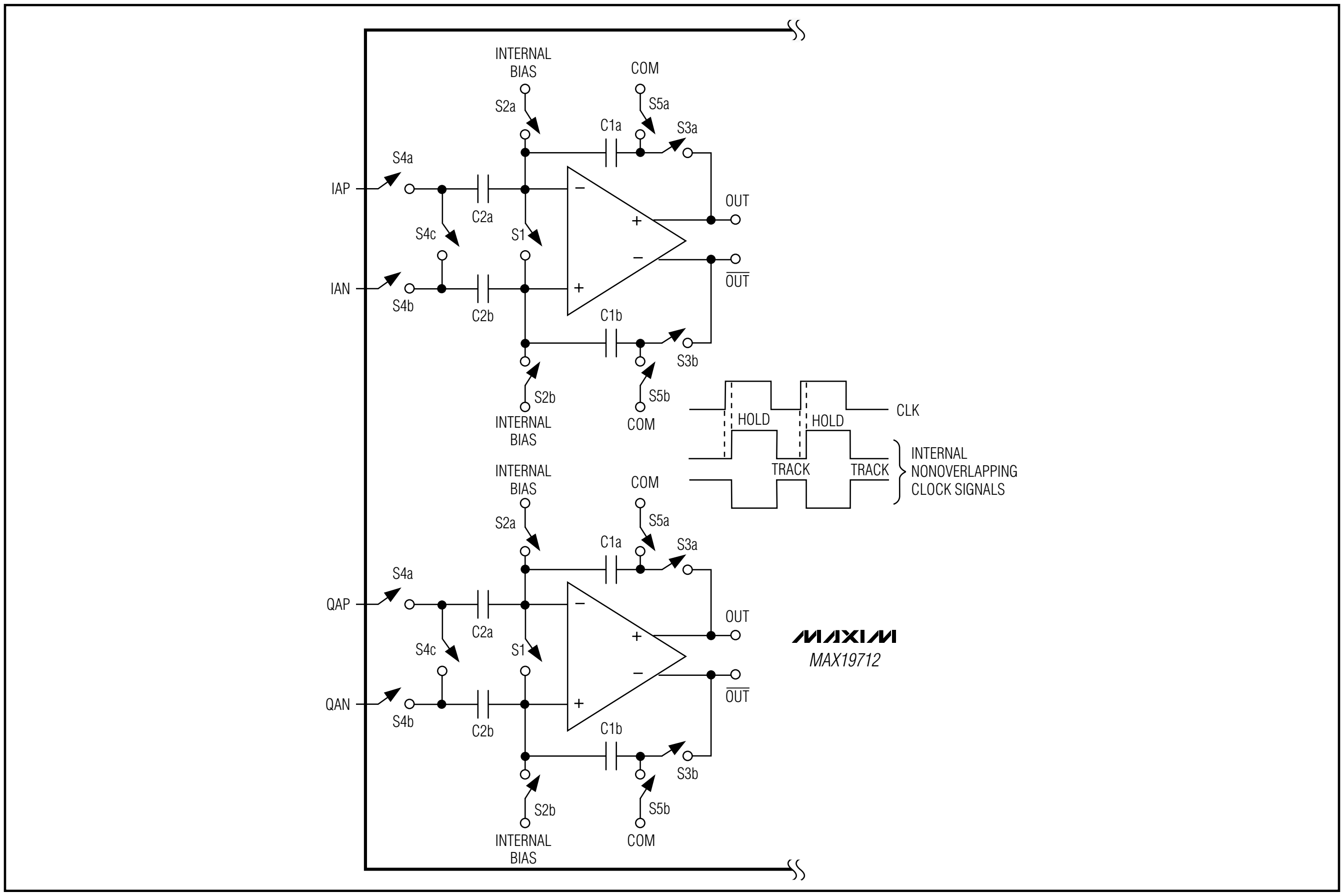


Figure 1. Rx ADC Internal T/H Circuits

MICROWIRE is a trademark of National Semiconductor Corp.

SPI is a trademark of Motorola, Inc.

Table 1. Rx ADC Output Codes vs. Input Voltage

DIFFERENTIAL INPUT VOLTAGE	DIFFERENTIAL INPUT (LSB)	OFFSET BINARY (AD0–AD9)	OUTPUT DECIMAL CODE
V_{REF} x 512/512	511 (+Full Scale - 1 LSB)	11 1111 1111	1023
V_{REF} x 511/512	510 (+Full Scale - 2 LSB)	11 1111 1110	1022
V_{REF} x 1/512	+1	10 0000 0001	513
V_{REF} x 0/512	0 (Bipolar Zero)	10 0000 0000	512
-V_{REF} x 1/512	-1	01 1111 1111	511
-V_{REF} x 511/512	-511 (-Full Scale + 1 LSB)	00 0000 0001	1
-V_{REF} x 512/512	-512 (-Full Scale)	00 0000 0000	0

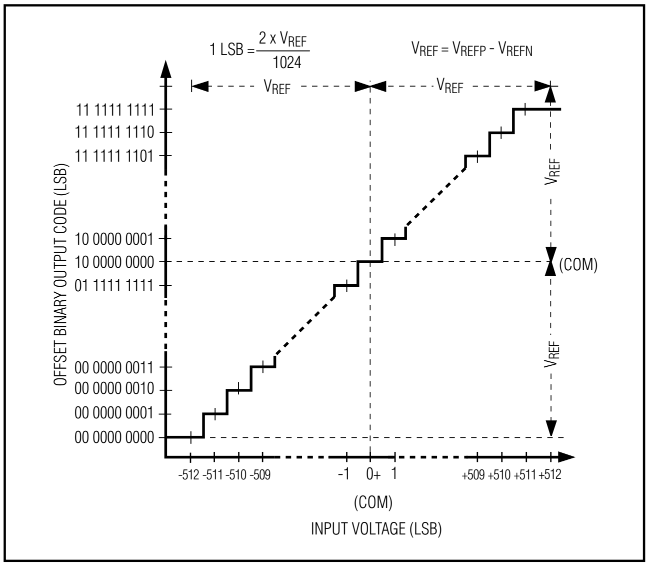


Figure 2. Rx ADC Transfer Function

tially or single-ended. Match the impedance of IAP and IAN, as well as QAP and QAN, and set the input signal common-mode voltage within the V_{DD} / 2 (±0.8V) Rx ADC range for optimum performance.

Rx ADC System Timing Requirements

Figure 3 shows the relationship between the clock, analog inputs, and the resulting output data. Channels IA and QA are sampled on the rising edge of the clock signal (CLK) and the resulting data is multiplexed at the AD0–AD9 outputs. Channel IA data is updated on the rising edge and channel QA data is updated on the falling edge of CLK. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for channel IA and 5.5 clock cycles for channel QA.

Digital Output Data (AD0–AD9)

AD0–AD9 are the Rx ADC digital logic outputs of the MAX19712. The logic level is set by OV_{DD} from 1.8V to V_{DD}. The digital output coding is offset binary (Table 1). Keep the capacitive load on the digital outputs AD0–AD9 as low as possible (< 15pF) to avoid large digital currents feeding back into the analog portion of the MAX19712 and degrading its dynamic performance. Buffers on the digital outputs isolate the outputs from heavy capacitive loads. Adding 100Ω resistors in series with the digital outputs close to the MAX19712 will help improve ADC performance. Refer to the MAX19712EVKIT schematic for an example of the digital outputs driving a digital buffer through 100Ω series resistors.

During SHDN, IDLE, STBY, SPI2, and SPI4 states, digital outputs AD0–AD9 are tri-stated.

Dual 10-Bit Tx DACs

The dual 10-bit digital-to-analog converters (Tx DACs) operate with clock speeds up to 22MHz. The Tx DAC digital inputs, DA0–DA9, are multiplexed on a single 10-bit transmit bus. The voltage reference determines the Tx DAC full-scale voltage at IDP, IDN and QDP, QDN analog outputs. See the *Reference Configurations* section for setting the reference voltage.

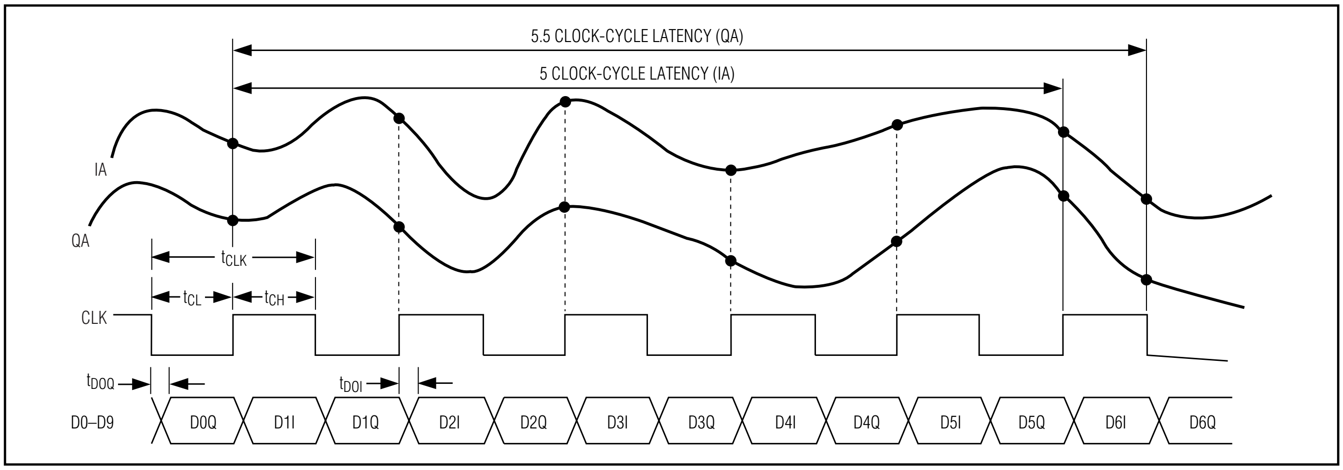


Figure 3. Rx ADC System Timing Diagram

Table 2. Tx DAC Output Voltage vs. Input Codes

(Internal Reference Mode V_{REFDAC} = 1.024V, External Reference Mode $V_{REFDAC} = V_{REFIN}$, V_{FS} = 400 for 800mV_{P-P} Full Scale)

DIFFERENTIAL OUTPUT VOLTAGE (V)	OFFSET BINARY (DA0–DA9)	INPUT DECIMAL CODE
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	11 1111 1111	1023
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	11 1111 1110	1022
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	10 0000 0001	513
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	10 0000 0000	512
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	01 1111 1111	511
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	00 0000 0001	1
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	00 0000 0000	0

The Tx DAC (IDN, IDP, QDN, QDP) are biased at an adjustable common-mode DC level and designed to drive a differential input stage with ≥ 70kΩ input impedance. This simplifies the analog interface between RF quadrature upconverters and the MAX19712. Many RF upconverters require a 0.89V to 1.36V common-mode bias. The MAX19712 common-mode DC bias eliminates discrete level-setting resistors and code-generated level shifting while preserving the full dynamic range of each Tx DAC. **The Tx DAC differential analog outputs cannot be used in single-ended mode because of the internally generated common-mode DC level.** Table 2 shows the Tx DAC output voltage vs. input codes. Table 10 shows the selection of DC common-mode levels. See Figure 4 for an illustration of the Tx DAC analog output levels.

The Tx DAC also features independent DC offset trim on each ID–QD channel. This feature is configured through the SPI interface. The DC offset correction is used to optimize sideband and carrier suppression in the Tx signal path (see Table 9).

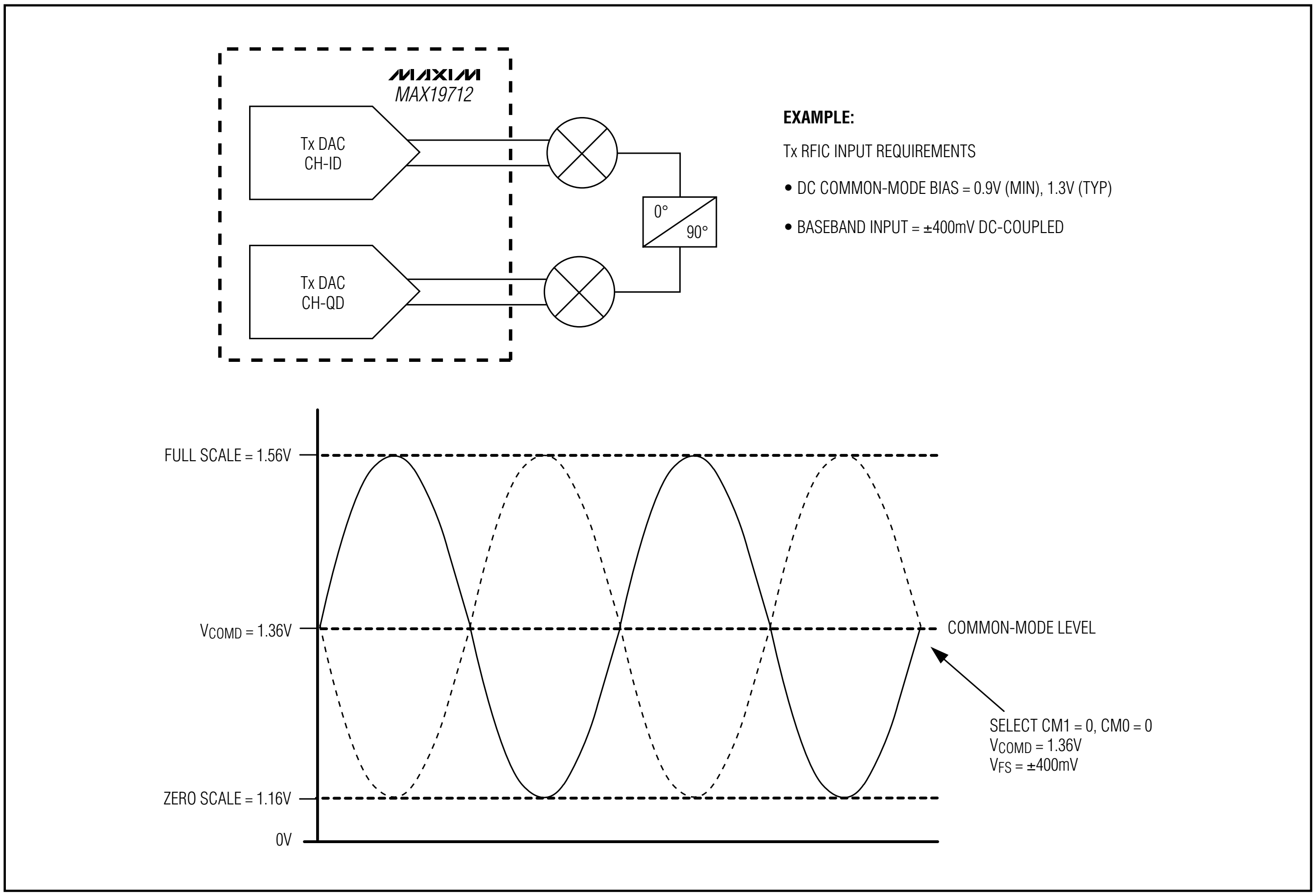


Figure 4. Tx DAC Common-Mode DC Level at IDN, IDP or QDN, QDP Differential Outputs

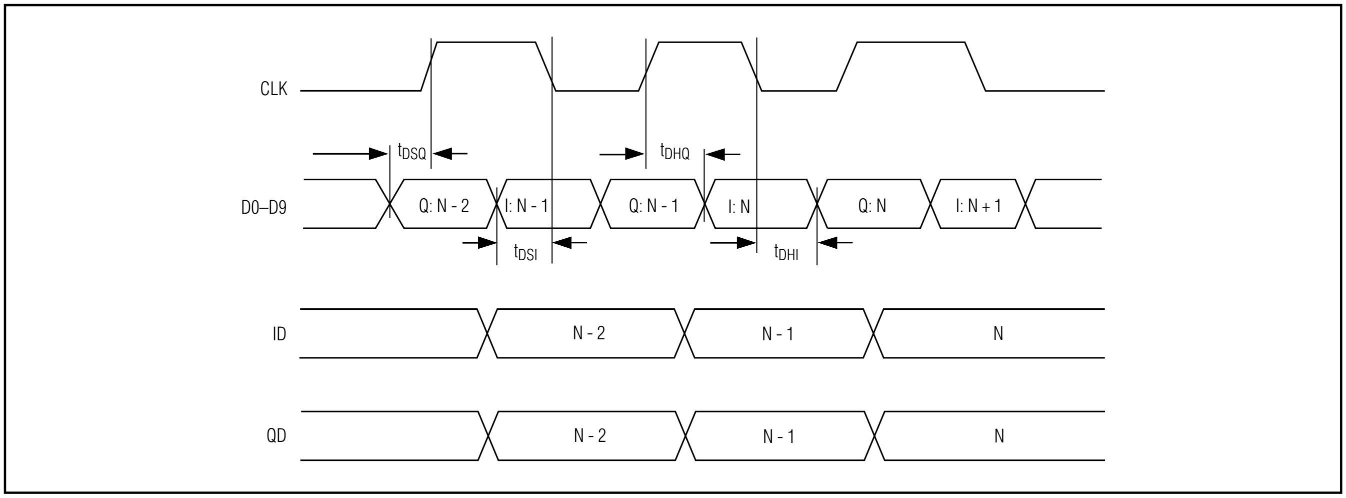


Figure 5. Tx DAC System Timing Diagram

Tx DAC Timing

Figure 5 shows the relationship among the clock, input data, and analog outputs. Channel ID data is latched on the falling edge of the clock signal, and channel QD data is latched on the rising edge of the clock signal, at which point both ID and QD outputs are simultaneously updated.

3-Wire Serial Interface and Operation Modes

The 3-wire serial interface controls the MAX19712 operation modes as well as the three 12-bit aux-DACs and the 10-bit aux-ADC. Upon power-up, program the MAX19712 to operate in the desired mode. Use the 3-wire serial interface to program the device for shutdown, idle, standby, FD, Rx, Tx, aux-DAC controls, or aux-ADC conversion. A 16-bit data register sets the mode control as shown in Table 3. The 16-bit word is composed of four control bits (A3–A0) and 12 data bits (D11–D0). Data is shifted in MSB first (D11) and LSB last (A0) format. Table 4 shows the MAX19712 power-management modes. Table 5 shows the SPI-controlled Tx, Rx, and FD modes. The serial interface remains active in all modes.

SPI Register Description

Program the control bits, A3–A0, in the register as shown in Table 3 to select the operating mode. Modify A3–A0 bits to select from ENABLE-16, Aux-DAC1, Aux-DAC2, Aux-DAC3, IOFFSET, QOFFSET, COMSEL, Aux-ADC, ENABLE-8, and WAKEUP-SEL modes. ENABLE-16 is the default operating mode (see Table 6). This mode allows for shutdown, idle, and standby states as well as switching between FAST, SLOW, Rx and Tx modes and the FD mode. Tables 4 and 5 show the required SPI settings for each mode.

In ENABLE-16 mode, the aux-DACs have independent control bits E4, E5, and E6, and bit E9 enables the aux-ADC. Table 7 shows the auxiliary DAC enable codes. Table 8 shows the auxiliary ADC enable code. Bits E11 and E10 are reserved. Program bits E11 and E10 to logic-low. Bits E3, E7, and E8 are not used.

Modes aux-DAC1, aux-DAC2, and aux-DAC3 select the aux-DAC channels named DAC1, DAC2, and DAC3 and hold the data inputs for each DAC. Bits _D11–_D0 are the data inputs for each aux-DAC and can be programmed through SPI. The MAX19712 also includes two 6-bit registers that can be programmed to adjust the offsets for the Tx DAC ID and QD channels independently (see Table 9). Use the COMSEL mode to select the output common-mode voltage with bits CM1 and CM0 (see Table 10). Use aux-ADC mode to start the auxiliary ADC conversion (see the *10-Bit, 333ksps Auxiliary ADC* section for details). Use ENABLE-8 mode for faster enable and switching between shutdown, idle, and standby states as well as switching between FAST, SLOW, Rx and Tx modes and the FD mode.

The WAKEUP-SEL register selects the operating mode that the MAX19712 is to enter immediately after coming out of shutdown (Table 11). See the *Wake-Up Function* section for more information.

Shutdown mode offers the most dramatic power savings by shutting down all the analog sections (including the reference) of the MAX19712. In shutdown mode, the Rx ADC digital outputs are in tri-state mode, the Tx DAC digital inputs are internally pulled to OV_{DD}, and the Tx DAC outputs are at 0V. When the Rx ADC outputs transition from tri-state to active mode, the last converted word is placed on the digital output bus. The Tx DAC previously stored data is lost when coming out of shutdown mode. The wake-up time from shutdown mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 500µs to enter Rx mode, 26.2µs to enter Tx mode, and 500µs to enter FD mode.

In all operating modes the Tx DAC inputs DA0–DA9 are internally pulled to OV_{DD}. To reduce the supply current of the MAX19712 in shutdown mode do not pull DA0–DA9 low. This consideration is especially important in shutdown mode to achieve the lowest quiescent current.

In idle mode, the reference and clock distribution circuits are powered, but all other functions are off. The Rx ADC outputs AD0–AD9 are forced to tri-state. The Tx DAC DA0–DA9 inputs are internally pulled to OV_{DD}, while the Tx DAC outputs are at 0V. The wake-up time is 7.2µs to enter Rx mode, 5.1µs to enter Tx mode, and 7.2µs to enter FD mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital output bus.

In standby mode, the reference is powered but all other device functions are off. The wake-up time from standby mode is 7.1µs to enter Rx mode, 22.8µs to enter Tx mode, and 22.8µs to enter FD mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital output bus.

FAST and SLOW Rx and Tx Modes

The MAX19712 features FAST and SLOW modes for switching between Rx and Tx operation. In FAST Tx mode, the Rx ADC core is powered on but the ADC digital outputs AD0–AD9 are tri-stated. The Tx DAC digital bus is active and the DAC core is fully operational.

In FAST Rx mode, the Tx DAC core is powered on. The Tx DAC outputs are set to midscale. In this mode, the Tx DAC input bus is disconnected from the DAC core and

Table 3. MAX19712 Mode Control

REGISTER NAME	D11 (MSB)	D10 15	D9 14	D8 13	D7 12	D6 11	D5 10	D4 9	D3 8	D2 7	D1 6	D0 5	A3 4	A2 3	A1 2	A0 1 (LSB)
ENABLE-16	E11 = 0 Reserved	E10 = 0 Reserved	E9	—	—	E6	E5	E4	—	E2	E1	E0	0	0	0	0
Aux-DAC1	1D11	1D10	1D9	1D8	1D7	1D6	1D5	1D4	1D3	1D2	1D1	1D0	0	0	0	1
Aux-DAC2	2D11	2D10	2D9	2D8	2D7	2D6	2D5	2D4	2D3	2D2	2D1	2D0	0	0	1	0
Aux-DAC3	3D11	3D10	3D9	3D8	3D7	3D6	3D5	3D4	3D3	3D2	3D1	3D0	0	0	1	1
IOFFSET	—	—	—	—	—	—	IO5	IO4	IO3	IO2	IO1	IO0	0	1	0	0
QOFFSET	—	—	—	—	—	—	QO5	QO4	QO3	QO2	QO1	QO0	0	1	0	1
COMSEL	—	—	—	—	—	—	—	—	—	—	CM1	CM0	0	1	1	0
Aux-ADC	AD11 = 0 Reserved	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0	1	1	1
ENABLE-8	—	—	—	—	—	—	—	—	—	E2	E1	E0	1	0	0	0
WAKEUP-SEL	—	—	—	—	—	—	—	—	—	W2	W1	W0	1	0	0	1

— = Not used.

Table 4. Power-Management Modes

ADDRESS				DATA BITS				MODE	FUNCTION (POWER MANAGEMENT)	DESCRIPTION	COMMENT
A3	A2	A1	A0	E9*	E2	E1	E0				
0000 (16-Bit Mode) or 1000 (8-Bit Mode)				1	0	0	0	SHDN	SHUTDOWN	Rx ADC = OFF Tx DAC = OFF (TX DAC outputs at 0V) Aux-DAC = OFF Aux-ADC = OFF CLK = OFF REF = OFF	Device is in complete shutdown.
				X**	0	0	1	IDLE	IDLE	Rx ADC = OFF Tx DAC = OFF (TX DAC outputs at 0V) Aux-DAC = Last State CLK = ON REF = ON	Fast turn-on time. Moderate idle power.
				X**	0	1	0	STBY	STANDBY	Rx ADC = OFF Tx DAC = OFF (TX DAC outputs at 0V) Aux-DAC = Last State CLK = OFF REF = ON	Slow turn-on time. Low standby power.

X = Don't care.
**Bit E9 is not available in 8-bit mode.*
***In IDLE and STBY modes, the aux-ADC can be turned on or off.*

Table 5. MAX19712 Tx, Rx, and FD Control Using SPI Commands

ADDRESS				DATA BITS			MODE	FUNCTION (Tx-Rx SWITCHING SPEED)	DESCRIPTION	COMMENT
A3	A2	A1	A0	E2	E1	E0				
0000 (16-Bit Mode) and 1000 (8-Bit Mode)				0	1	1	SPI1-Rx	SLOW	**Rx Mode:** Rx ADC = ON Rx Bus = Enabled Tx DAC = OFF (Tx DAC outputs at 0V) Tx Bus = OFF (all inputs are pulled high)	Slow transition to Tx mode from this mode. Low power.
				1	0	0	SPI2-Tx	SLOW	**Tx Mode:** Rx ADC = OFF Rx Bus = Tri-state Tx DAC = ON Tx Bus = ON	Slow transition to Rx mode from this mode. Low power.
				1	0	1	SPI3-Rx	FAST	**Rx Mode:** Rx ADC = ON Rx Bus = Enabled Tx DAC = ON (Tx DAC outputs at midscale) Tx Bus = OFF (all inputs are pulled high)	Fast transition to Tx mode from this mode. Moderate power.
				1	1	0	SPI4-Tx	FAST	**Tx Mode:** Rx ADC = ON Rx Bus = Tri-state Tx DAC = ON Tx Bus = ON	Fast transition to Rx mode from this mode. Moderate power.
				1	**1**	**1**	**FD**	**FAST**	**FD Mode:** Rx ADC = ON Rx Bus = ON Tx DAC = ON Tx Bus = ON	**Default Mode** Fast transition to any mode. Moderate power.

DA0–DA9 are internally pulled to OV_{DD}. The Rx ADC digital bus is active and the ADC core is fully operational.

In FAST mode, the switching time from Tx to Rx, or Rx to Tx is minimized because the converters are on and do not have to recover from a power-down state. In FAST mode, the switching time from Rx to Tx and Tx to Rx is 0.1µs. Power consumption is higher in FAST mode because both Tx and Rx cores are always on.

In SLOW Tx mode, the Rx ADC core is powered off and the ADC digital outputs AD0–AD9 are tri-stated. The Tx DAC digital bus is active and the DAC core is fully operational. In SLOW Rx mode, the Tx DAC core is powered off. The Tx DAC outputs are set to 0. In SLOW Rx mode, the Tx DAC input bus is disconnected from the DAC core and DA0–DA9 are internally pulled to OV_{DD}. The Rx ADC digital bus is active and the ADC core is fully operational. The switching times for SLOW modes are 5.1µs for Rx to Tx and 7.5µs for Tx to Rx.

Power consumption in SLOW Tx mode is 33.9mW, and 39.9mW in SLOW Rx mode. Power consumption in FAST Tx mode is 49.2mW, and 47.4mW in FAST Rx mode.

Table 6. MAX19712 Default (Power-On) Register Settings

<table>
<tr><th rowspan="2">REGISTER NAME</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><th>16 (MSB)</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th></tr>
<tr><td rowspan="2">ENABLE-16</td><td rowspan="2">0</td><td rowspan="2">0</td><td>0</td><td rowspan="2">—</td><td rowspan="2">—</td><td>0</td><td>0</td><td>0</td><td rowspan="2">—</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Aux-ADC = ON</td><td colspan="3">Aux-DAC1 to Aux-DAC3 = ON</td><td colspan="3">FD mode</td></tr>
<tr><td rowspan="2">Aux-DAC1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td colspan="12">DAC1 output set to 1.1V</td></tr>
<tr><td rowspan="2">Aux-DAC2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="12">DAC2 output set to 0V</td></tr>
<tr><td rowspan="2">Aux-DAC3</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="12">DAC3 output set to 0V</td></tr>
<tr><td rowspan="2">IOFFSET</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="6">No offset on channel ID</td></tr>
<tr><td rowspan="2">QOFFSET</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="6">No offset on channel QD</td></tr>
<tr><td rowspan="2">COMSEL</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td>0</td><td>0</td></tr>
<tr><td colspan="2">V_{COMD} = 1.36V</td></tr>
<tr><td rowspan="2">Aux-ADC</td><td rowspan="2">0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="11">Aux-ADC = ON, Conversion = IDLE, Aux-ADC REF = 2.048V, MUX = ADC1, Averaging = 1, Clock Divider = 1, DOUT = Disabled</td></tr>
<tr><td rowspan="2">ENABLE-8</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="3">FD mode</td></tr>
<tr><td rowspan="2">WAKEUP-SEL</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td rowspan="2">—</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="3">Wake-up state = FD mode</td></tr>
</table>

Table 7. Aux-DAC Enable Table (ENABLE-16 Mode)

E6	E5	E4	Aux-DAC3	Aux-DAC2	Aux-DAC1
0	0	0	ON	ON	ON
0	0	1	ON	ON	OFF
0	1	0	ON	OFF	ON
0	1	1	ON	OFF	OFF
1	0	0	OFF	ON	ON
1	0	1	OFF	ON	OFF
1	1	0	OFF	OFF	ON
1	1	1	OFF	OFF	OFF
0	**0**	**0**	**Default mode**		

Table 8. Aux-ADC Enable Table (ENABLE-16 Mode)

E9	SELECTION
0 (Default)	Aux-ADC is Powered ON
1	Aux-ADC is Powered OFF

FD Mode

The MAX19712 features an FD mode, which is ideal for applications supporting frequency-division duplex. In FD mode, both Rx ADC and Tx DAC, as well as their respective digital buses, are active and the device can receive and transmit simultaneously. Switching from FD mode to other Rx or Tx modes is fast (0.1µs) since

Table 9. Offset Control Bits for ID and QD Channels (IOFFSET or QOFFSET Mode)

BITS IO5–IO0 WHEN IN IOFFSET MODE, BITS QO5–QO0 WHEN IN QOFFSET MODE						OFFSET 1 LSB = (VFS$_{P-P}$ / 1023)
IO5/QO5	**IO4/QO4**	**IO3/QO3**	**IO2/QO2**	**IO1/QO1**	**IO0/QO0**	
1	1	1	1	1	1	-31 LSB
1	1	1	1	1	0	-30 LSB
1	1	1	1	0	1	-29 LSB
• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	0	0	0	1	0	-2 LSB
1	0	0	0	0	1	-1 LSB
1	0	0	0	0	0	0mV
0	0	0	0	0	0	0mV (Default)
0	0	0	0	0	1	1 LSB
0	0	0	0	1	0	2 LSB
• • •	• • •	• • •	• • •	• • •	• • •	• • •
0	1	1	1	0	1	29 LSB
0	1	1	1	1	0	30 LSB
0	1	1	1	1	1	31 LSB

Note: *1 LSB = (800mV$_{P-P}$ / 1023) = 0.782mV.*

Table 10. Common-Mode Select (COMSEL Mode)

CM1	CM0	Tx PATH OUTPUT COMMON MODE (V)
0	0	1.36 (Default)
0	1	1.20
1	0	1.05
1	1	0.89

the on-board converters are already powered. Consequently, power consumption in this mode is the maximum of all operating modes. In FD mode the MAX19712 consumes 50.4mW.

Wake-Up Function

The MAX19712 uses the SPI interface to control the operating modes of the device including the shutdown and wake-up functions. Once the device has been placed in shutdown through the appropriate SPI command, the first pulse on $\overline{CS}$/WAKE performs a wake-up function. At the first rising edge of $\overline{CS}$/WAKE, the MAX19712 is forced to a preset operating mode determined by the WAKEUP-SEL register. This mode is termed the wake-up state. If the WAKEUP-SEL register has not been programmed, the wake-up state for the MAX19712 is FD mode by default (Tables 6, 11). The WAKEUP-SEL register cannot be programmed with W2 = 0, W1 = 0, and W0 = 0. If this value is inadvertently written to the device, it is ignored and the register continues to store its previous value. Upon wake-up, the

Table 11. WAKEUP-SEL Register

W2	W1	W0	POWER MODE AFTER WAKE-UP (WAKE-UP STATE)
0	0	0	**Invalid Value**. This value is ignored when inadvertently written to the WAKEUP-SEL register.
0	0	1	IDLE
0	1	0	STBY
0	1	1	SPI1-SLOW Rx
1	0	0	SPI2-SLOW Tx
1	0	1	SPI3-FAST Rx
1	1	0	SPI4-FAST Tx
1	1	1	FD **(Default)**

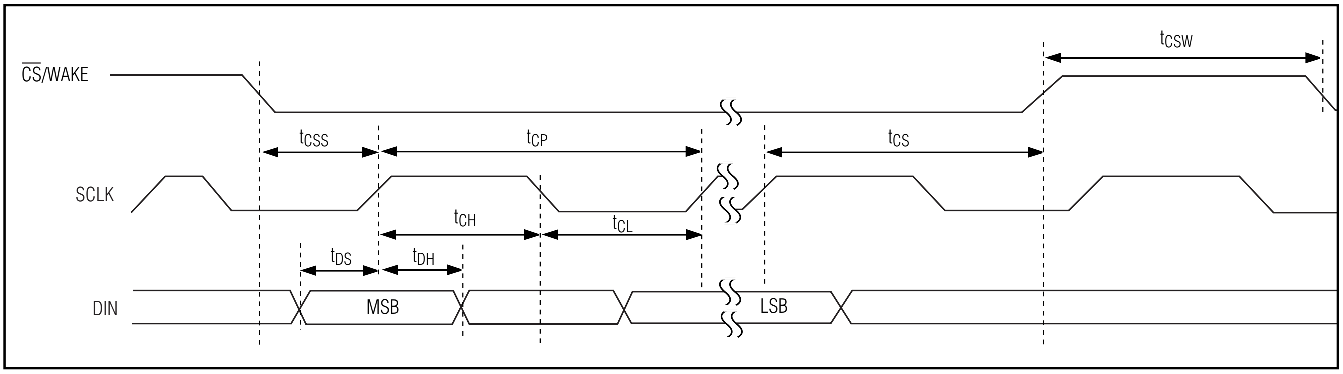


Figure 6. Serial-Interface Timing Diagram

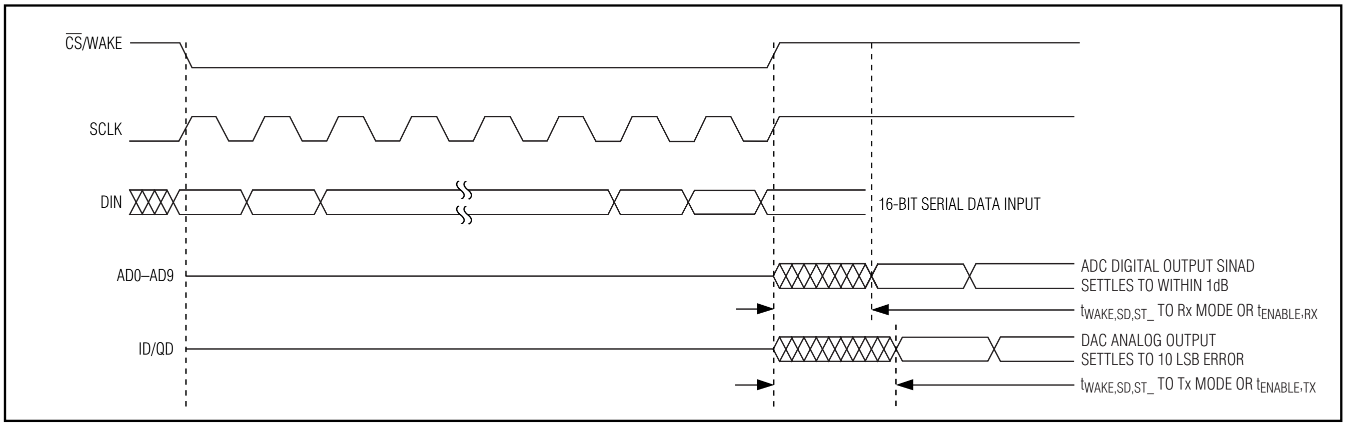


Figure 7. Mode-Recovery Timing Diagram

MAX19712 enters the power mode determined by the WAKEUP-SEL register, however, all other settings (Tx DAC offset, Tx DAC common-mode voltage, aux-DAC settings, aux-ADC state) are restored to their values prior to shutdown.

The only SPI line that is monitored by the MAX19712 during shutdown is $\overline{CS}$/WAKE. Any information transmitted to the MAX19712 concurrent with the $\overline{CS}$/WAKE wake-up pulse is ignored.

SPI Timing

The serial digital interface is a standard 3-wire connection ($\overline{CS}$/WAKE, SCLK, DIN) compatible with SPI/QSPI™/MICROWIRE/DSP interfaces. Set $\overline{CS}$/WAKE low to enable the serial data loading at DIN or output at DOUT. Following a $\overline{CS}$/WAKE high-to-low transition, data is shifted synchronously, most significant bit first, on the rising edge of the serial clock (SCLK). After 16 bits are loaded into the serial input register, data is transferred to the latch when $\overline{CS}$/WAKE transitions high. $\overline{CS}$/WAKE must transition high for a minimum of 80ns before the next write sequence. SCLK can idle either high or low between transitions. Figure 6 shows the detailed timing diagram of the 3-wire serial interface.

Mode-Recovery Timing

Figure 7 shows the mode-recovery timing diagram. t_{WAKE} is the wake-up time when exiting shutdown, idle, or standby mode and entering Rx, Tx, or FD mode. t_{ENABLE} is the recovery time when switching between either Rx or Tx mode. t_{WAKE} or t_{ENABLE} is the time for the Rx ADC to settle within 1dB of specified SINAD performance and Tx DAC settling to 10 LSB error. t_{WAKE} and t_{ENABLE} times are measured after the 16-bit serial command is latched into the MAX19712 by a $\overline{CS}$/WAKE transition high. In FAST mode, the recovery time is 0.1µs to switch between Tx or Rx modes.

QSPI is a trademark of Motorola, Inc.

System Clock Input (CLK)

Both the Rx ADC and Tx DAC share the CLK input. The CLK input accepts a CMOS-compatible signal level set by OV_{DD} from 1.8V to V_{DD}. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (< 2ns). Specifically, sampling occurs on the rising edge of the clock signal, requiring this edge to provide the lowest possible jitter. Any significant clock jitter limits the SNR performance of the on-chip Rx ADC as follows:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_{AJ}}\right)$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the clock jitter.

Clock jitter is especially critical for undersampling applications. Consider the clock input as an analog input and route away from any analog input or other digital signal lines. The MAX19712 clock input operates with an OV_{DD} / 2 voltage threshold and accepts a 50% ±10% duty cycle.

When the clock signal is stopped at CLK input (CLK = 0V or OV_{DD}), all internal registers hold their last value and the MAX19712 saves the last power-management mode or Tx/Rx/FD command. All converter circuits (Rx ADC, Tx DAC, aux-ADC, and aux-DACs) hold their last value. When the clock signal is restarted at CLK, allow 7.1µs (clock wake-up time) for the internal clock circuitry to settle before updating the Tx DAC, reading a valid Rx ADC conversion result, or starting an aux-ADC conversion. This ensures the converters (Rx ADC, Tx DAC, aux-ADC) meet all dynamic performance specifications. The aux-DAC channels are not dependent on CLK, so they may be updated when CLK is idle.

12-Bit, Auxiliary Control DACs

The MAX19712 includes three 12-bit aux-DACs (DAC1, DAC2, DAC3) with 1µs settling time for controlling variable-gain amplifier (VGA), automatic gain-control (AGC), and automatic frequency-control (AFC) functions. The aux-DAC output range is 0.2V to 2.57V as defined by V_{OH} - V_{OL}. During power-up, the VGA and AGC outputs (DAC2 and DAC3) are at zero. The AFC DAC (DAC1) is at 1.1V during power-up. The aux-DACs can be independently controlled through the SPI bus, except during SHDN mode where the aux-DACs are turned off completely and the output voltage is set to zero. In STBY and IDLE modes the aux-DACs maintain the last value. On wakeup from SHDN, the aux-DACs resume the last values.

Loading on the aux-DAC outputs should be carefully observed to achieve the specified settling time and stability. The capacitive load must be kept to a maximum of 5pF including package and trace capacitance. The resistive load must be greater than 200kΩ. If capacitive loading exceeds 5pF, then add a 10kΩ resistor in series with the output. Adding the series resistor helps drive larger load capacitance (< 15pF) at the expense of slower settling time.

10-Bit, 333ksps Auxiliary ADC

The MAX19712 integrates a 333ksps, 10-bit aux-ADC with an input 4:1 multiplexer. In the aux-ADC mode register, setting bit AD0 begins a conversion with the auxiliary ADC. Bit AD0 automatically clears when the conversion is complete. Setting or clearing AD0 during a conversion has no effect (see Table 12). Bit AD1 determines the internal reference of the auxiliary ADC (see Table 13). Bits AD2 and AD3 determine the auxiliary ADC input source (see Table 14). Bits AD4, AD5, and AD6 select the number of averages taken when a single start-convert command is given. The conversion time increases as the number of averages increases (see Table 15). The conversion clock can be divided down from the system clock by properly setting bits AD7, AD8, and AD9 (see Table 16). The aux-ADC output data can be written out of DOUT by setting bit AD10 high (see Table 17).

The aux-ADC features a 4:1 input multiplexer to allow measurements on four input sources. The input sources are selected by AD3 and AD2 (see Table 14). Two of the multiplexer inputs (ADC1 and ADC2) can be connected to external sources such as an RF power detector like the MAX2208 or temperature sensor like the MAX6613. The other two multiplexer inputs are internal connections to V_{DD} and OV_{DD} that monitor the power-supply voltages. The internal V_{DD} and OV_{DD} connections are made through integrated dividers that yield V_{DD} / 2 and OV_{DD} / 2 measurement results. The aux-ADC voltage reference can be selected between an internal 2.048V bandgap reference or V_{DD} (see Table 13). The V_{DD} reference selection is provided to allow measurement of an external voltage source with a full-scale range extending beyond the 2.048V level. The input source voltage range cannot extend above V_{DD}.

The conversion requires 12 clock edges (1 for input sampling, 1 for each of the 10 bits, and 1 at the end for loading into the serial output register) to complete one conversion cycle (when no averaging is being done). Each conversion of an average (when averaging is set greater than 1) requires 12 clock edges. The conversion clock is generated from the system clock input (CLK). An SPI-programmable divider divides the system

Table 12. Auxiliary ADC Convert

AD0	SELECTION
0	Aux-ADC Idle (Default)
1	Aux-ADC Start-Convert

Table 13. Auxiliary ADC Reference

AD1	SELECTION
0	Internal 2.048V Reference (Default)
1	Internal V_{DD} Reference

Table 14. Auxiliary ADC Input Source

AD3	AD2	Aux-ADC INPUT SOURCE
0	0	ADC1 (Default)
0	1	ADC2
1	0	V_{DD} / 2
1	1	OV_{DD} / 2

Table 15. Auxiliary ADC Averaging

AD6	AD5	AD4	Aux-ADC AVERAGING
0	0	0	1 Conversion (No Averaging) (Default)
0	0	1	Average of 2 Conversions
0	1	0	Average of 4 Conversions
0	1	1	Average of 8 Conversions
1	0	0	Average of 16 Conversions
1	0	1	Average of 32 Conversions
1	1	X	Average of 32 Conversions

X = Don't care.

clock by the appropriate divisor (set with bits AD7, AD8, and AD9; see Table 16) and provides the conversion clock to the auxiliary ADC. The auxiliary ADC has a maximum conversion rate of 333ksps. The maximum conversion clock frequency is 4MHz (333ksps x 12 clocks). Choose the proper divider value to keep the conversion clock frequency under 4MHz, based upon the system CLK frequency supplied to the MAX19712 (see Table 16). The total conversion time (t_{CONV}) of the auxiliary ADC can be calculated as $t_{CONV} = (12 \times N_{AVG} \times N_{DIV}) / f_{CLK}$; where N_{AVG} is the number of averages (see Table 15), N_{DIV} is the CLK divisor (see Table 16), and f_{CLK} is the system CLK frequency.

Table 16. Auxiliary ADC Clock (CLK) Divider

AD9	AD8	AD7	Aux-ADC CONVERSION CLOCK
0	0	0	CLK Divided by 1 (Default)
0	0	1	CLK Divided by 2
0	1	0	CLK Divided by 4
0	1	1	CLK Divided by 8
1	0	0	CLK Divided by 16
1	0	1	CLK Divided by 32
1	1	0	CLK Divided by 64
1	1	1	CLK Divided by 128

Table 17. Auxiliary ADC Data Output Mode

AD10	SELECTION
0	Aux-ADC Data is Not Available on DOUT (Default)
1	Aux-ADC Enters Data Output Mode Where Data is Available on DOUT

Reading DOUT from the Aux-ADC

DOUT is normally in a high-impedance condition. Upon setting the auxiliary ADC start conversion bit (bit AD0), DOUT becomes active and goes high, indicating that the aux-ADC is busy. When the conversion cycle is complete (including averaging), the data is placed into an output register and DOUT goes low, indicating that the output data is ready to be driven onto DOUT. When bit AD10 is set (AD10 = 1), the aux-ADC enters a data output mode where data is available at DOUT on the next low assertion of $\overline{CS}$/WAKE. The auxiliary ADC data is shifted out of DOUT (MSB first) with the data transitioning on the falling edge of the serial clock (SCLK). Since a DOUT read requires 16 bits, DOUT holds the value of the last conversion data bit for the last 6 bits (6 least significant bits) following the aux-ADC conversion data. DOUT enters a high-impedance state when $\overline{CS}$/WAKE is deasserted high. When bit AD10 is cleared (AD10 = 0), the aux-ADC data is not available on DOUT (see Table 17).

After the aux-ADC completes a conversion, the data result is loaded to an output register waiting to be shifted out. No further conversions are possible until data is shifted out. This means that if the first conversion command sets AD10 = 0, AD0 = 1, then it cannot be followed by conversion commands setting AD10 = 0, AD0 = 1 or AD10 = 1, AD0 = 1. If this sequence of commands is inadvertently used then DOUT is disabled. To resume normal operation set AD0 = 0.

The fastest method to perform sequential conversions with the aux-ADC is by sending consecutive commands setting AD10 = 1, AD0 = 1. With this sequence the $\overline{\text{CS}}$/WAKE falling edge shifts data from the previous conversion on to DOUT and the rising edge of $\overline{\text{CS}}$/WAKE loads the next conversion command at DIN. Allow enough time for each conversion to complete before sending the next conversion command. See Figure 8 for single and continuous conversion examples.

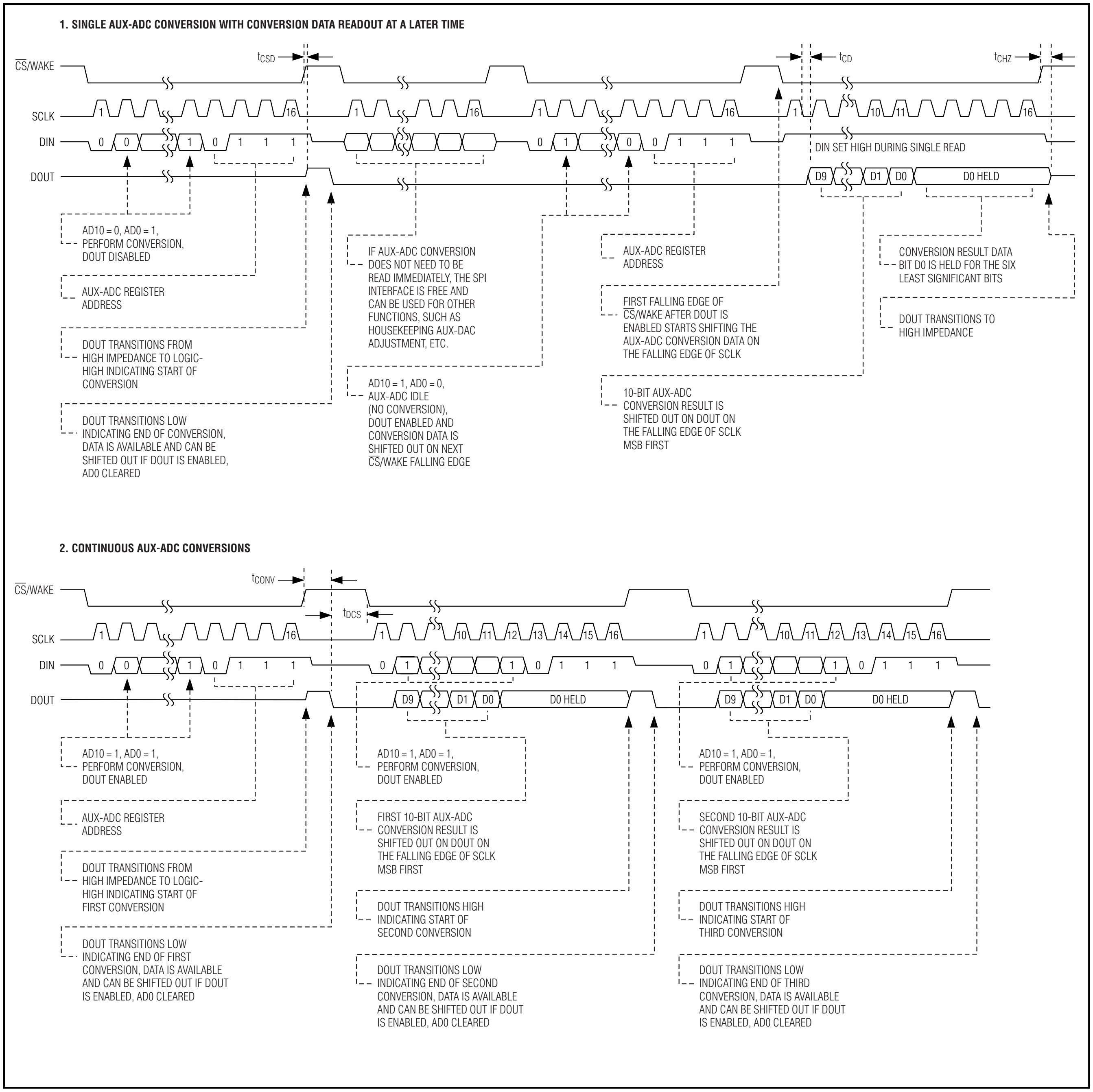


Figure 8. Aux-ADC Conversions Timing

DIN can be written independent of DOUT state. A 16-bit instruction at DIN updates the device configuration. To prevent modifying internal registers while reading data from DOUT, hold DIN at a high state (only applies if sequential aux-ADC conversions are not executed). This effectively writes all ones into address 1111. Since address 1111 does not exist, no internal registers are affected.

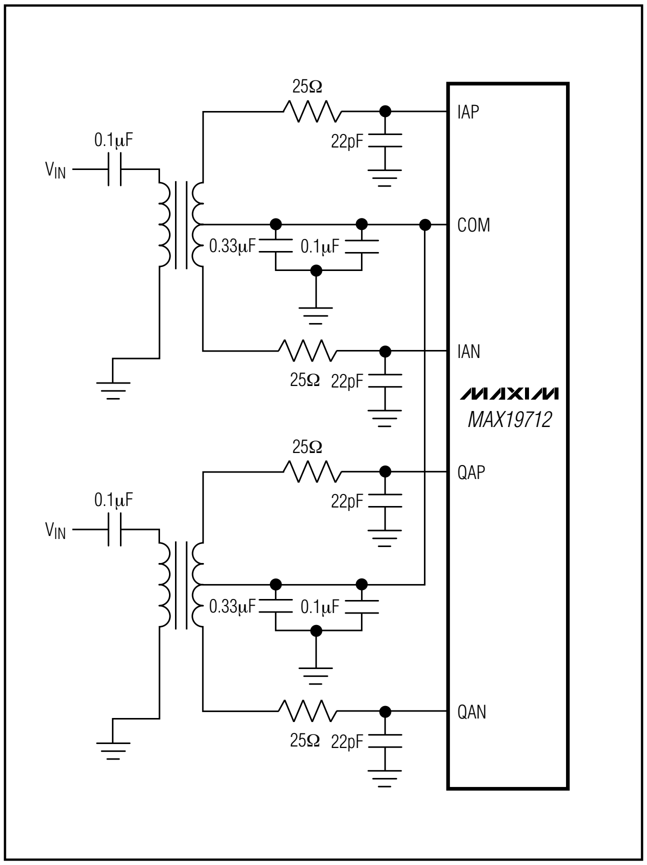


Figure 9. Balun Transformer-Coupled Single-Ended-to-Differential Input Drive for Rx ADC

Reference Configurations

The MAX19712 features an internal precision 1.024V bandgap reference that is stable over the entire power-supply and temperature ranges. The REFIN input provides two modes of reference operation. The voltage at REFIN (V_{REFIN}) sets the reference operation mode (Table 18).

In internal reference mode, connect REFIN to V_{DD}. V_{REF} is an internally generated 0.512V ±4% reference level. COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REF} / 2$, and $V_{REFN} = V_{DD} / 2 - V_{REF} / 2$. Bypass REFP, REFN, and COM each with a 0.33μF capacitor. Bypass REFIN to GND with a 0.1μF capacitor.

In buffered external reference mode, apply 1.024V ±10% at REFIN. In this mode, COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REFIN} / 4$, and $V_{REFN} = V_{DD} / 2 - V_{REFIN} / 4$. Bypass REFP, REFN, and COM each with a 0.33μF capacitor. Bypass REFIN to GND with a 0.1μF capacitor. In this mode, the Tx path full-scale output is proportional to the external reference. For example, if the V_{REFIN} is increased by 10% (max), the Tx path full-scale output is also increased by 10% or ±440mV.

Applications Information

Using Balun Transformer AC-Coupling

An RF transformer (Figure 9) provides an excellent solution to convert a single-ended signal source to a fully differential signal for optimum ADC performance. Connecting the center tap of the transformer to COM provides a V_{DD} / 2 DC level shift to the input. A 1:1 transformer can be used, or a step-up transformer can be selected to reduce the drive requirements. In general, the MAX19712 provides better SFDR and THD with fully differential input signals than single-ended signals, especially for high input frequencies. In differential mode, even-order harmonics are lower as both inputs (IAP, IAN, QAP, QAN) are balanced, and each of the Rx ADC inputs only requires half the signal swing com-

Table 18. Reference Modes

V_{REFIN}	REFERENCE MODE
> 0.8V x V_{DD}	Internal Reference Mode. V_{REF} is internally generated to be 0.512V. Bypass REFP, REFN, and COM each with a 0.33μF capacitor.
1.024V ±10%	Buffered External Reference Mode. An external 1.024V ±10% reference voltage is applied to REFIN. V_{REF} is internally generated to be V_{REFIN} / 2. Bypass REFP, REFN, and COM each with a 0.33μF capacitor. Bypass REFIN to GND with a 0.1μF capacitor.

pared to single-ended mode. Figure 10 shows an RF transformer converting the MAX19712 Tx DAC differential analog outputs to single-ended.

Using Op-Amp Coupling

Drive the MAX19712 Rx ADC with op amps when a balun transformer is not available. Figures 11 and 12 show the Rx ADC being driven by op amps for AC-coupled single-ended and DC-coupled differential applications. Amplifiers such as the MAX4454 and MAX4354 provide high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity. The op-amp circuit shown in Figure 12 can also be used to interface with the Tx DAC differential analog outputs to provide gain or buffering. The Tx DAC differential analog outputs cannot be used in single-ended mode because of the internally generated common-mode level. Also, the Tx DAC analog outputs are designed to drive a differential input stage with input impedance ≥ 70kΩ. If single-ended outputs are desired, use an amplifier to provide differential-to-single-ended conversion and select an amplifier with proper input common-mode voltage range.

FDD Application

Figure 13 illustrates a typical FDD application circuit. The MAX19712 interfaces directly with the MAX2392 and MAX2395 provide a complete “RF-to-Bits” front-end solution for WCDMA applications. The MAX19712 can also interface with the MAX2021 in RFID applications and other radio systems. The MAX19712 provides system benefits to digital baseband developers:

- Fast Time-to-Market
- High-Performance, Low-Power Analog Functions
- Low-Risk, Proven Analog Front-End Solution
- No Mixed-Signal Test Times
- No NRE Charges
- No IP Royalty Charges
- Enables Digital Baseband and Scale with 65nm to 90nm CMOS

Grounding, Bypassing, and Board Layout

The MAX19712 requires high-speed board layout design techniques. Refer to the MAX19712 EV kit data sheet for a board layout reference. Place all bypass capacitors as close to the device as possible, preferably on the same side of the board as the device, using surface-mount devices for minimum inductance. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor in parallel with a 2.2µF capacitor. Bypass OV_{DD} to OGND with a 0.1µF ceramic capacitor in parallel with a 2.2µF capacitor. Bypass REFP, REFN, and COM each to GND with a 0.33µF ceramic capacitor. Bypass REFIN to GND with a 0.1µF capacitor.

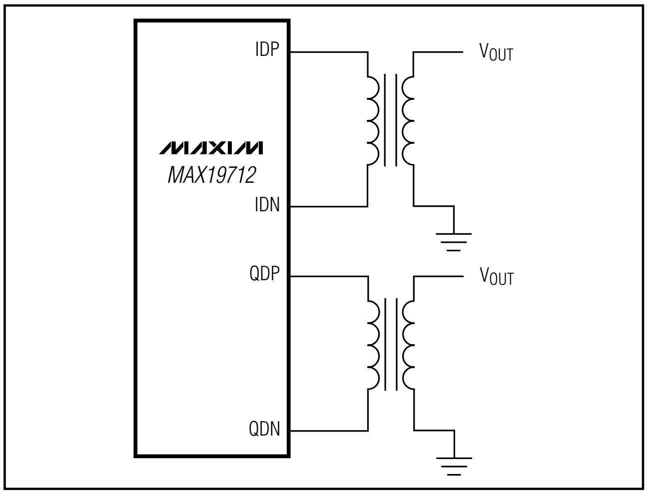


Figure 10. Balun Transformer-Coupled Differential-to-Single-Ended Output Drive for Tx DAC

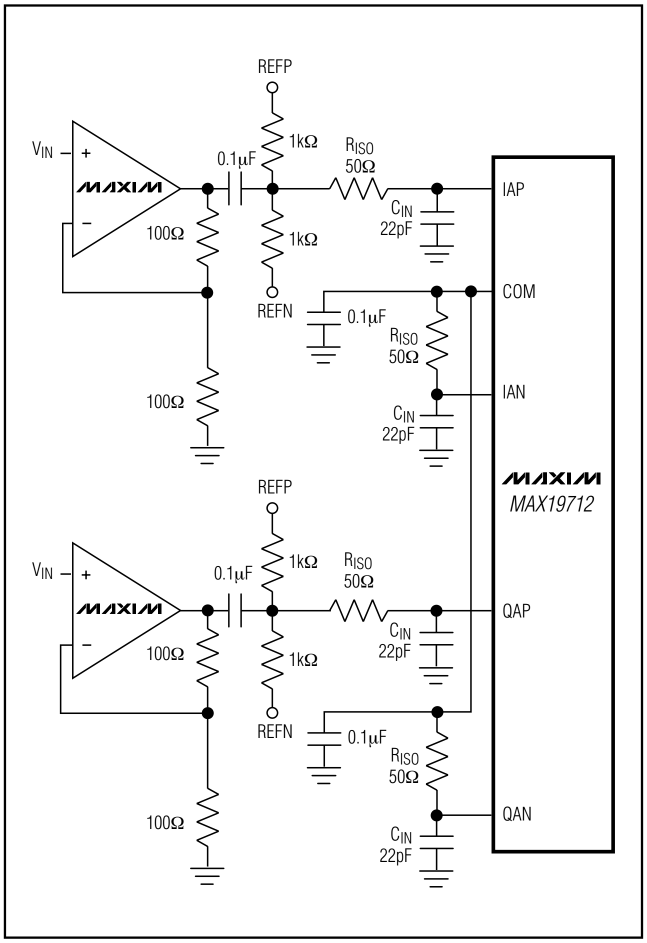


Figure 11. Single-Ended Drive for Rx ADC

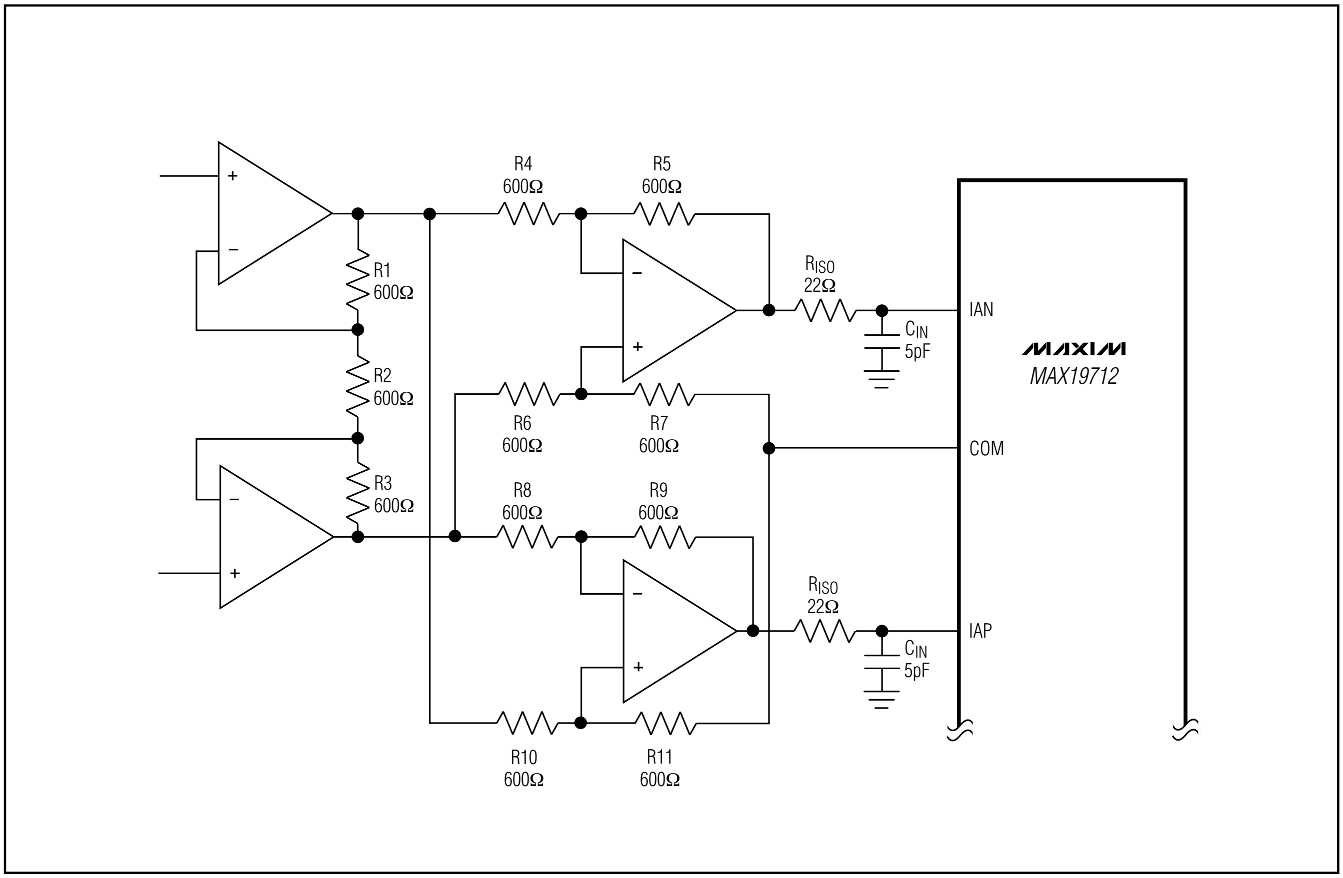


Figure 12. Rx ADC DC-Coupled Differential Drive

Multilayer boards with separated ground and power planes yield the highest level of signal integrity. Use a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output-driver ground (OGND) on the device package. Connect the MAX19712 exposed backside paddle to the GND plane. Join the two ground planes at a single point so the noisy digital ground currents do not interfere with the analog ground plane. The ideal location for this connection can be determined experimentally at a point along the gap between the two ground planes. Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead, or a direct short. Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy digital system's ground plane (e.g., downstream output buffer or DSP ground plane).

Route high-speed digital signal traces away from sensitive analog traces. Make sure to isolate the analog input lines to each respective converter to minimize channel-to-channel crosstalk. Keep all signal lines short and free of 90° turns.

Dynamic Parameter Definitions

ADC and DAC Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the device are measured using the best-straight-line fit (DAC Figure 14a).

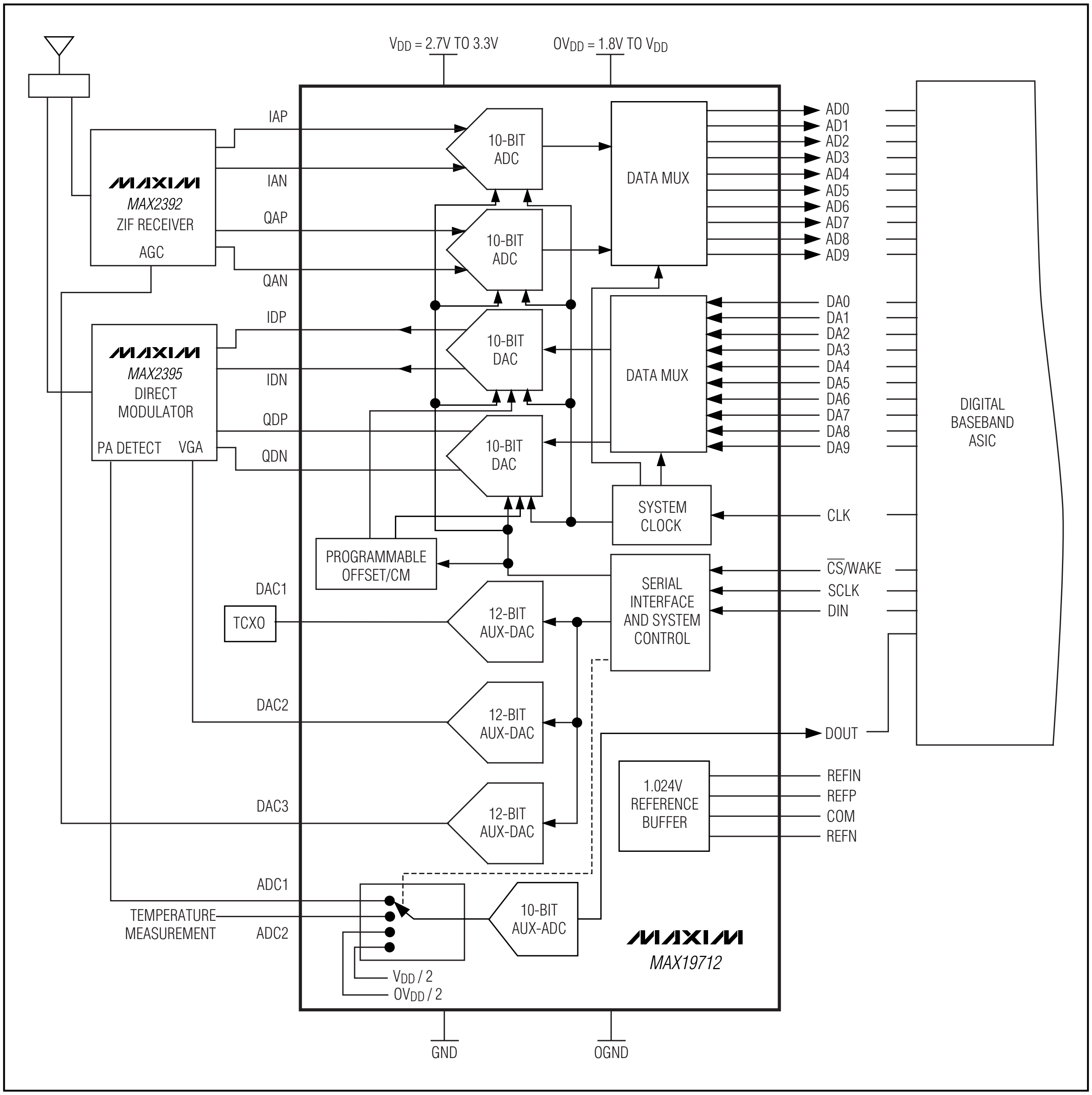


Figure 13. Typical WCDMA Application Circuit

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes (ADC) and a monotonic transfer function (ADC and DAC) (DAC Figure 14b).

ADC Offset Error

Ideally, the midscale transition occurs at 0.5 LSB above midscale. The offset error is the amount of deviation between the measured transition point and the ideal transition point.

DAC Offset Error

Offset error (Figure 14a) is the difference between the ideal and actual offset point. The offset point is the output value when the digital input is midscale. This error affects all codes by the same amount and usually can be compensated by trimming.

ADC Gain Error

Ideally, the ADC full-scale transition occurs at 1.5 LSB below full scale. The gain error is the amount of deviation between the measured transition point and the ideal transition point with the offset error removed.

ADC Dynamic Parameter Definitions

Aperture Jitter

Figure 15 shows the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 15).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error) and results directly from the ADC's resolution (N bits):

$$SNR(max) = 6.02 \times N + 1.76 \text{ (in dB)}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise and Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

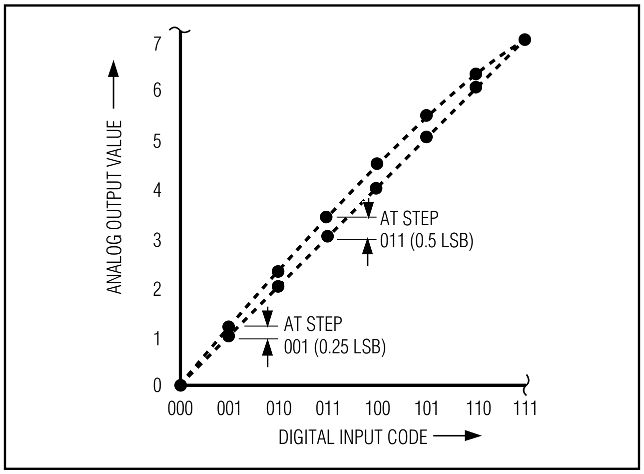


Figure 14a. Integral Nonlinearity

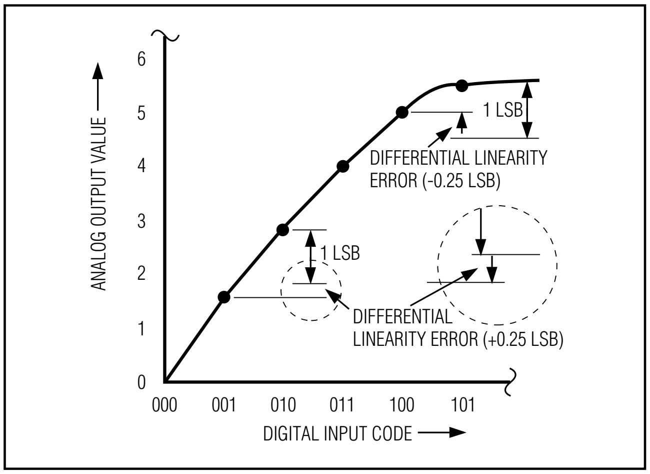


Figure 14b. Differential Nonlinearity

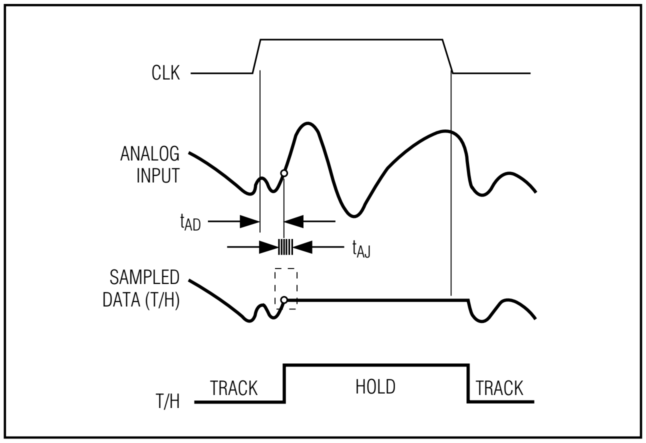


Figure 15. T/H Aperture Timing

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$$

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log\left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2–V_6 are the amplitudes of the 2nd- through 6th-order harmonics.

Third Harmonic Distortion (HD3)

HD3 is defined as the ratio of the RMS value of the third harmonic component to the fundamental input signal.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

IMD is the total power of the intermodulation products relative to the total input power when two tones, f_{IN1} and f_{IN2}, are present at the inputs. The intermodulation products are ($f_{IN1} \pm f_{IN2}$), ($2 \times f_{IN1}$), ($2 \times f_{IN2}$), ($2 \times f_{IN1} \pm f_{IN2}$), ($2 \times f_{IN2} \pm f_{IN1}$). The individual input tone levels are at -7dBFS.

3rd-Order Intermodulation (IM3)

IM3 is the power of the worst 3rd-order intermodulation product relative to the input power of either input tone when two tones, f_{IN1} and f_{IN2}, are present at the inputs. The 3rd-order intermodulation products are ($2 \times f_{IN1} \pm f_{IN2}$), ($2 \times f_{IN2} \pm f_{IN1}$). The individual input tone levels are at -7dBFS.

Power-Supply Rejection

Power-supply rejection is defined as the shift in offset and gain error when the power supply is changed ±5%.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in such a way that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. Note that the T/H performance is usually the limiting factor for the small-signal input bandwidth.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as the full-power bandwidth frequency.

DAC Dynamic Parameter Definitions

Total Harmonic Distortion

THD is the ratio of the RMS sum of the output harmonics up to the Nyquist frequency divided by the fundamental:

$$\text{THD} = 20 \times \log\left[\frac{\sqrt{(V_2^2 + V_3^2 + \ldots + V_n^2)}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2 through V_n are the amplitudes of the 2nd through nth harmonic up to the Nyquist frequency.

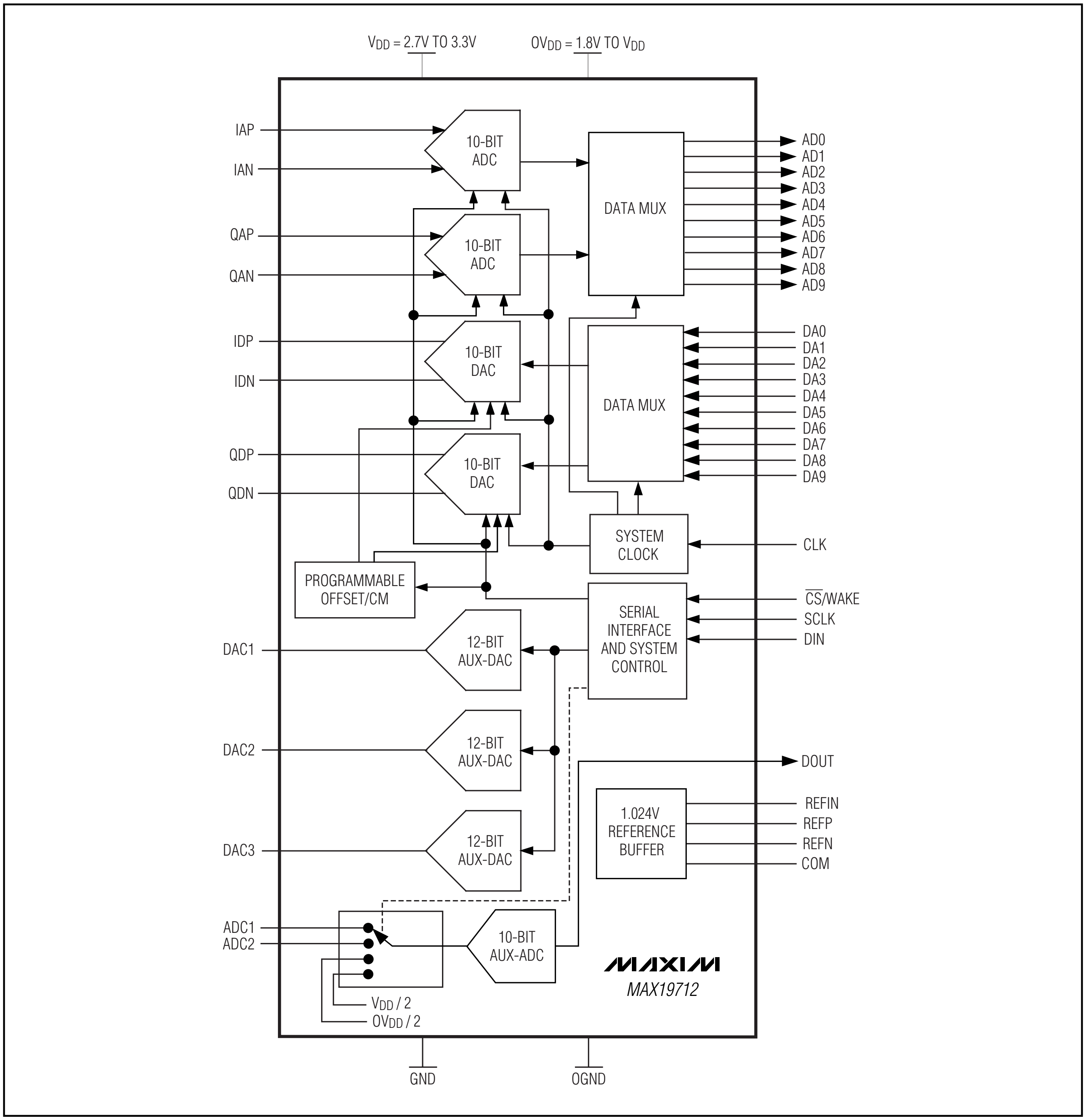
Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component up to the Nyquist frequency excluding DC.

Selector Guide

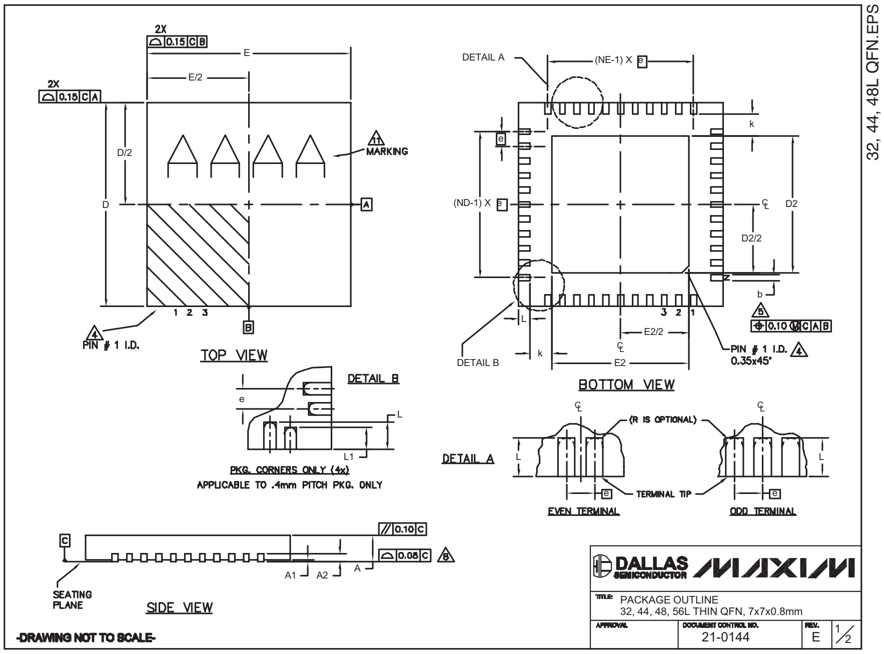
PART	SAMPLING RATE (Msps)	INTEGRATED CDMA Tx FILTERS
MAX19710	7.5	No
MAX19711	11	Yes
MAX19712	22	No
MAX19713	45	No

Functional Diagram



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.40	0.50	0.60
L1	–	–	–	–	–	–	–	–	–	–	–	–	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C	DOWN BONDS ALLOWED
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–	YES
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–	NO
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–	NO
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T4877-4	–	5.45	5.60	5.63	5.45	5.60	5.63	–	YES
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–	NO
T4877-6	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T5677-1	–	5.20	5.30	5.40	5.20	5.30	5.40	–	YES

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED.
TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	E	2/2